Swiss participation in AIDAinnova

This project has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 101004761.

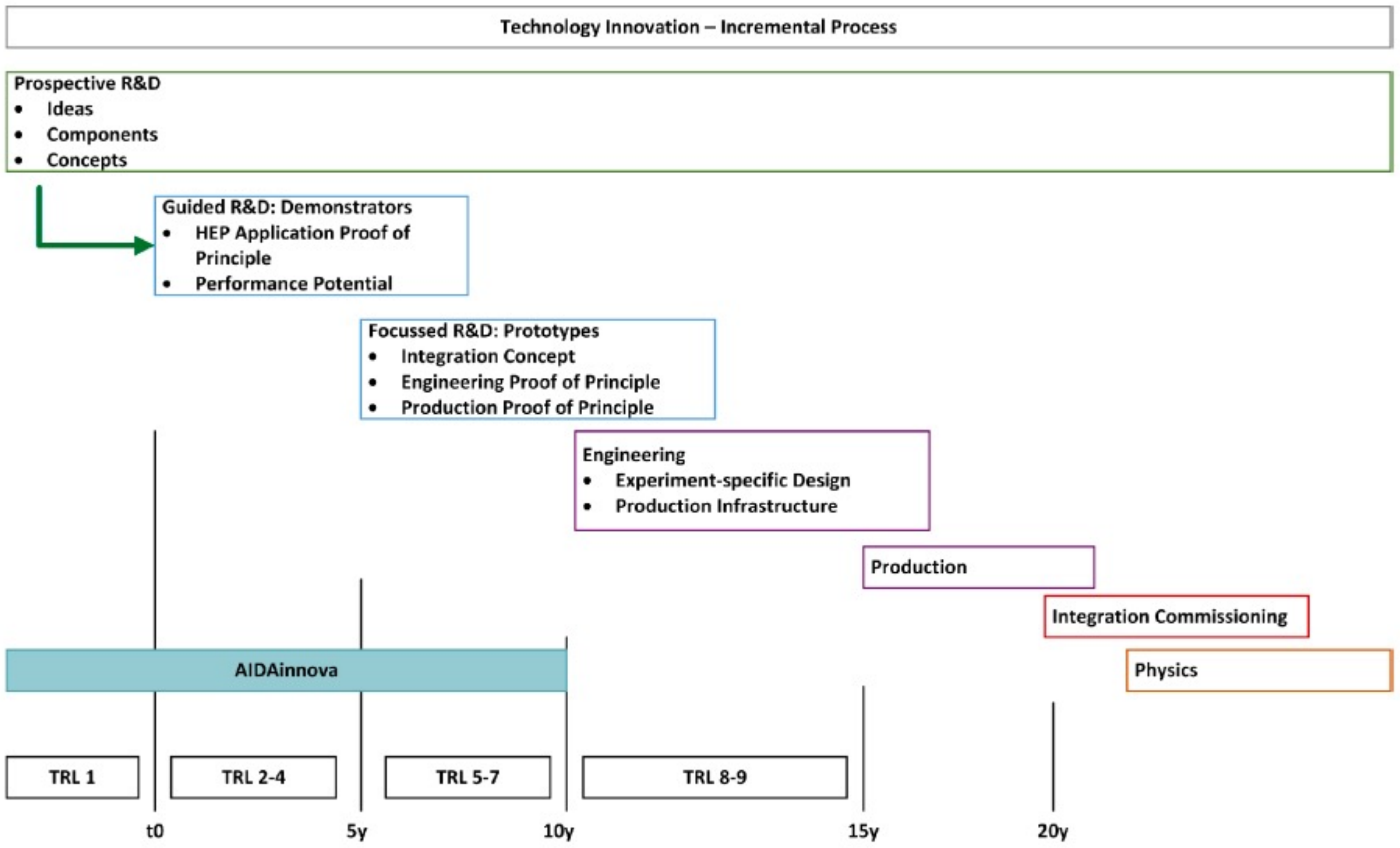
AIDAinnova scope

AIDAinnova focusses on Strategic R&D in the pre-TDR phase

- Technology Readiness Levels 2-7
- Not yet experiment-specific: potential to unfold synergies **Include some prospective R&D**
- competitive call at start of project • "Blue Sky", quantum sensors,…

Targeted applications

- Higgs Factories
- ALICE, LHCb LS3 pre-TDR, ATLAS & CMS LS4
- Accelerator-based neutrino experiments
- and others



Technology Innovation – Incremental Process

Prospective R&D
- Ideas
- Components
- Concepts

Guided R&D: Demonstrators
- HEP Application Proof of Principle
- Performance Potential

Focussed R&D: Prototypes
- Integration Concept
- Engineering Proof of Principle
- Production Proof of Principle

Engineering
- Experiment-specific Design
- Production Infrastructure

Production

Integration Commissioning

Physics

AIDAinnova

TRL 1 | TRL 2-4 | TRL 5-7 | TRL 8-9

t0 | 5y | 10y | 15y | 20y

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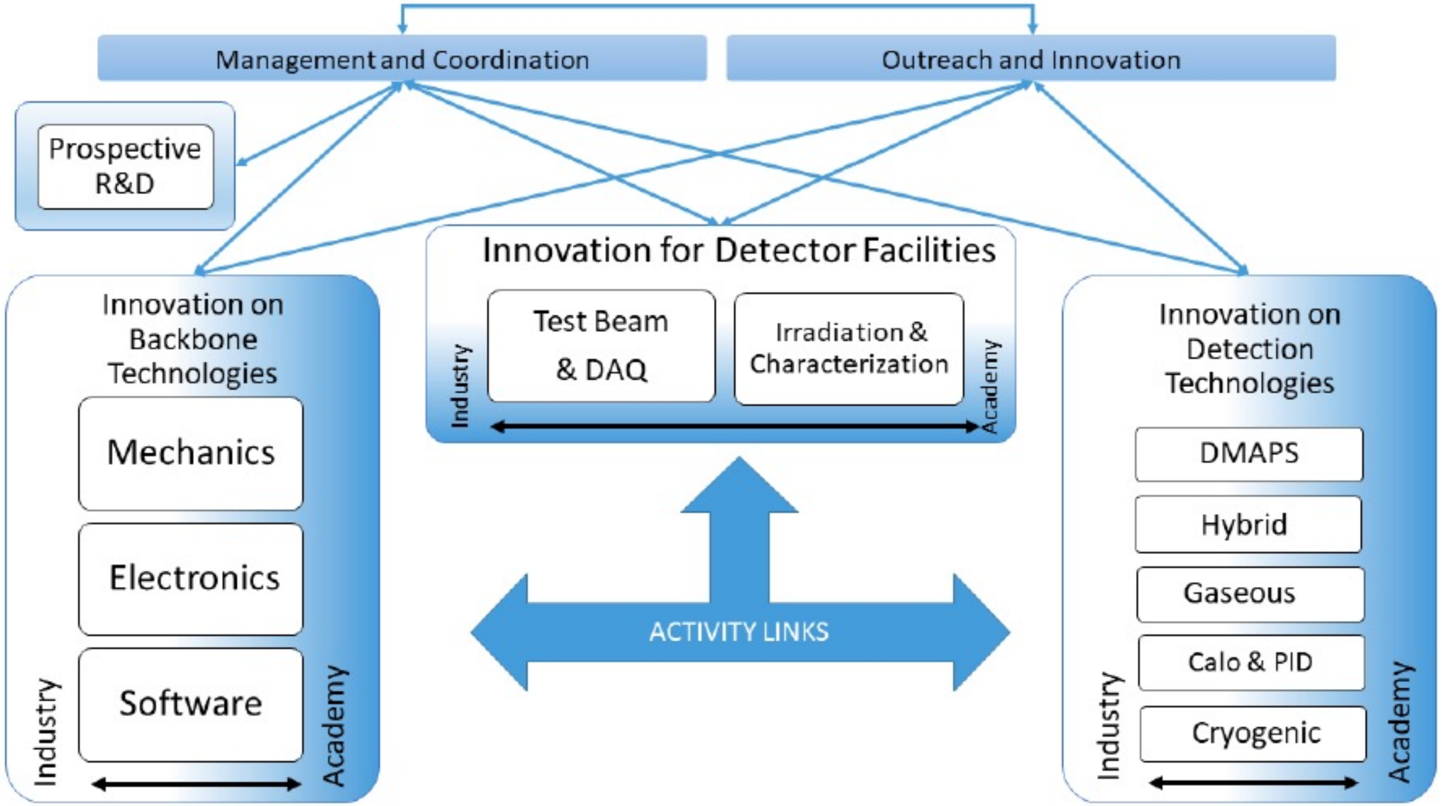
AIDAinnova: Work Packages


Management and Coordination

Outreach and Innovation

Prospective R&D

Innovation for Detector Facilities

- Test Beam & DAQ
- Irradiation & Characterization

Industry ↔ Academy

Innovation on Backbone Technologies

- Mechanics
- Electronics
- Software

Industry ↔ Academy

Innovation on Detection Technologies

- DMAPS
- Hybrid
- Gaseous
- Calo & PID
- Cryogenic

Industry ↔ Academy

ACTIVITY LINKS

Similarities with
- AIDA-2020
- CERN Detector R&D
- ECFA Detector Roadmap

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WP5: Depleted Monolithic Active Pixel Sensors

DMAPS development

High rate & radiation:
radhard (TID & NIEL) + fast resp. time + fast R/O
example: LHC upgrades & FCC

High granularity:
excellent spatial resolution + (fast + radhard):
ex.: Belle II upgrade & future Higgs factory etc.

concrete development lines

Foundry line	chips dev. line	charge coll.	high rate & radiation	high granularity	special aim
LFoundry 150 nm	LF-Monopix2	large electrode	X		radhard, robust
LFoundry 150 nm	LF-MPW3/4	large electrode	X	(X)	small pixels
TowerJazz 180 nm	TJ-Monopix2/3	small electrode	(X)	X	Belle II Upgrade
TowerJazz 180 nm	TJ-MALTA2/3	small electrode	X	(X)	low power
LFoundry 110 nm	ARCADIA	small electrode		X	large area, low power
TowerJazz 65 nm	TJ 65	tbd ... likely small		X	small feature size

WP5 convenors: Sebastian Grinstein (IFAE Barcelona), David-Leon Pohl, NW (Univ. of Bonn)

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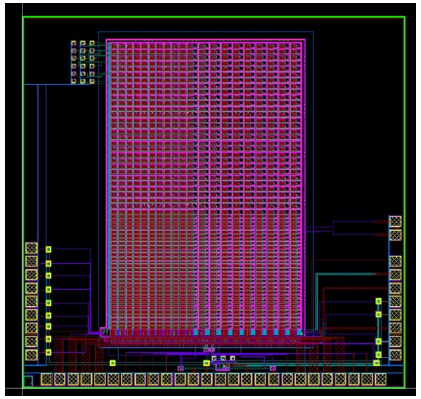
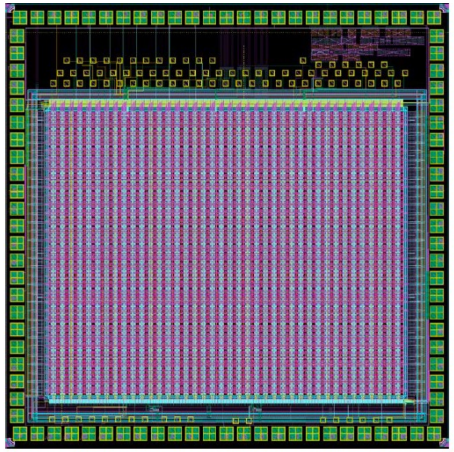
WP5: PSI activities

- PSI is partner organization in AIDAinnova – WP5: Depleted Monolithic Active Pixel Sensors
- Development of radiation tolerant Depleted Monolithic Active Pixel Sensors (DMAPS) for high-rate applications
  - in close collaboration with ETH and UZH
- For future upgrades of the CMS experiment, future collider experiments, in-house experiments and other applications
- Effort started in 2018
- Evaluated different technologies, now following up two (TSI and Lfoundry110) with own submissions
- More information in this Tilman Rohe's talk



Pixel chip in TSI prototype run:

- *4 different pixel sizes*
- *Discriminator in each pixel with 3 trim bits*
- *External hold possible (as in R4S chip)*



Motic A: Monolithic timing chip

- *LF110 nm with back-side implant*
- *Pulse height and time of arrival is measured*
- *5x5 mm^2 chip with different preamplifier designs*

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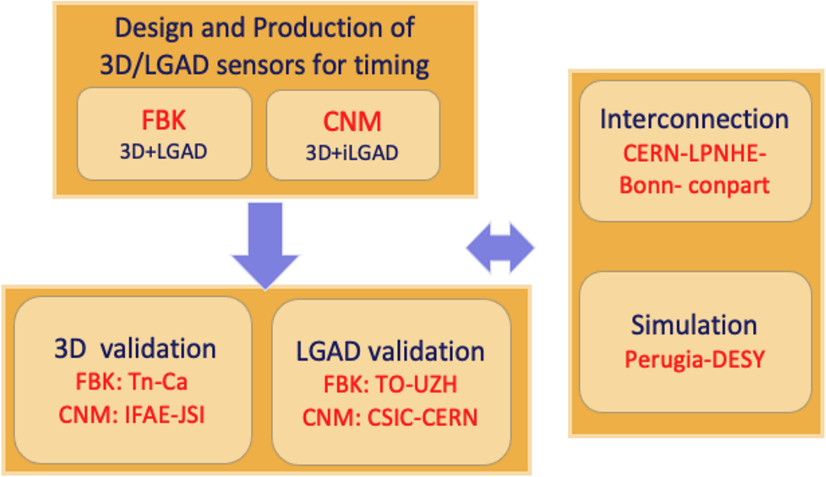
WP6:Timing detectors

WP6 Work Plan



Design and Production of 3D/LGAD sensors for timing

FBK
3D+LGAD

CNM
3D+iLGAD

3D validation
FBK: Tn-Ca
CNM: IFAE-JSI

LGAD validation
FBK: TO-UZH
CNM: CSIC-CERN

Interconnection
CERN-LPNHE-Bonn- conpart

Simulation
Perugia-DESY

Timing applications @ FCC

- 4D Tracking and pile-up mitigation at FCC-hh
- Potential applications at FCC-ee:
  - Interest for use as a PID detector
  - Search for long-lived particles
  - Studies of the characteristics of events from different regions of the interacting bunches

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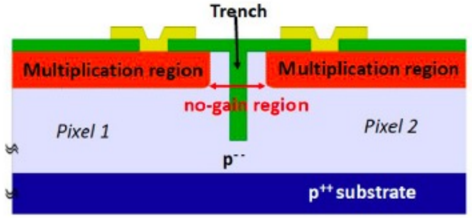
WP6: Technologies for 3D and pixelated LGADs

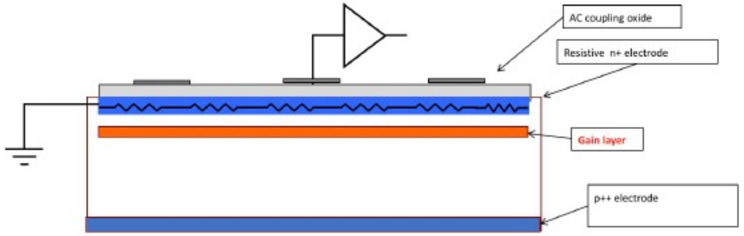
Low Gain Avalanche Diode (LGAD) detectors proposed for timing applications: upgrades of Endcap timing layer in CMS and High Granularity Timing Detector in ATLAS.

- In WP6 pushing for higher segmentation and rad-hardness.

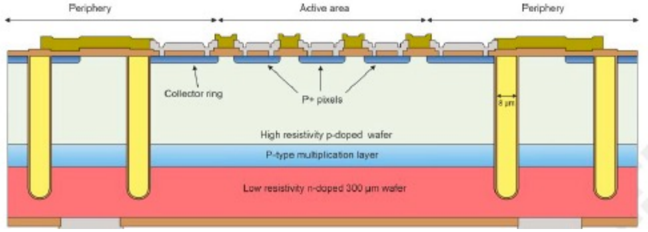
- LGADs with Trench-Isolated trenches (TI-LGAD)



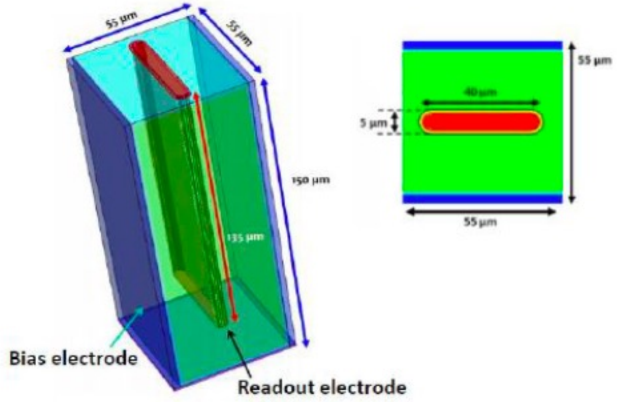
- Resistive AC-Coupled Silicon Detectors (RSD)
  - AC-pad coupled to the resistive n+ via dielectric coupling layer
  - Not segmented gain layer: 100% fill factor
  - Radiation hardness to be evaluated



- Inverse LGAD (iLGAD):
  - multiplication region on the opposite side of the read-out electrodes



3D pixels for timing



The idea is to use a 3D based on trenches instead of columns in order to obtain a more uniform electric/weighting field between electrodes → reduction of the dependence of timing on the impact position of particles

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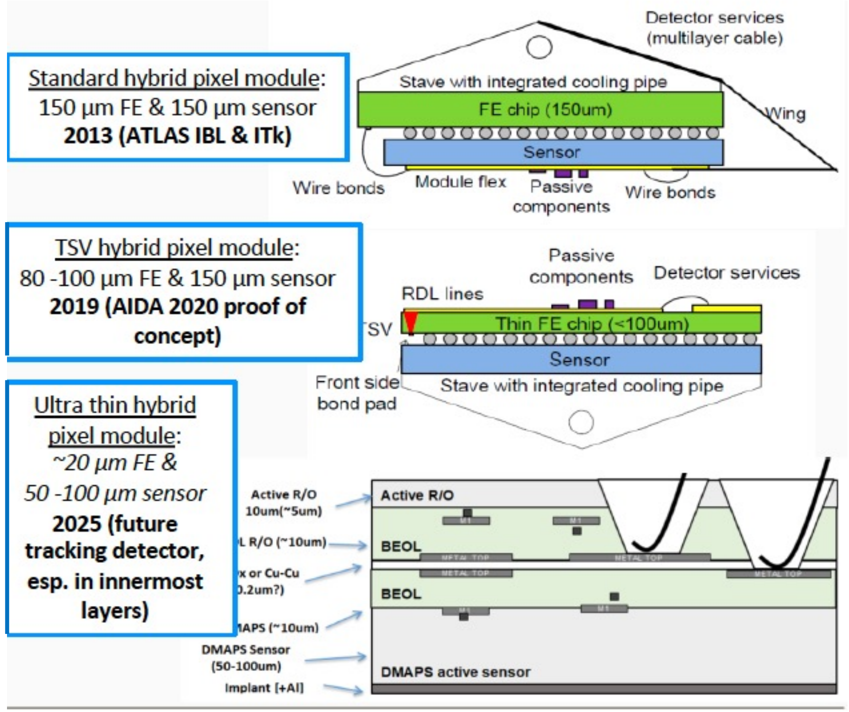
Interconnection technologies: wafer-to-wafer

Goal: reduce mass, i.e. thickness of pixel detectors as much as possible while keeping the benefits of the hybrid approach:

- Separate development and optimization of sensors and FE electronics allowing for best performance of FE electronic and sensor.
- Fine pitch interconnection between FE and sensor pixel with about 20 µm pitch.
- Thinning of FE and sensor parts to the minimum. Target is the development of ultra-thin hybrid pixel detectors based on:
  - 50 – 100 µm thick pixel sensor on 200 (300) mm CMOS wafers
  - ~20 µm thick pixel FE chip thickness on 200 (300) mm CMOS



Standard hybrid pixel module:
150 µm FE & 150 µm sensor
2013 (ATLAS IBL & ITk)

TSV hybrid pixel module:
80 -100 µm FE & 150 µm sensor
2019 (AIDA 2020 proof of concept)

Ultra thin hybrid pixel module:
~20 µm FE & 50 -100 µm sensor
2025 (future tracking detector, esp. in innermost layers)

Bonn Uni and IZM

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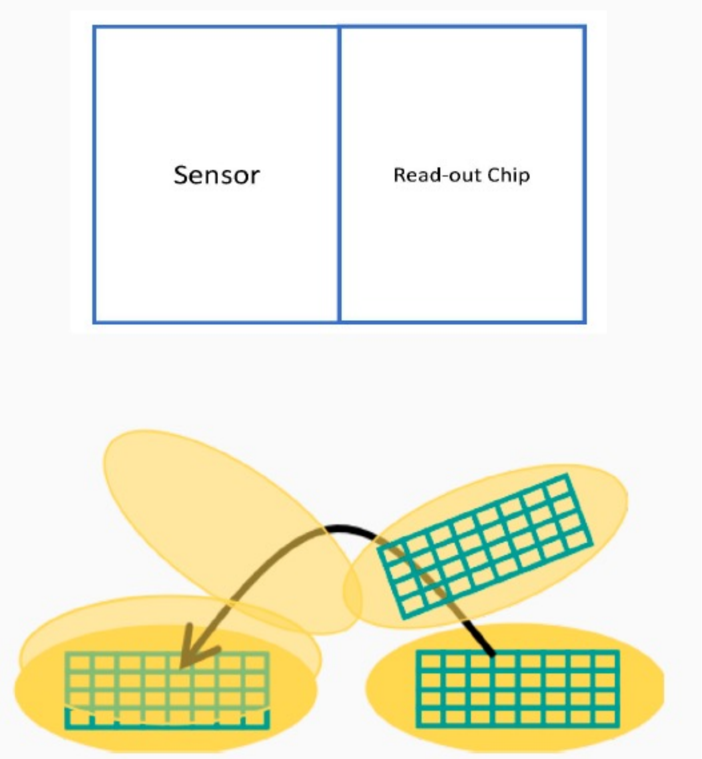
Wafer to wafer: Proof of concept for AIDAInnova

Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:

- Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from Lfoundry
- Use either TimePix3 chip wafers (130 nm on 200 mm wafers) or own FE development on the same wafer as the sensor
- Develop and optimize hybridization process including thinning and interconnection from chip's backside
- Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics (long term, not with AIDAinnova)



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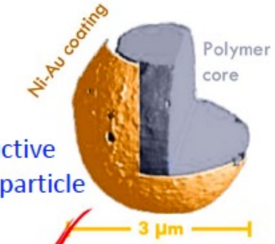
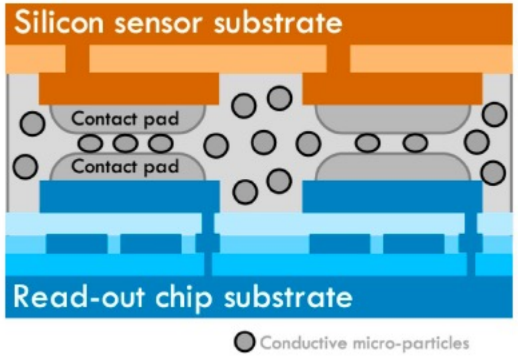
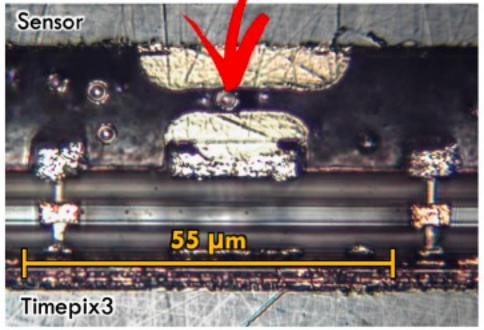
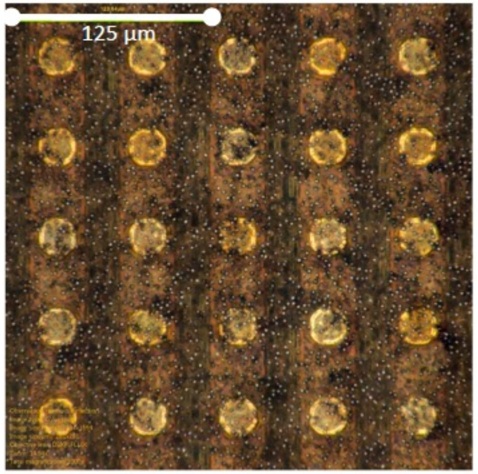
WP6: ACF for pixel detector hybridization

- Bump bonding in specialized industry is costly / complex
- Alternative process: Anisotropic Conductive Films (ACF)
  - Epoxy film for mechanical connection, embedded conductive particles for el. connection
  - Mask-less sensor/ASIC metallization: Electroless Nickel Gold (ENIG) deposition
  - In-house flip-chip process
  - Challenge: Optimization of ACF material and flip-chip process for fine pitch


Conductive micro particle


ACF interconnect scheme


Cross section Timepix3 ACF assembly


ACF on Timepix ASIC

Involved groups:
- CERN: Sample preparation (metallisation), flip-chip detector assembly, testing, process optimization
- Conpart: Industrial partner / ACF supplier, R&D on micro particles, ACF characterisation, process optimization
- CNRS-LPNHE: Sensor and test-structure procurement and production, testing
- Outside AidaInnova: DESY (test beam) and Geneva (Support for flip-chip infrastructure)

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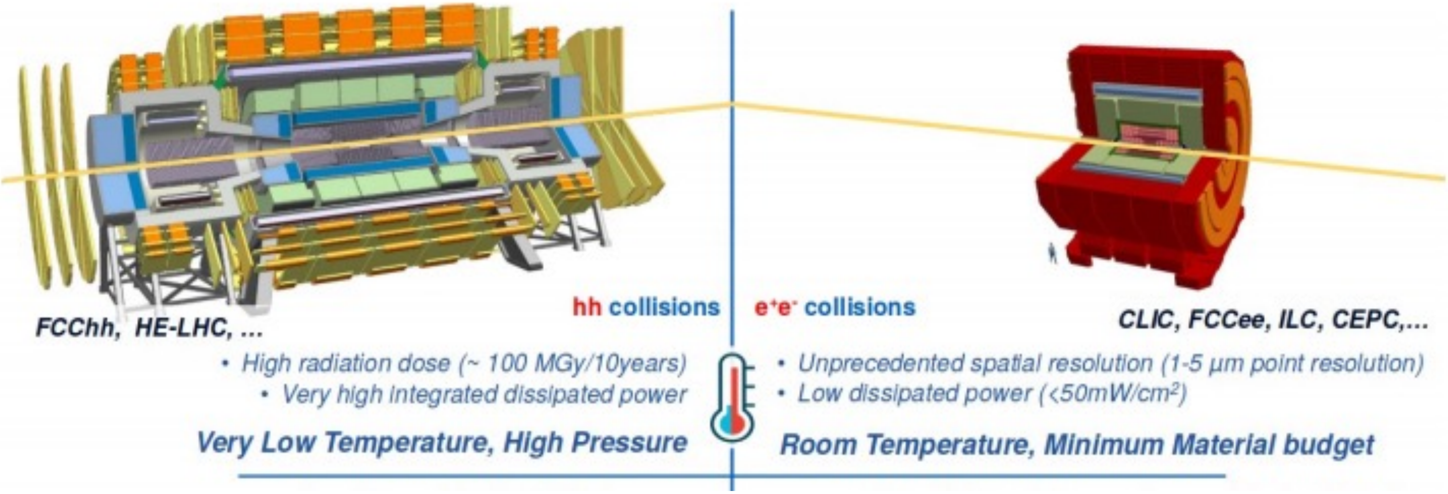
WP10: Advanced mechanics for tracking and vertex detectors

- Bring to maturity CMOS-compatible Si-μ-channel fab processes
- Exploit additive manufacturing for
  - Ultra-thin metal cooling devices
  - Ceramic (composites?) cooling devices
  - Hydraulic connections and interconnections
- Ultra light structures integrating cooling features
- New approach to (natural) refrigerant fluids for warm and cold applications
- Develop instrumentation for accurate absolute position measurements on very small devices



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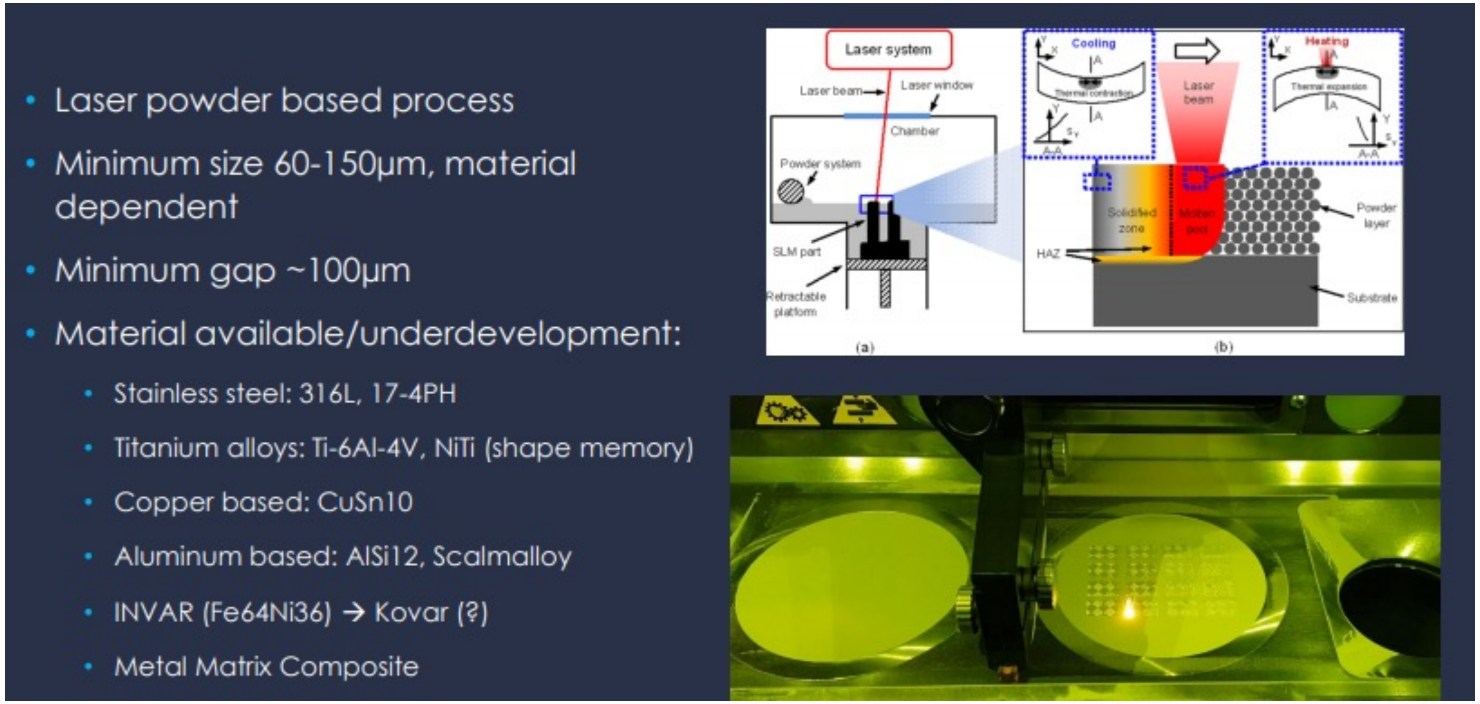
WP10:
Ultra light 3D printed cold plates @CSEM

- Additive Manufacturing technologies (“3D-printing”):
- standardised and reliable approaches to produce 3D-printed high precision micro-channel cold plates.
- Study Different metallic alloys and ceramic composites
- Investigate the minimum channel cross section attainable for a fixed channel length
- Guidelines toward engineering of the future advanced detector cooling solutions.

- Top Swiss RTO* with strong background (among others) in high precision manufacturing.
- Involved: Additive Manufacturing & Component Reliability group
- Specialist of metal printing



- Laser powder based process
- Minimum size 60-150µm, material dependent
- Minimum gap ~100µm
- Material available/underdevelopment:
  - Stainless steel: 316L, 17-4PH
  - Titanium alloys: Ti-6Al-4V, NiTi (shape memory)
  - Copper based: CuSn10
  - Aluminum based: AlSi12, Scalmalloy
  - INVAR (Fe64Ni36) → Kovar (?)
  - Metal Matrix Composite

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* Research and Technology organization

Additional material

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The AIDAinnova call

Another call in FP8 was not obvious

- Followed intensive discussions with EC, incl. actions by the CERN directorate

Targeted Call INFRAINNOV-04-2020: Innovation pilots

- Adressing advanced Integrated Activities (i.e. the AIDA-2020 community)
- which have reached a high level of integration and can focus on joint research: **collaborative**

Objectives

- Support research **infrastructure** networks developing and implementing a **common strategy/roadmap** including technological development required for improving their services through **partnership with industry**
- Support **incremental innovation** and cooperation with industry

Complementarity to ATTRACT (competitive, disruptive)

Increased focus on industrial partners

No Transnational Access

infrastructure: common interest

Proposed funding 10 M€ for 4 years

Felix Sefkow | April 2021

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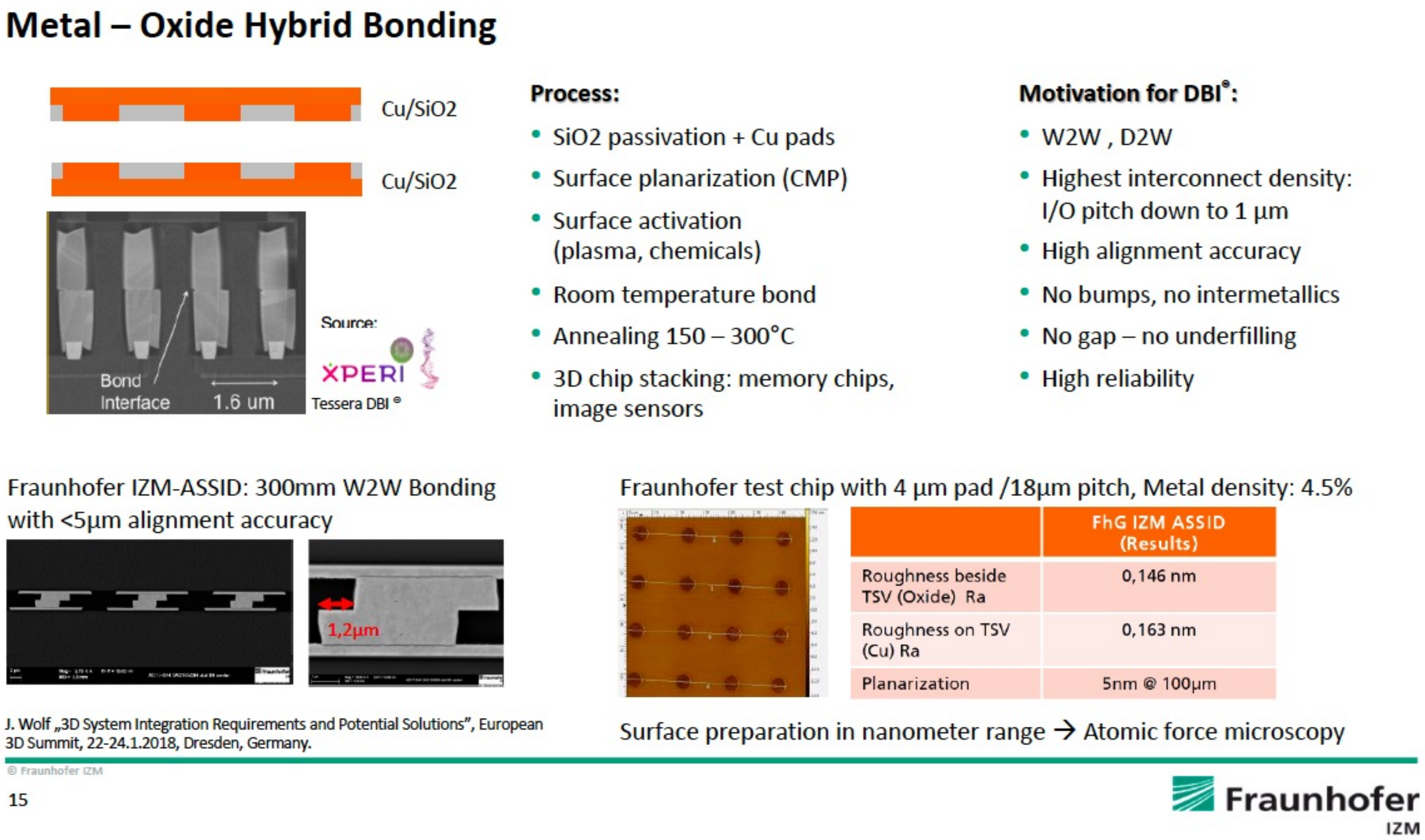
WP6: Interconnection technologies



Metal – Oxide Hybrid Bonding

Process:

- SiO2 passivation + Cu pads
- Surface planarization (CMP)
- Surface activation (plasma, chemicals)
- Room temperature bond
- Annealing 150 – 300°C
- 3D chip stacking: memory chips, image sensors

Motivation for DBI®:

- W2W , D2W
- Highest interconnect density: I/O pitch down to 1 µm
- High alignment accuracy
- No bumps, no intermetallics
- No gap – no underfilling
- High reliability

Fraunhofer IZM-ASSID: 300mm W2W Bonding with <5µm alignment accuracy

J. Wolf „3D System Integration Requirements and Potential Solutions", European 3D Summit, 22-24.1.2018, Dresden, Germany.

Fraunhofer test chip with 4 µm pad /18µm pitch, Metal density: 4.5%

	FhG IZM ASSID (Results)
Roughness beside TSV (Oxide) Ra	0,146 nm
Roughness on TSV (Cu) Ra	0,163 nm
Planarization	5nm @ 100µm

Surface preparation in nanometer range → Atomic force microscopy

© Fraunhofer IZM

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