Monolithic silicon pixel detectors for timing

Giuseppe Iacobucci
Université de Genève

Silicon detectors at UNIGE

- Long tradition at UNIGE with hybrid silicon detectors:
  - strip detectors (ATLAS-SCT, AMS, DAMPE)
  - pixel detectors (ATLAS-IBL)

- Since 2013, we started a research on novel pixel sensors
  - first on CCPD and then on monolithic pixel sensors for ATLAS HL-LHC upgrade

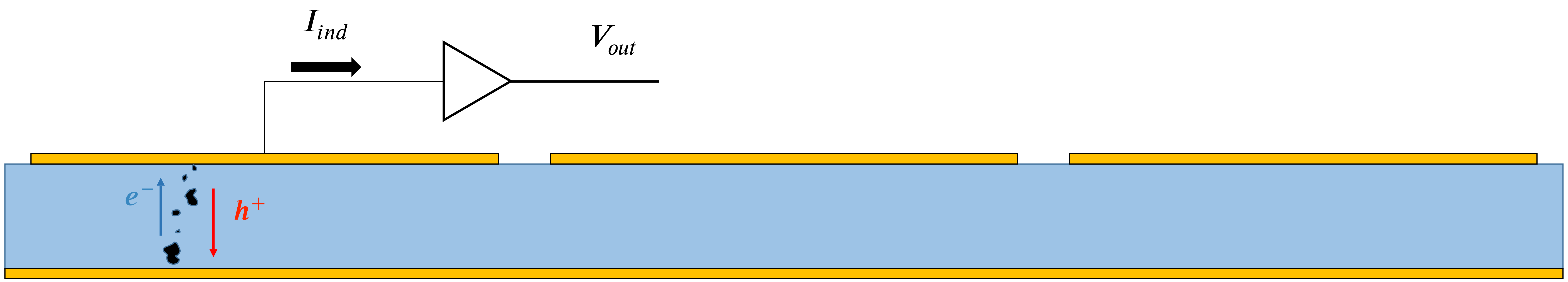
- More recently we launched an R&D on monolithic pixel sensors in SiGe BiCMOS technology for timing purposes, for experiments and applications.

  AIM: develop **monolithic** sensor with **time resolution** below 100ps

Time resolution of silicon pixel sensors: our rationale

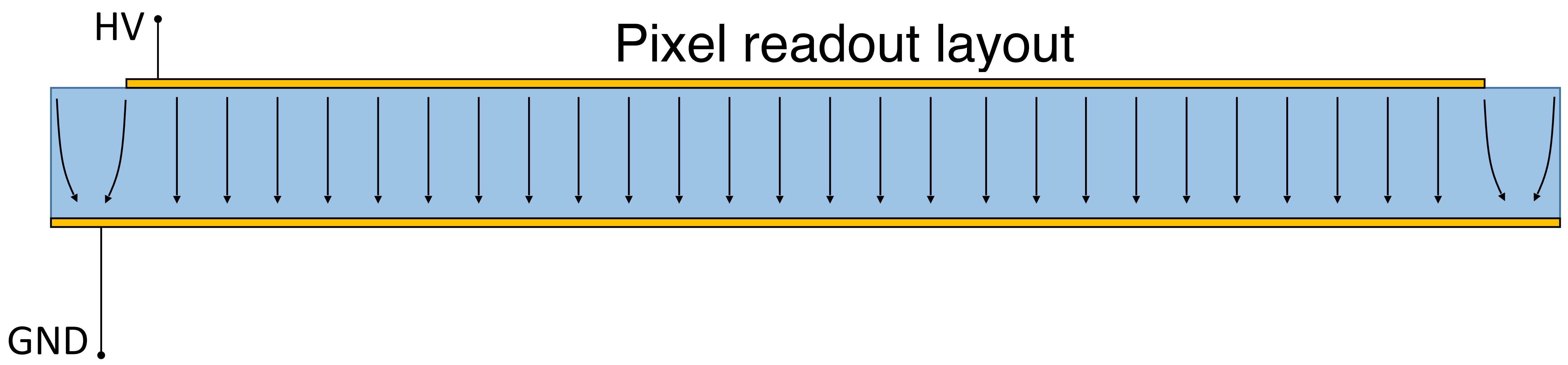
Main parameters that control the time resolution of semiconductor detectors:

1. Geometry & fields
2. Charge collection (Landau) noise
3. Electronics noise



1. Geometry and fields

Sensor optimization for time measurement means that:
the **sensor time response** must be **independent of the particle trajectory**

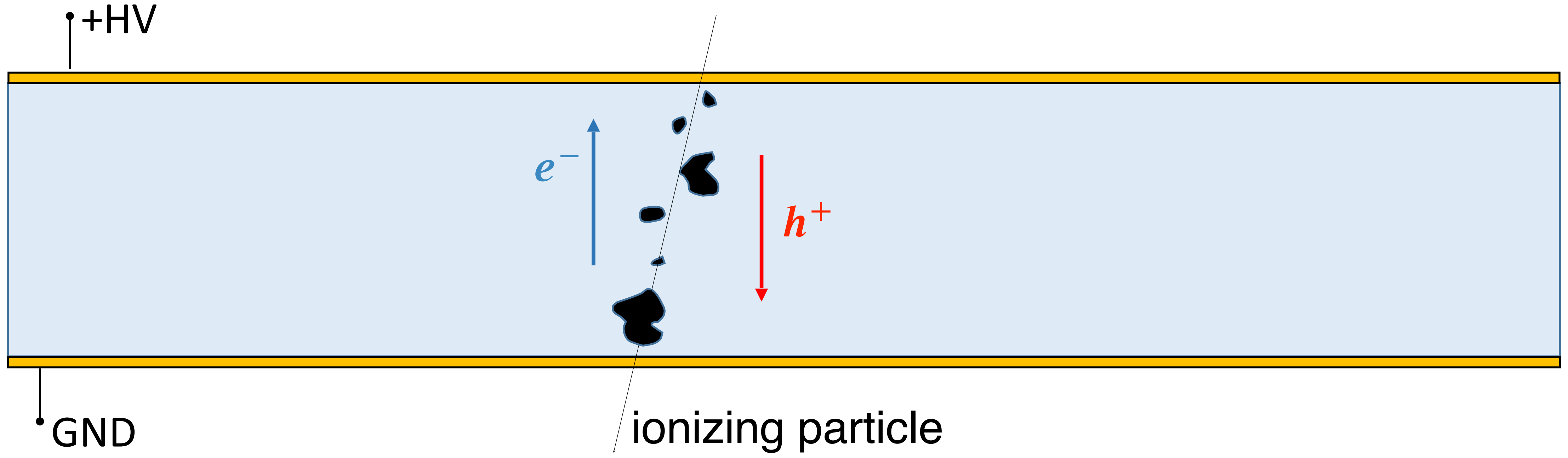


Wide pixel w.r.t. depletion depth: **“parallel plate”** read out

Desired features:

- **Uniform** electric field (charge transport)
- **Uniform** Ramo field (signal induction)
- **Saturated** charge drift velocity

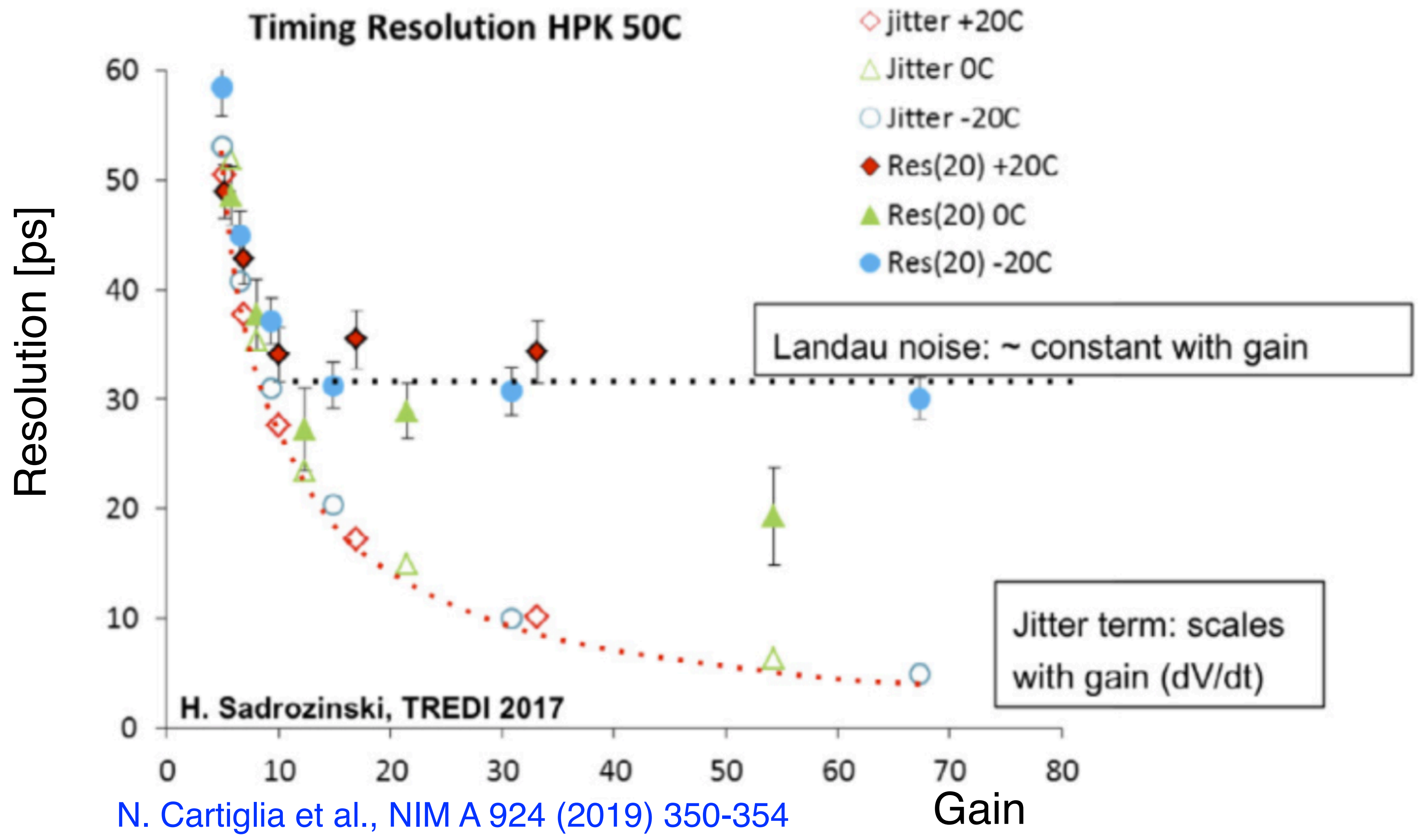
2. Charge-collection (Landau) noise



The charge-collection noise is produced by **Landau fluctuations** of charge deposition in the sensor:

$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

Large charge clusters produce large fluctuations of the induced current.
The **statistical origin** of this variability of I_{ind} makes this effect irreducible in PN-junction sensors.

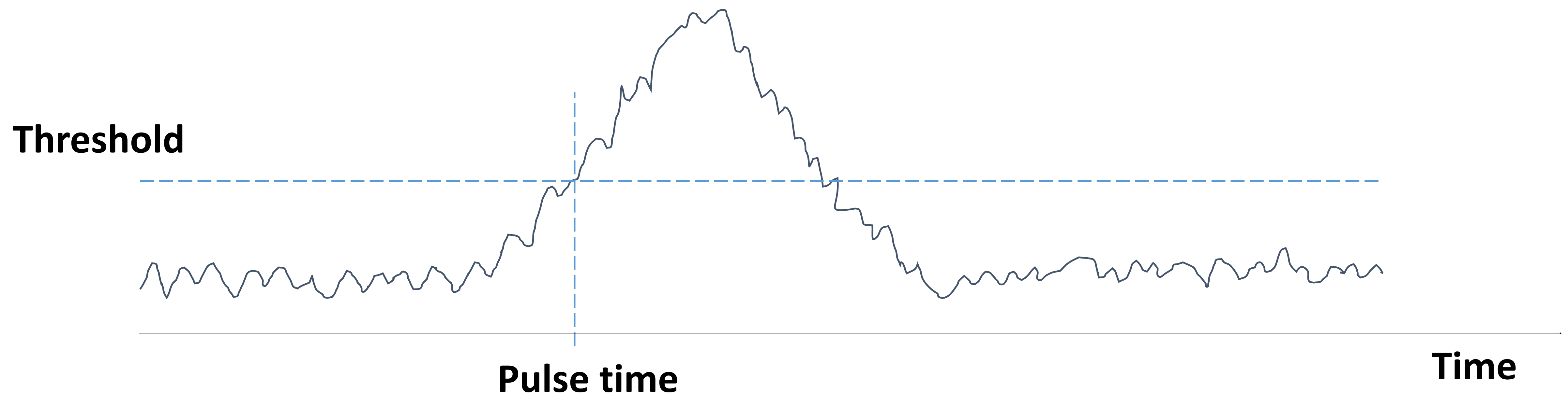


N. Cartiglia et al., NIM A 924 (2019) 350-354

To minimise this effect, we developed and patented a **novel multi PN-junction sensor**: the **picoAD** (Picosecond Avalanche Detector).

3. Electronic noise

Once the geometry has been fixed, the time resolution depends mostly on the amplifier performance.



$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} = \frac{A_{Gain} \cdot ENC}{A_{Gain} \cdot I_{ind}} \cong \frac{t_{rise}}{\frac{Q}{ENC}} = \frac{t_{rise}}{Signal/_{Noise}}$$

Need an ultra-fast, low noise (and low power) electronics with fast rise time and small capacitance.

Our solution:

SiGe HBT technology $\Longrightarrow$ high f_T, single transistor preamplifier

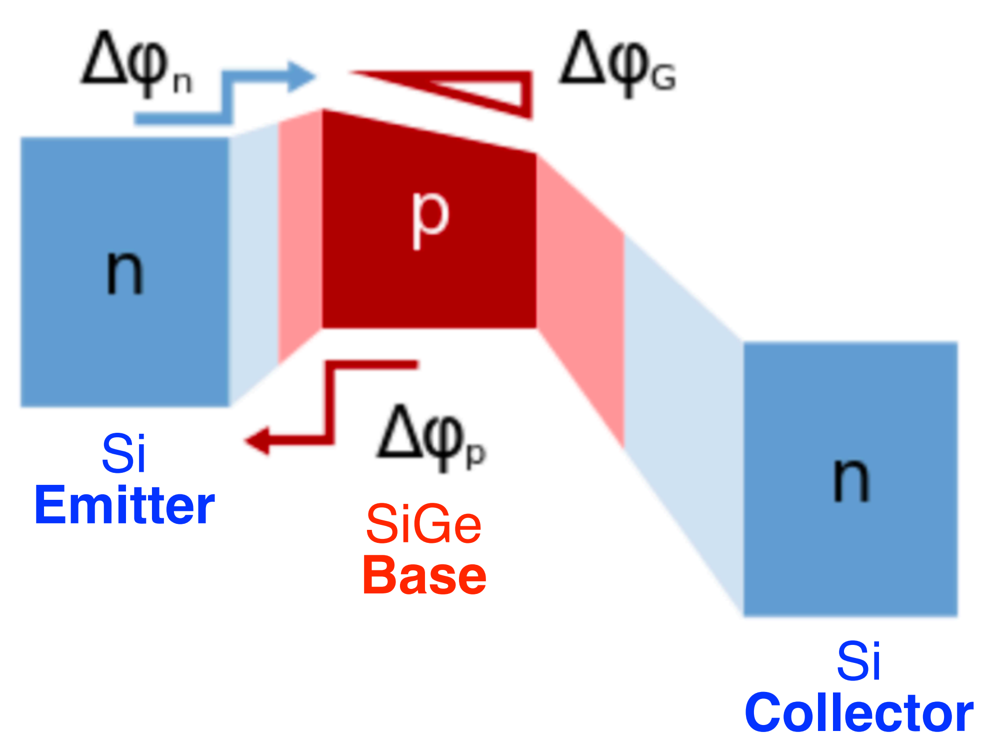
↳ ~1 ns rise time, < 90 e^- ENC on ~70 fF capacitance

SiGe HBT transistors for low-noise, fast amplifiers

In **SiGe Heterojunction Bipolar Transistors** (HBT) the **grading** of the bandgap in the Base changes the **charge-transport mechanism** in the Base **from diffusion to drift**:

NPN SiGe HBT

(depleted regions in light colors)
from wikimedia



Heterojunction:

High doping density in the Base

$\Longrightarrow$ thinner Base $\Longrightarrow$ reduction of base resistance R_b

Grading of germanium in the base:

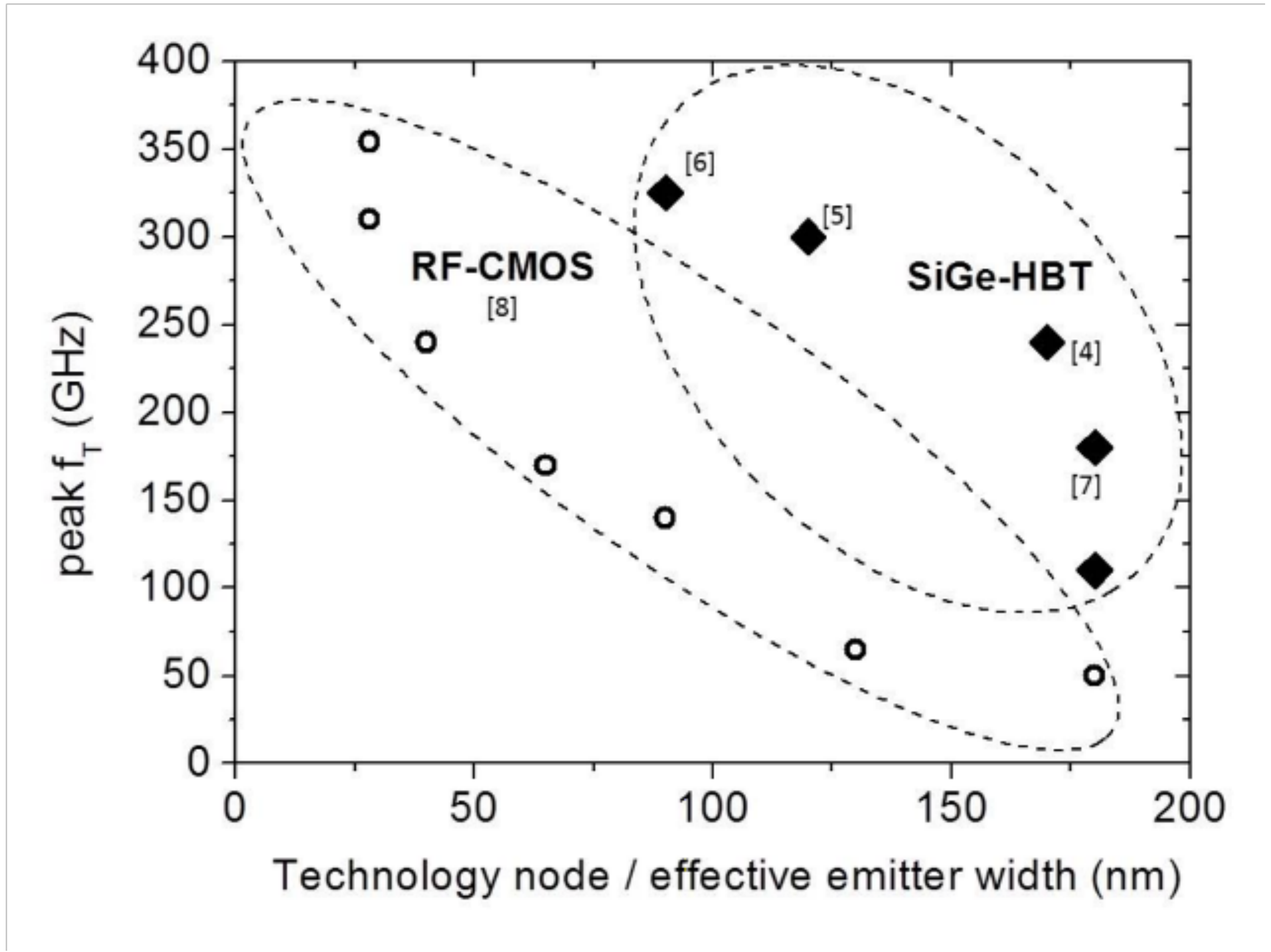
field-assisted charge transport in the Base,
equivalent to introducing an electric field in the Base
$\Longrightarrow$ short e^- transit time in Base $\Longrightarrow$ very high β

High f_T and high β SiGe HBT allows for amplifiers with:

- ➡ **Low series noise**
- ➡ **Fast pulse integration**
- ➡ **High gain**
- ➡ **Very low-power consumption**

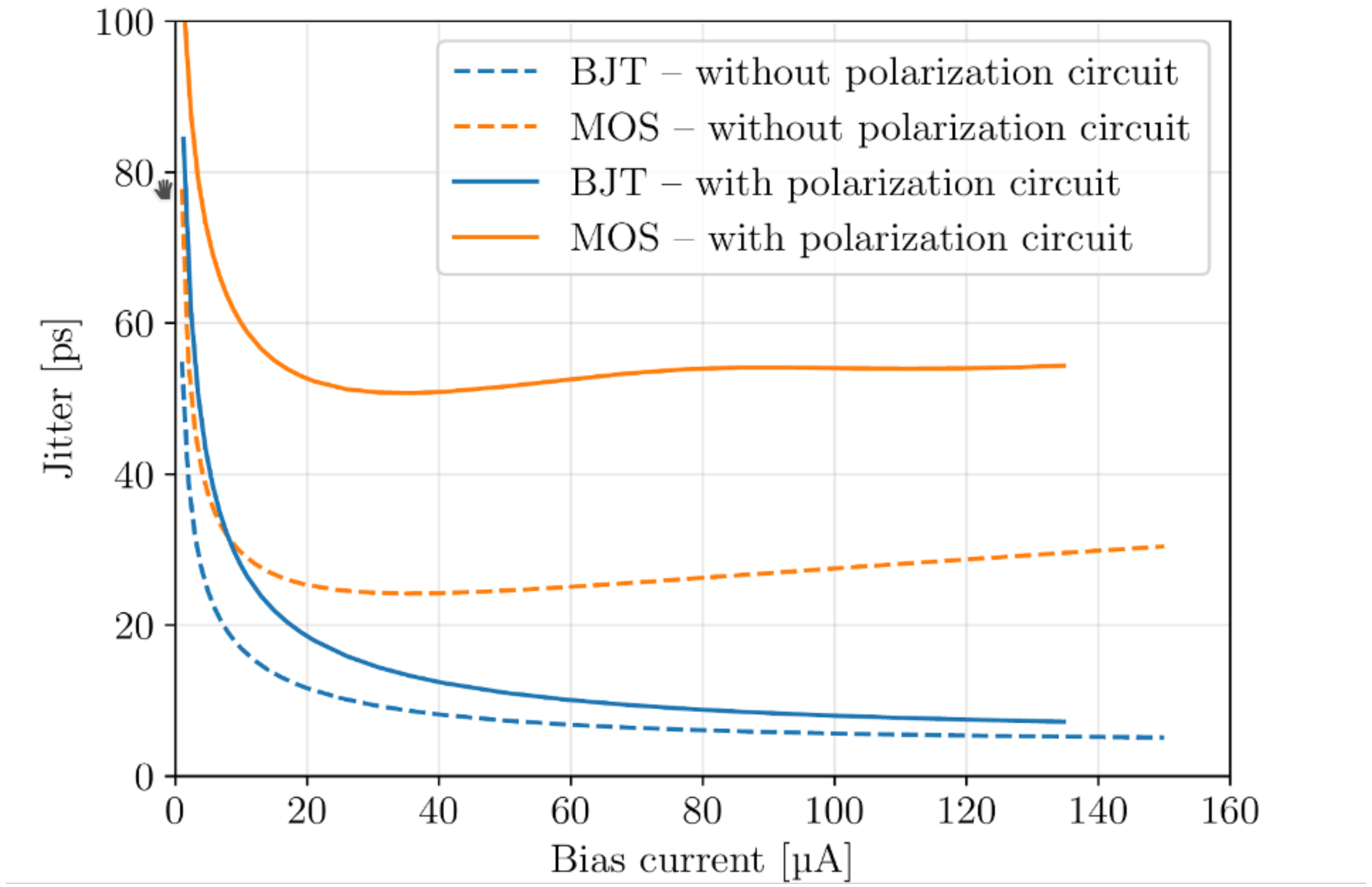
SiGe HBT vs. CMOS

Peak transition frequency vs. technology node



A. Mai and M. Kaynak,
SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

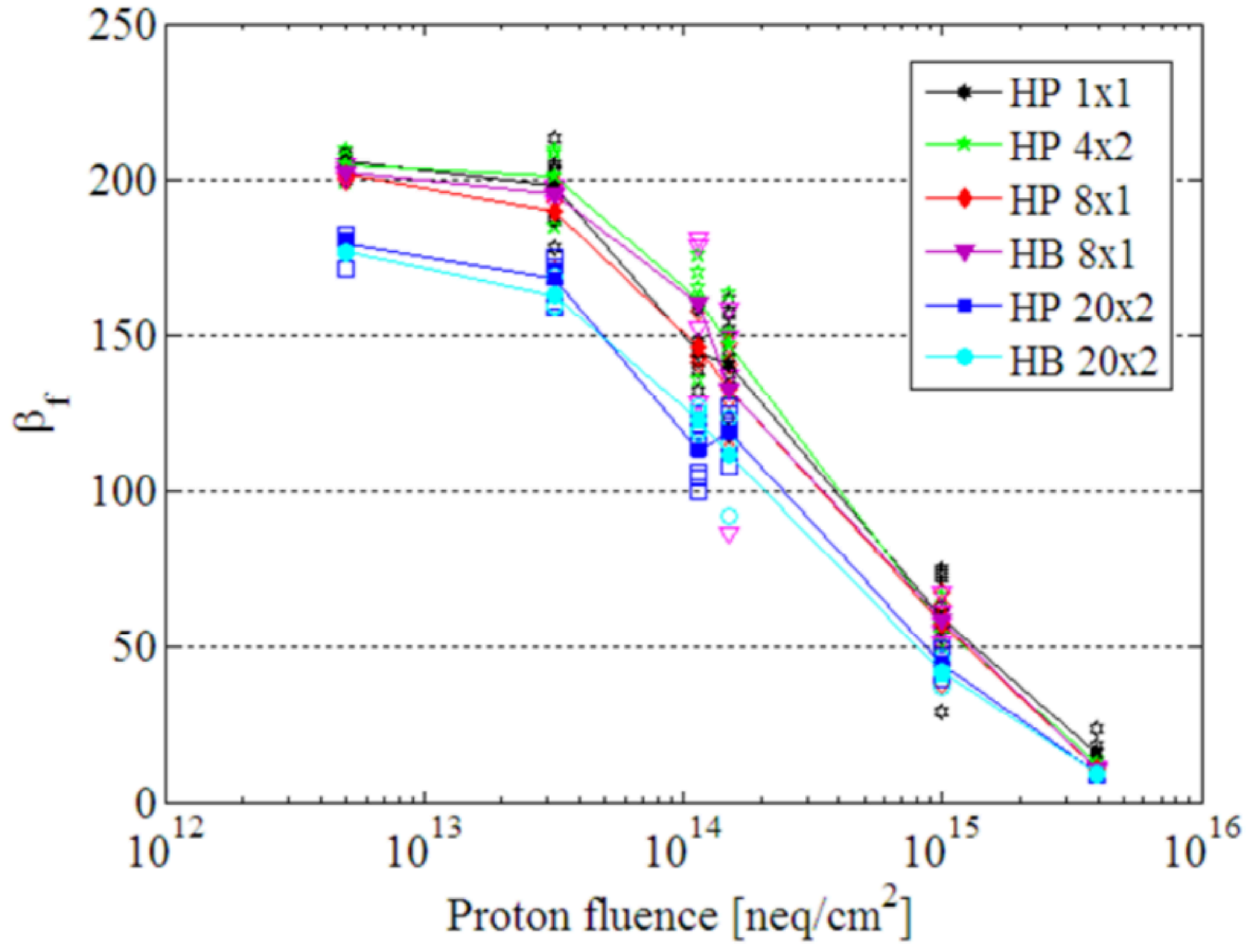
Intrinsic **amplifier jitter**:
common emitter (source) configuration
in a 130nm technology



L. Paolozzi et al.,
Time resolution and power consumption of a monolithic silicon pixel prototype in SiGe BiCMOS technology,
JINST 15 (2020) P11025, https://doi.org/10.1088/1748-0221/15/11/P11025

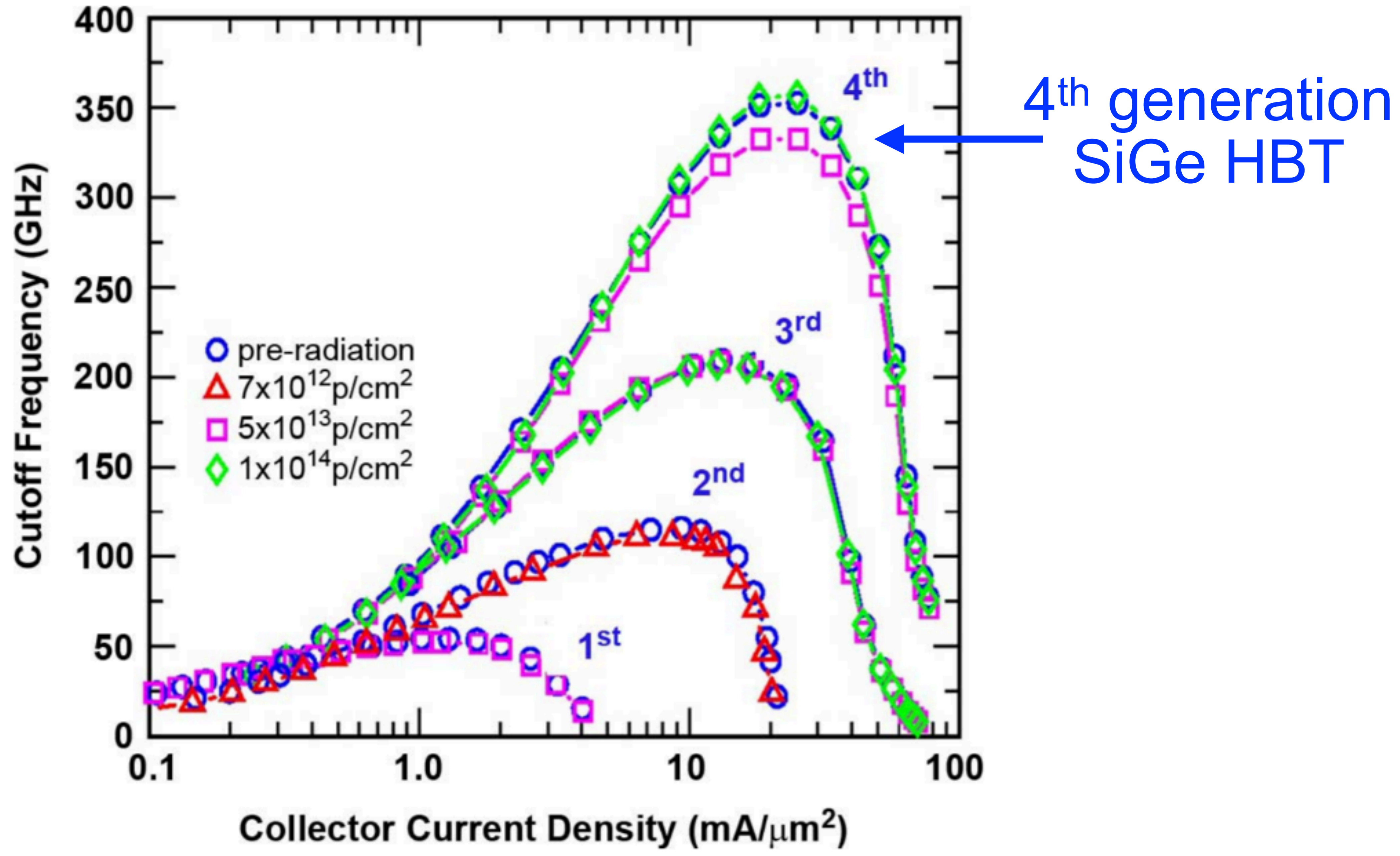
Radiation hardness of standard commercial HBTs

DC characteristics



S. Díez et al, IEEE Nuclear Science Symposium & Medical Imaging Conference, Knoxville, TN, 2010, pp. 587-593, doi: 10.1109/NSSMIC.2010.5873828.

AC characteristics



From: J.D. Cressler, IEEE transactions on nuclear science, vol. 60, n. 3 (2013)

SiGe BJT is **inherently radiation hard** up to **10^{14} n_{eq}/cm^2**,

well above the **FCCee** yearly integrated doses.

SiGe BiCMOS markets served


Optical fiber networks


Smartphones


IoT Devices


Microwave Communication


Automotive: LiDAR, Radar and Ethernet


HDD preamplifiers, line drivers, Ultra-high speed DAC/ADCS

source: https://towerjazz.com/technology/rf-and-hpa/sige-bicmos-platform/

Several large-volume foundries offer SiGe processes: TJ, TSMC, ST, AMS, GF, …

as well as research institutes: like **IHP**

Fast growing technology: f_{max} = 0.7 THz transistor recently developed (**H2020 DOT7 project** by **IHP**)

Technology choice: IHP 130nm SiGe process

Exploit the properties of state-of-the-art SiGe Bi-CMOS transistors :

Leading-edge technology: **IHP SG13G2**

130 nm process featuring **SiGe HBT** with

- Transistor transition frequency: f_T **= 0.3 THz**
- Current gain: β **= 900**
- Delay gate: **1.8 ps**

innovations for high performance microelectronics

Leibniz-Institut für innovative Mikroelektronik

In this IHP process **we produced**:

1) an ultra-fast, low-noise **amplifier** with low-power consumption (**60 μW/ch** to obtain **$\sigma_t \sim$ 50 ps**, and **4 μW/ch** for **$\sigma_t \sim$ 200 ps**)

2) a **TDC** that, with a simple architecture, provides a time resolution of **1.6 ps** at a power consumption of **~4 mW/ch**

R&D at UNIGE

Articles:

Small-area pixels power consumption: JINST 15 (2020) P11025, https://doi.org/10.1088/1748-0221/15/11/P11025
Hexagonal small-area pixels: JINST 14 (2019) P11008, https://doi.org/10.1088/1748-0221/14/11/P11008
TT-PET demonstrator chip testbeam: JINST 14 (2019) P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
TT-PET demonstrator chip design: JINST 14 (2019) P07013, https://doi.org/10.1088/1748-0221/14/07/P07013
First TT-PET prototype: JINST 13 (2017) P02015, https://doi.org/10.1088/1748-0221/13/04/P04015
Proof-of-concept amplifier: JINST 11 (2016) P03011, https://doi.org/10.1088/1748-0221/11/03/P03011

Patents:

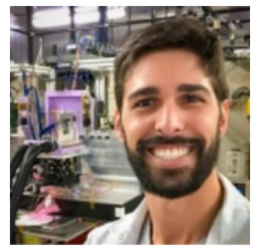
PLL-less TDC & synchronization System: EU Patent EP18181123.3
Picosecond Avalanche Detector (PicoAD): EU Patent EP18207008.6

Silicon Team at UNIGE

Giuseppe Iacobucci
- project P.I.
- System design

Didier Ferrere
- System integration
- Laboratory test

Pierpaolo Valerio
- Lead chip design
- Digital electronics



Mateus Vicente
- System integration
- Laboratory test

Yana Gurimskaya
- Radiation tolerance
- Laboratory test

Yannick Favre
- Board design
- RO system

Théo Moretti
- Laboratory test

Antonio Picardi
- Chip design

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Sergio Gonzalez-Sevilla
- System integration
- Laboratory test

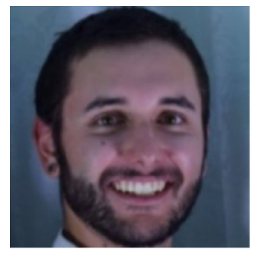
Magdalena Munker
- Sensor design
- Laboratory test

Roberto Cardella
- Sensor design
- Laboratory test

Fulvio Martinelli
- Chip design

Stéphane Débieux
- Board design
- RO system

Chiara Magliocca
- Laboratory test



Matteo Milanesio
- Laboratory test

Main research partners:

Roberto Cardarelli
INFN Rome Tor Vergata

Marzio Nessi
CERN & UNIGE

Ivan Peric
KIT

Holger Rücker
IHP Mikroelektronik

Mehmet Kaynak
IHP Mikroelektronik

Bernd Heinemann
IHP Mikroelektronik

Funded by:

FNSNF Swiss National Science Foundation

European Research Council
Established by the European Commission

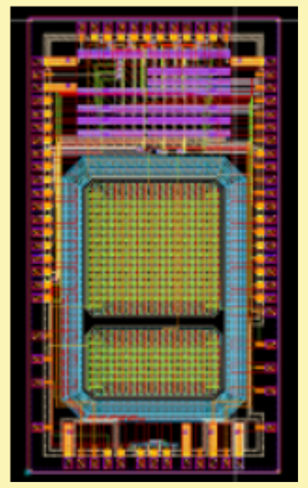
FNSNF Sinergia

ATTRACT

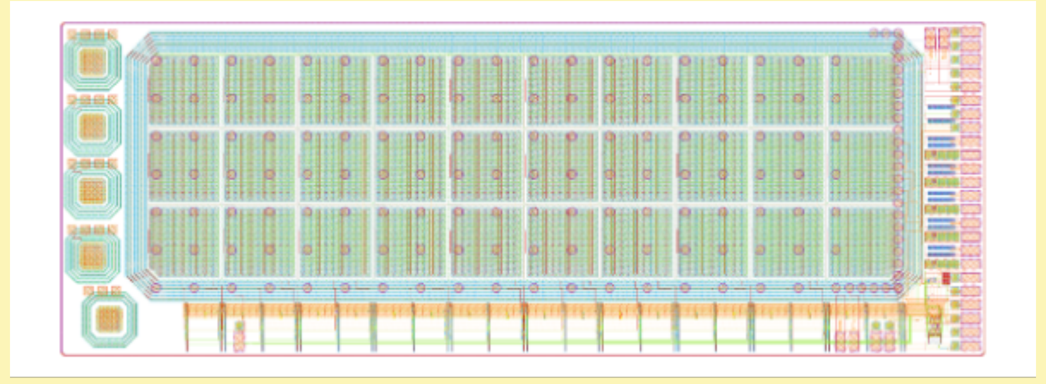
UNIVERSITÉ DE GENÈVE UNITEC

Prototypes produced in SiGe BiCMOS technology by UNIGE

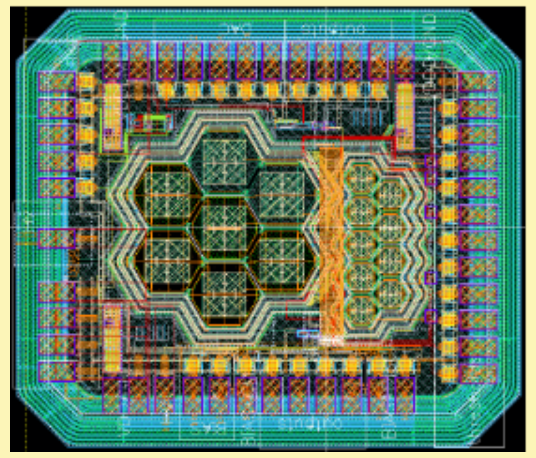
2016



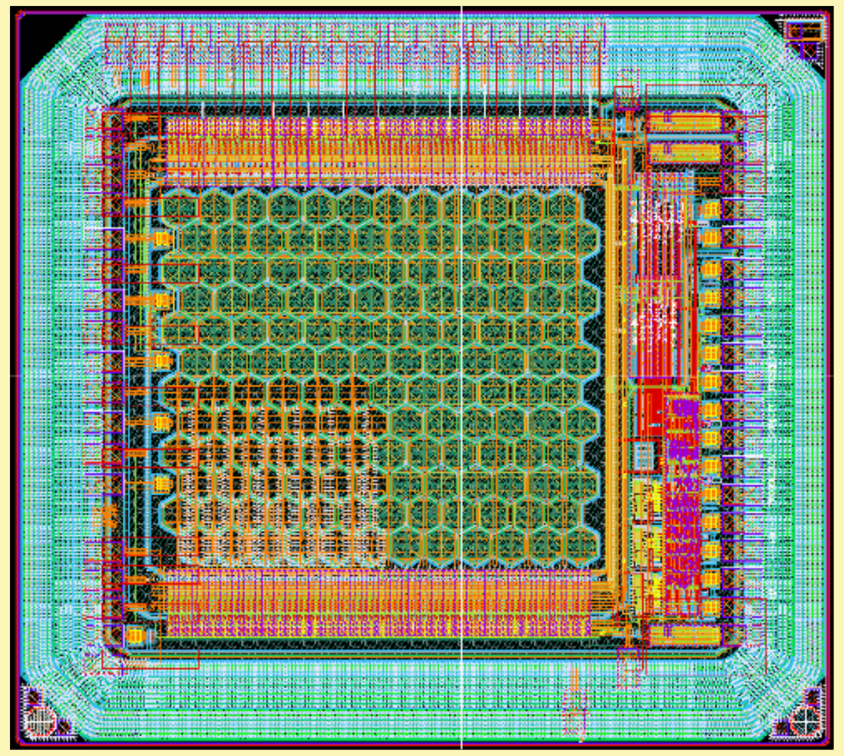
2017



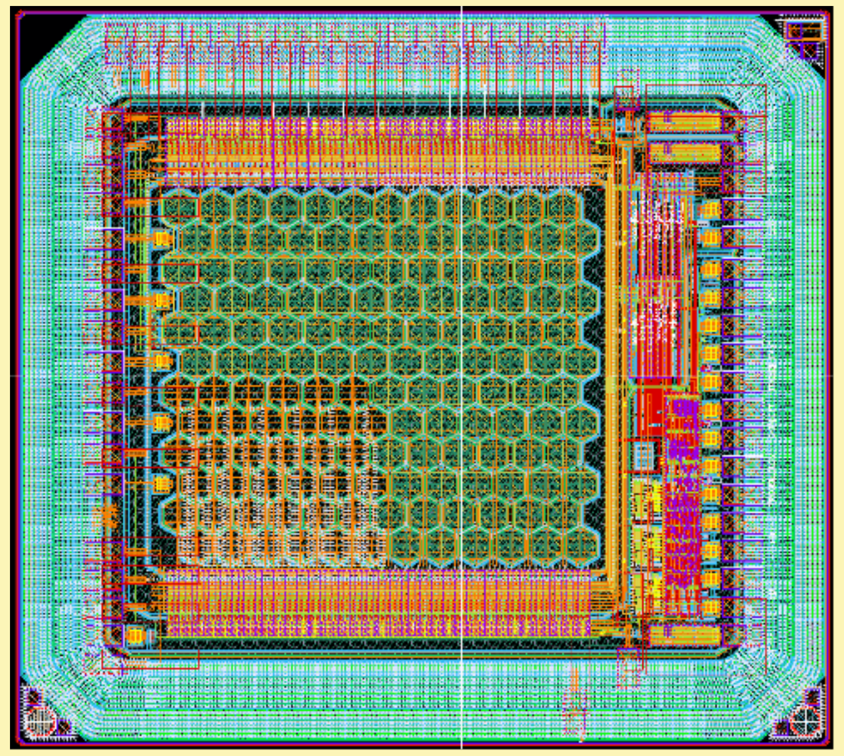
2018



2019



2021



Monolithic prototype ASICs for timing purposes

200ps
- 1 and 0.5 mm^2 pixels
- Discriminator output

110ps
- 30 pixels 500x500μm^2
- 100ps TDC +I/O logic

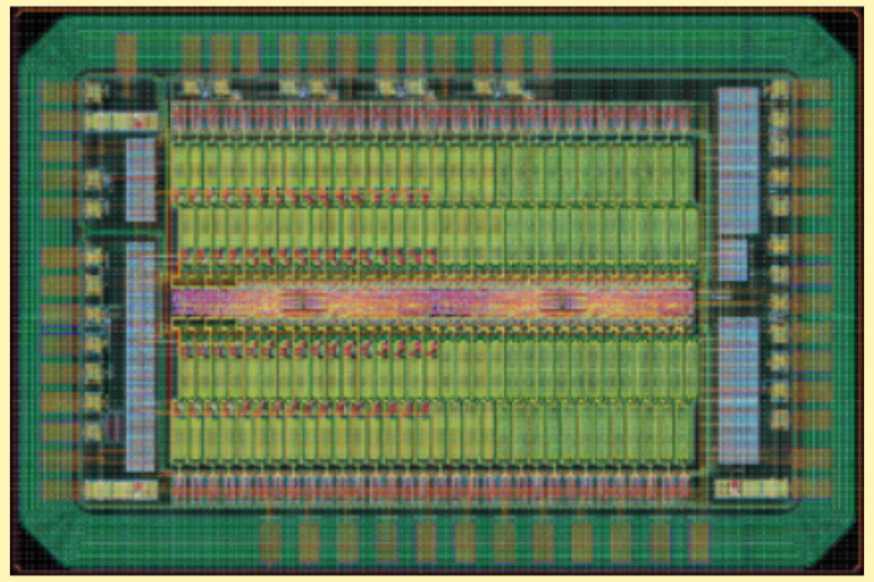
50ps
- Hexagonal pixels 65μm and 130μm side
- Discriminator output

$\lesssim$ 40 ps
- Hexagonal pixels 65μm side
- 30ps TDC +I/O logic
- Analog channels

PicoAD prototype
- epitaxial layers + **gain layer**
- expected: ~10ps

Other ASICs produced:

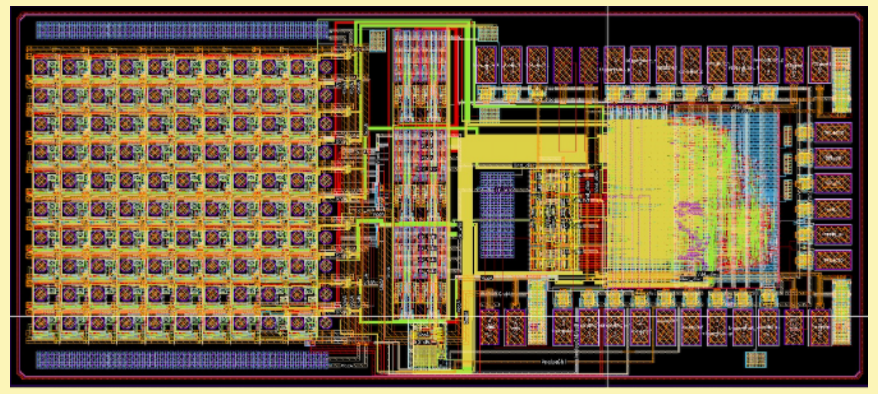
FASER pre-shower prototype



Time resolution 100ps — low power (40μW/ch)
Very large pixel dynamic range: 0.2 — 50 fC

Electronics-only

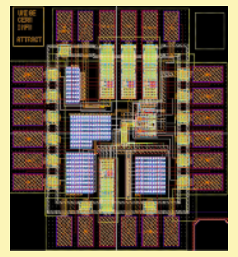
10 by 10 pixel matrix (100 μm pitch)
to be hybridised with different sensors



Highly unable frontend
50ps TDC channels
+ experimental 1ps channel

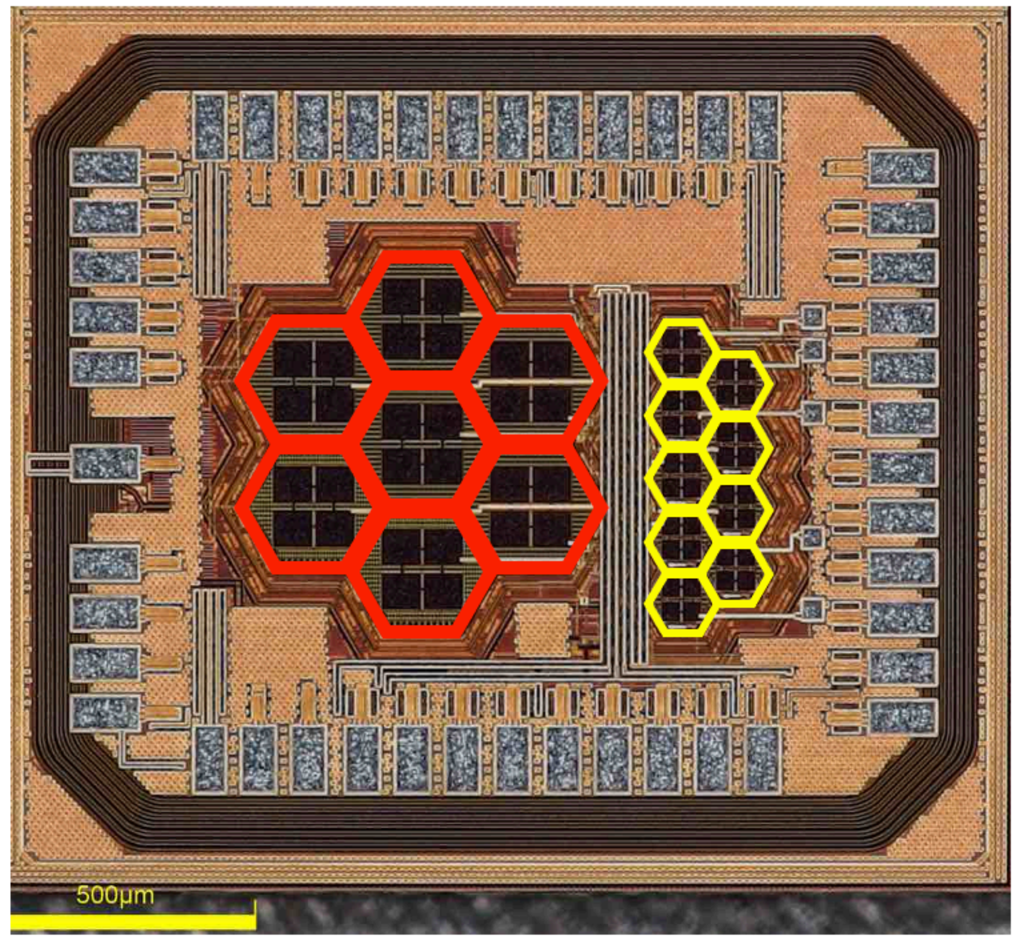
Picosecond TDC

Proof of concept.
Novel Time-to-Amplitude design
for ps accuracy

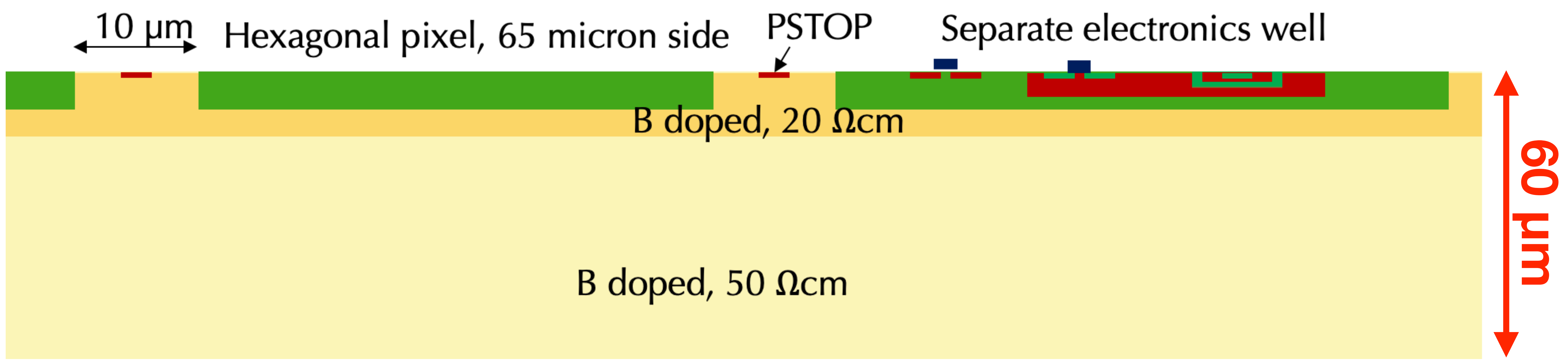


Compact, low-power,
high dynamic range

The 2018 prototype



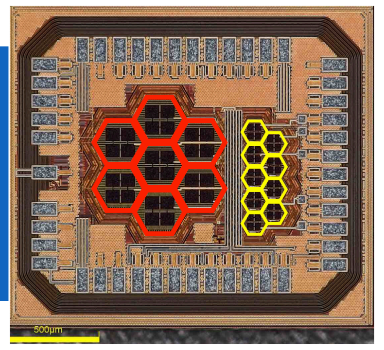
- Matrices with pixels of two sizes.
  The smaller-area pixels have:
  - Hexagon sides: 65µm (pitch ~100µm)
  - Total capacitance: 70 fF
  - Equivalent Noise Charge: 90 e^-
- Discriminator output
- New **dedicated custom components** developed with the IHP foundry



- Negative HV applied to substrate from backside and from top
- All pixels and electronics nwells at positive low voltage
- Bias voltage of -140V provides a **depletion layer of 26 µm**
  - with typical signal charge for a MIP: **~1600 electrons**

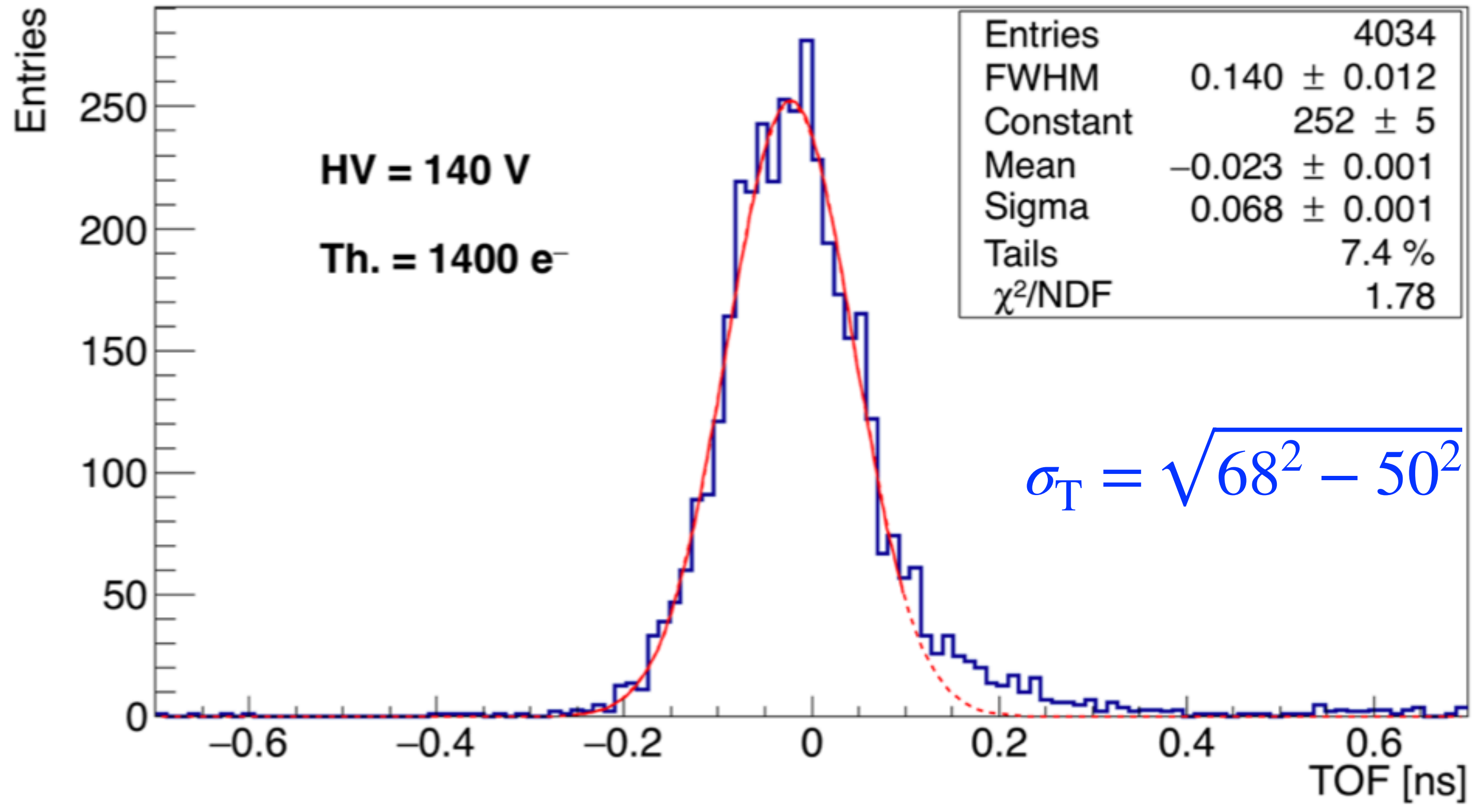
Note that this sensor was **thinned to 60 µm,** including the electronics

The 2018 prototype



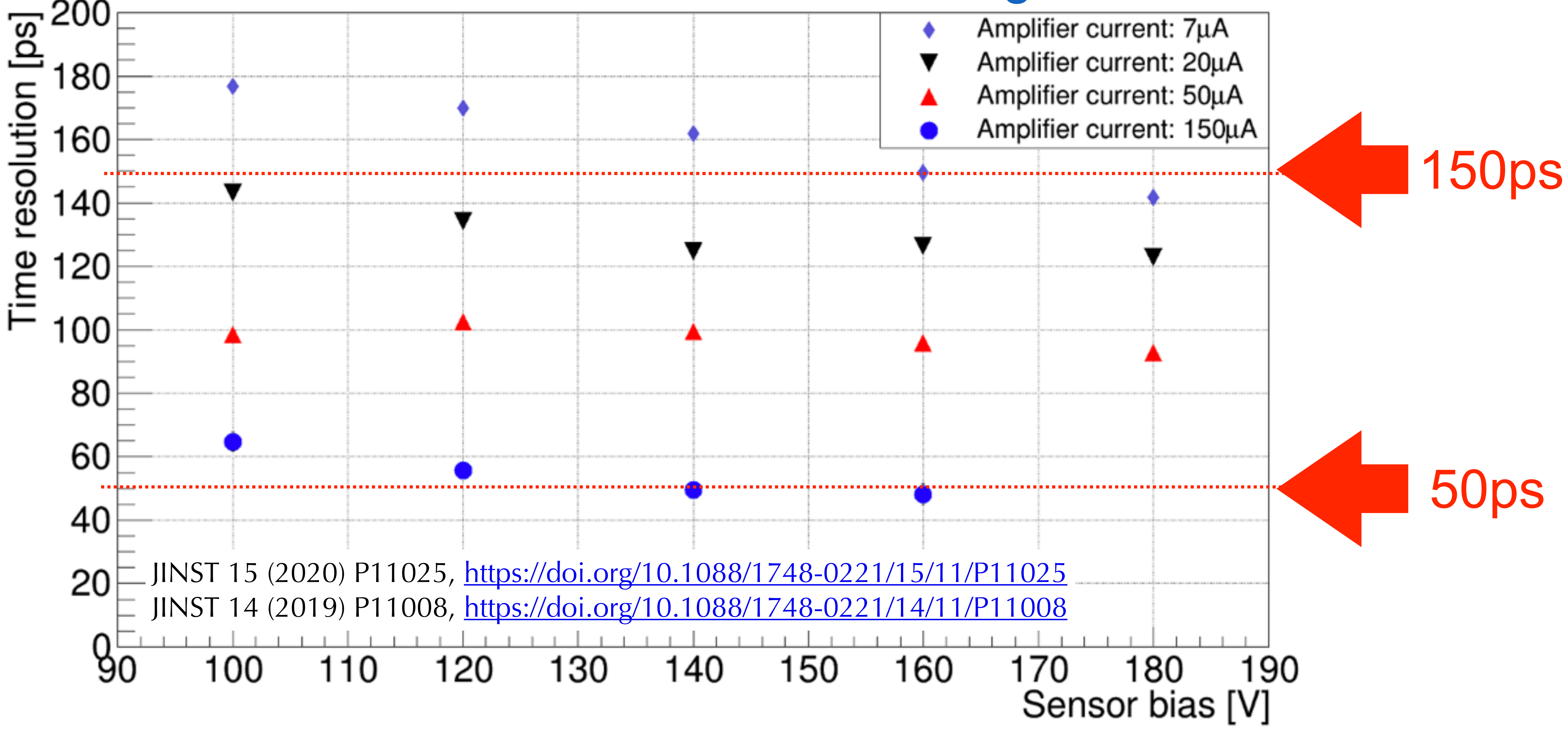
Data taken with ^{90}**Sr source**

TOF between our sensor and an LGAD



$$\sigma_T = \sqrt{68^2 - 50^2} = 46 \text{ ps}$$

Time resolution vs. bias voltage



Excellent results: **50 ps time resolution** at high power consumption

The 150 ps achieved at ~20 times smaller power consumption allows **a series of new applications**. See below.

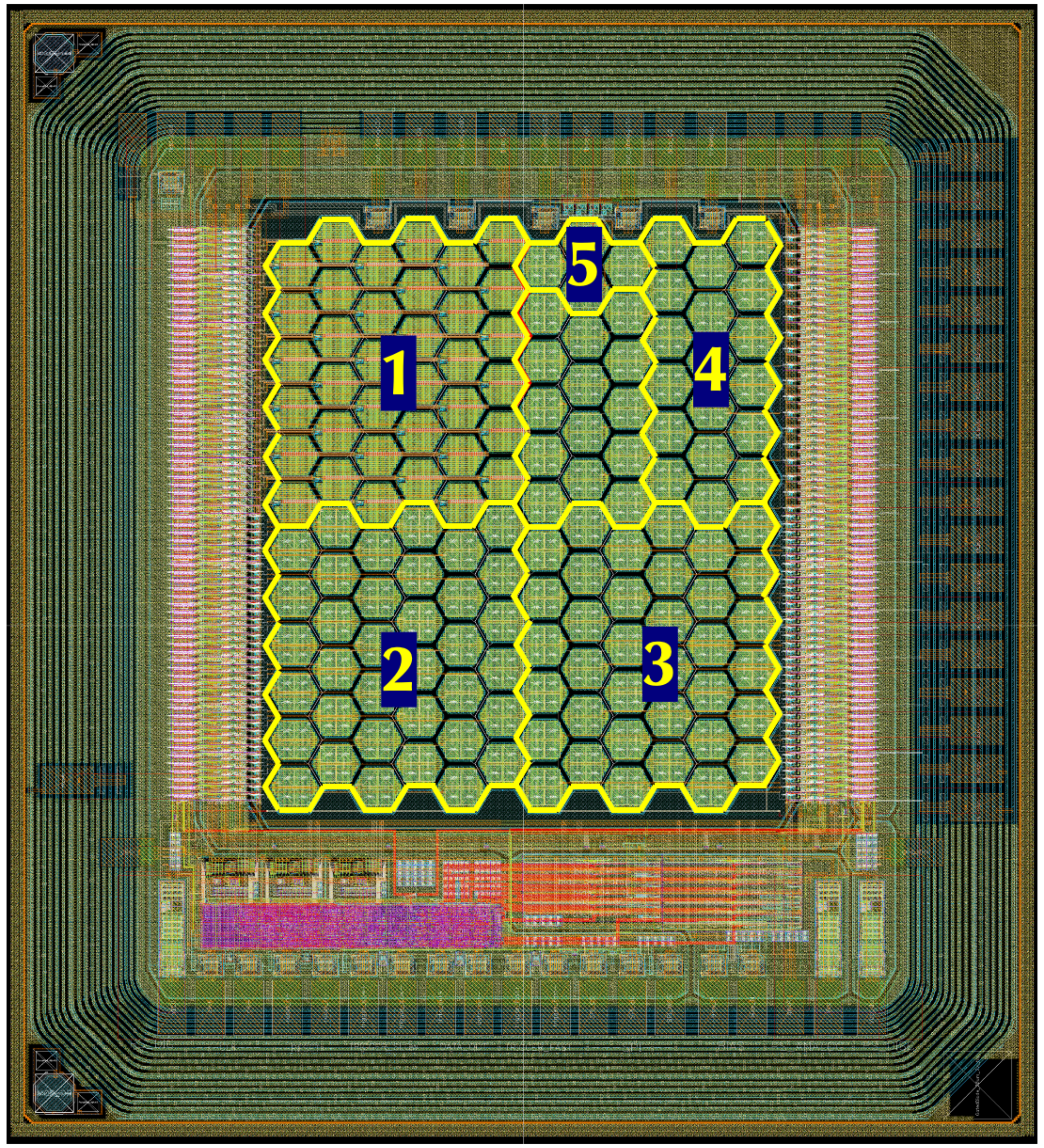
Note that: for this chip the performance was **limited by time-walk correction** (done with TOT)

The “ATTRACT” prototype

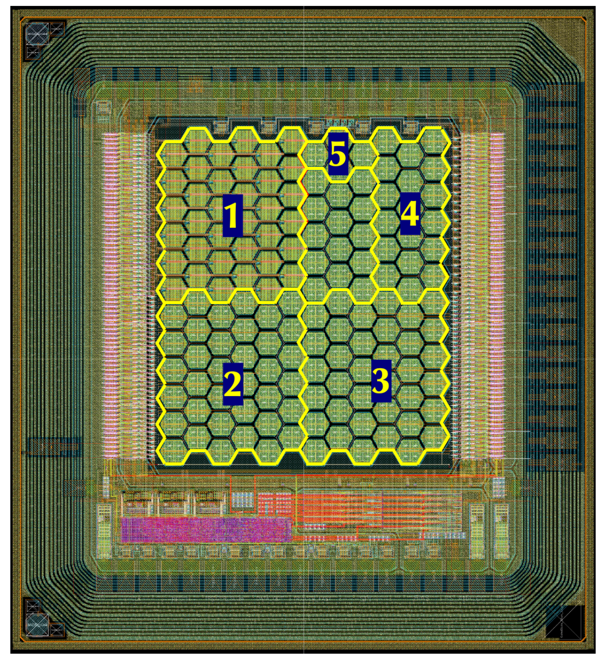
2019 MPW submission funded by H2020 ATTRACT MonPicoAD project

Five different matrices of pixels:

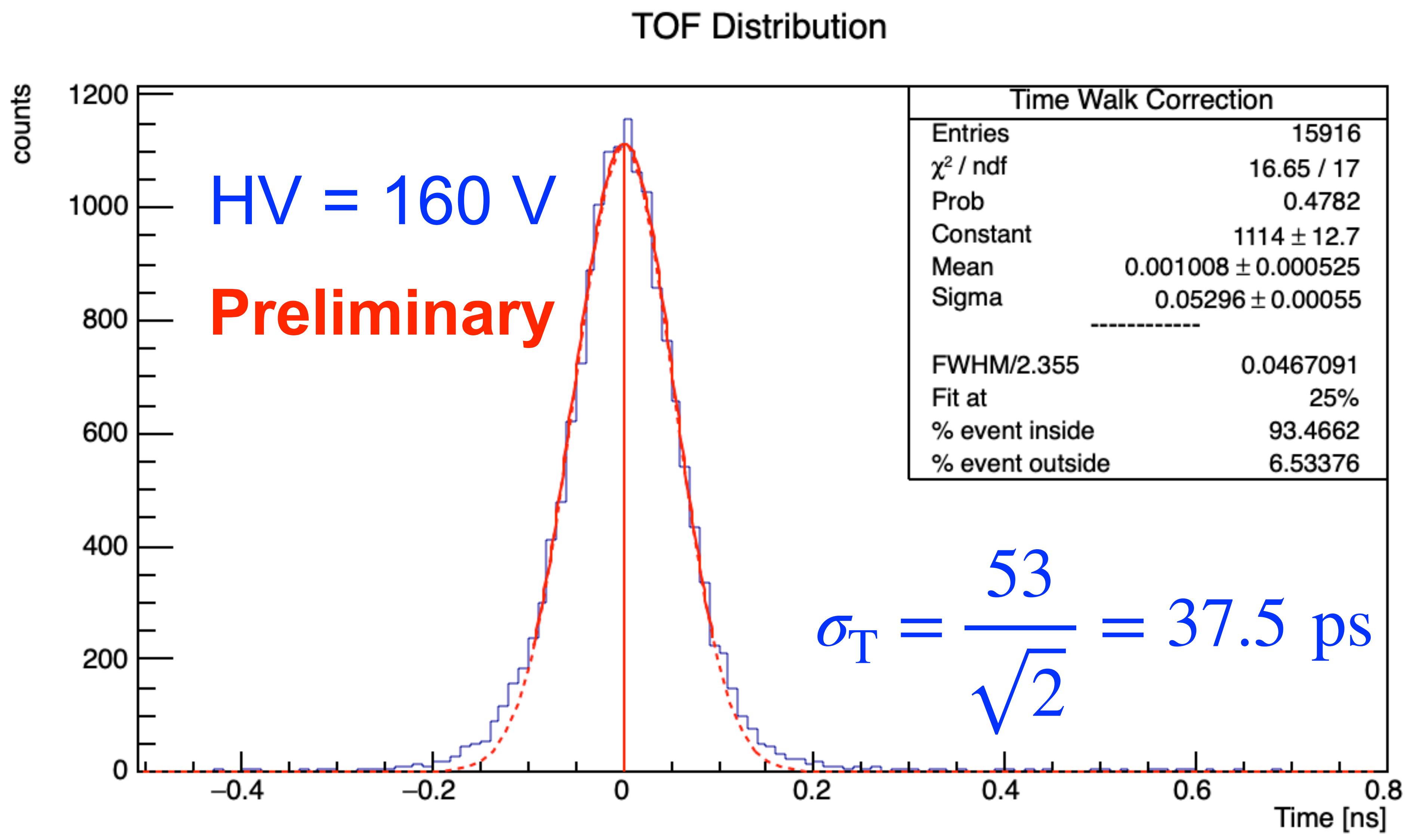
1. Active pixel
   - ➡ Front end in pixel
   - ➡ HBT preamp + driver (in pixel) + CMOS discriminator (outside pixel)
2. PET-project version:
   - ➡ HBT preamp + CMOS discriminator
3. Limiting amplifier:
   - ➡ HBT preamp + HBT limiting amplifier
4. Double threshold:
   - ➡ HBT preamp + two CMOS discriminators
5. Analog channels:
   - ➡ HBT preamp + two HBT Emitter Followers to 500Ω resistance on pad



The "ATTRACT" prototype

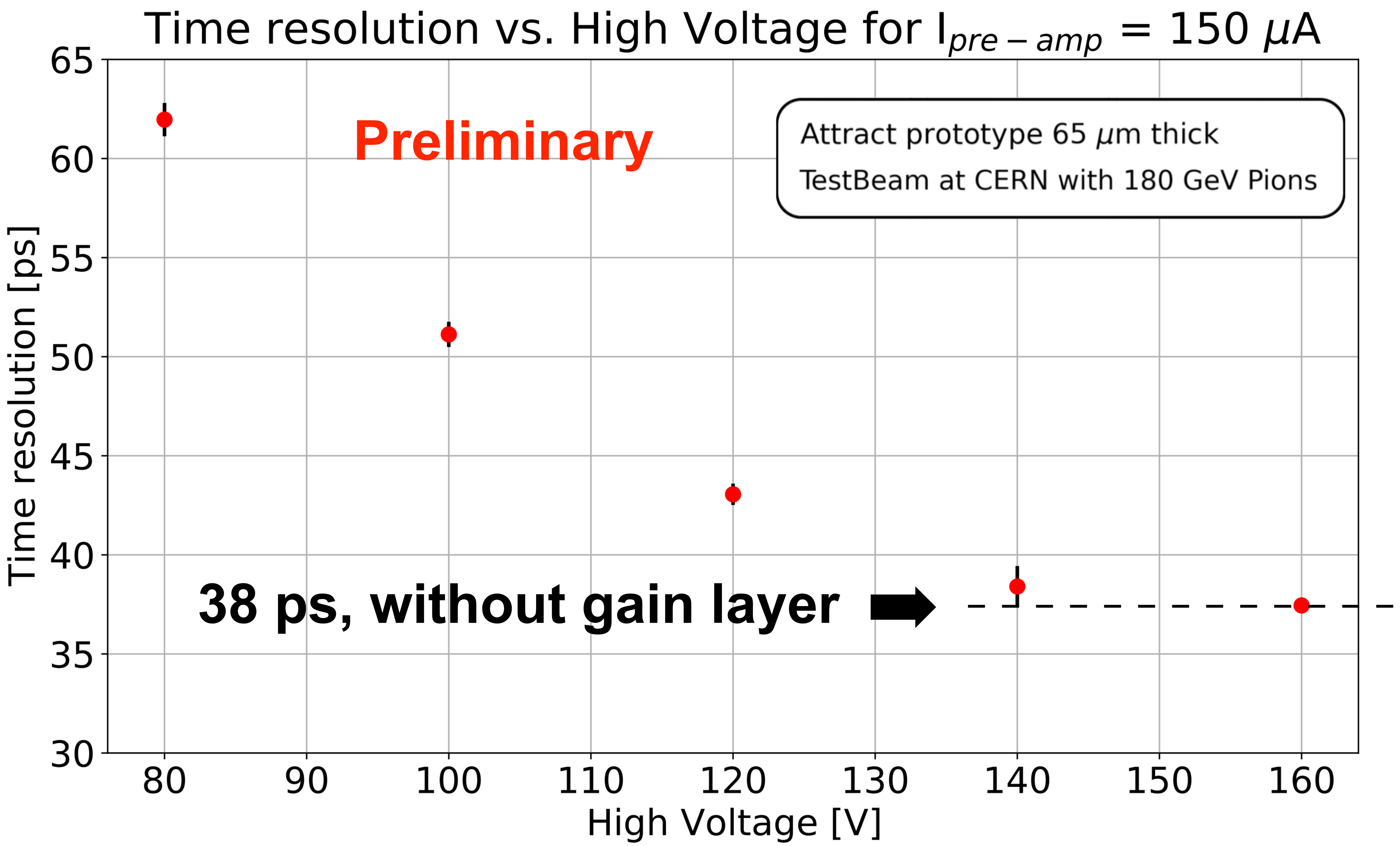


CERN SPS **testbeam** in July 2021
TOF resolution between two sensors
Very simple data analysis



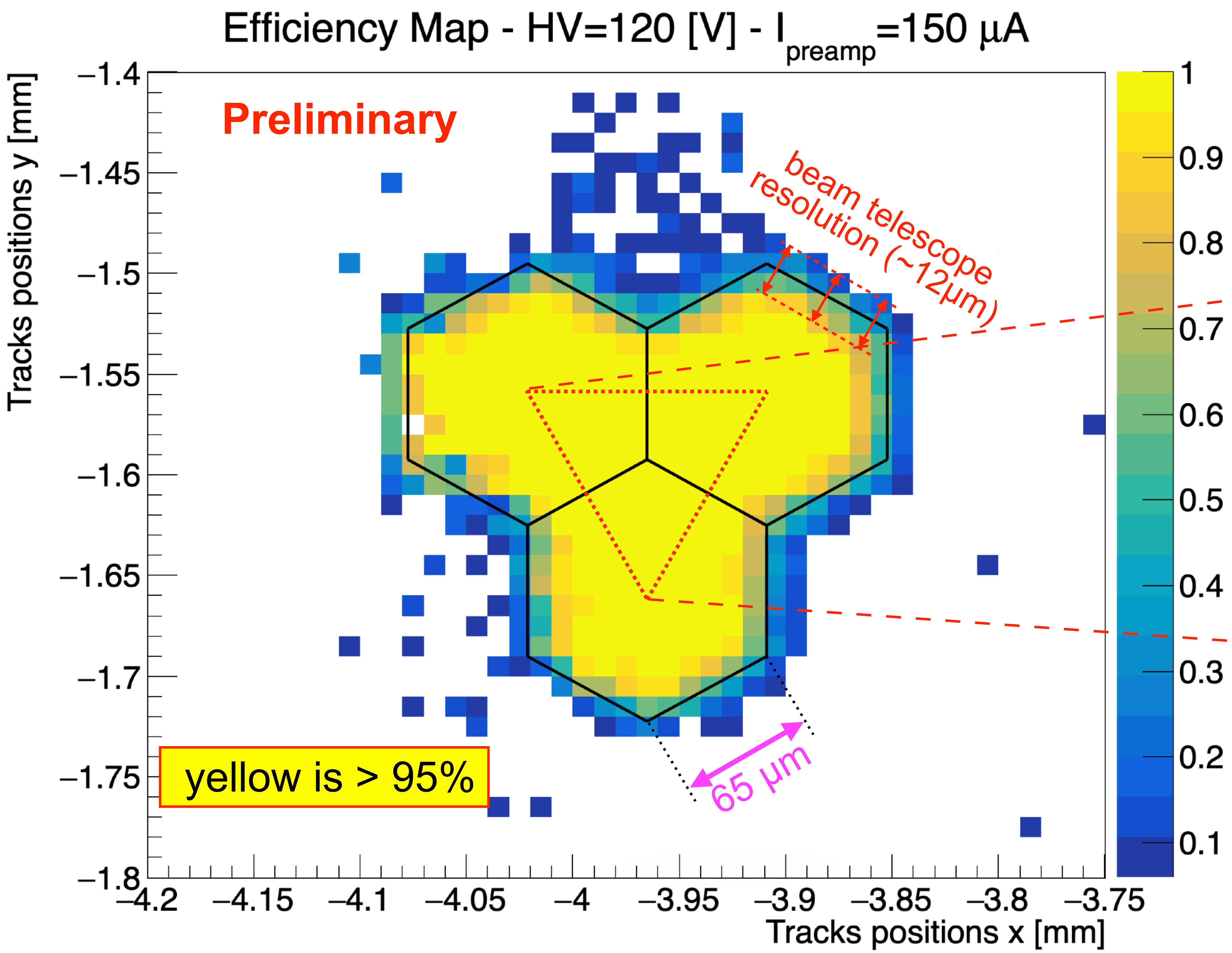
$$\sigma_T = \frac{53}{\sqrt{2}} = 37.5 \text{ ps}$$

Improved time-walk correction
(done now with signal amplitude):

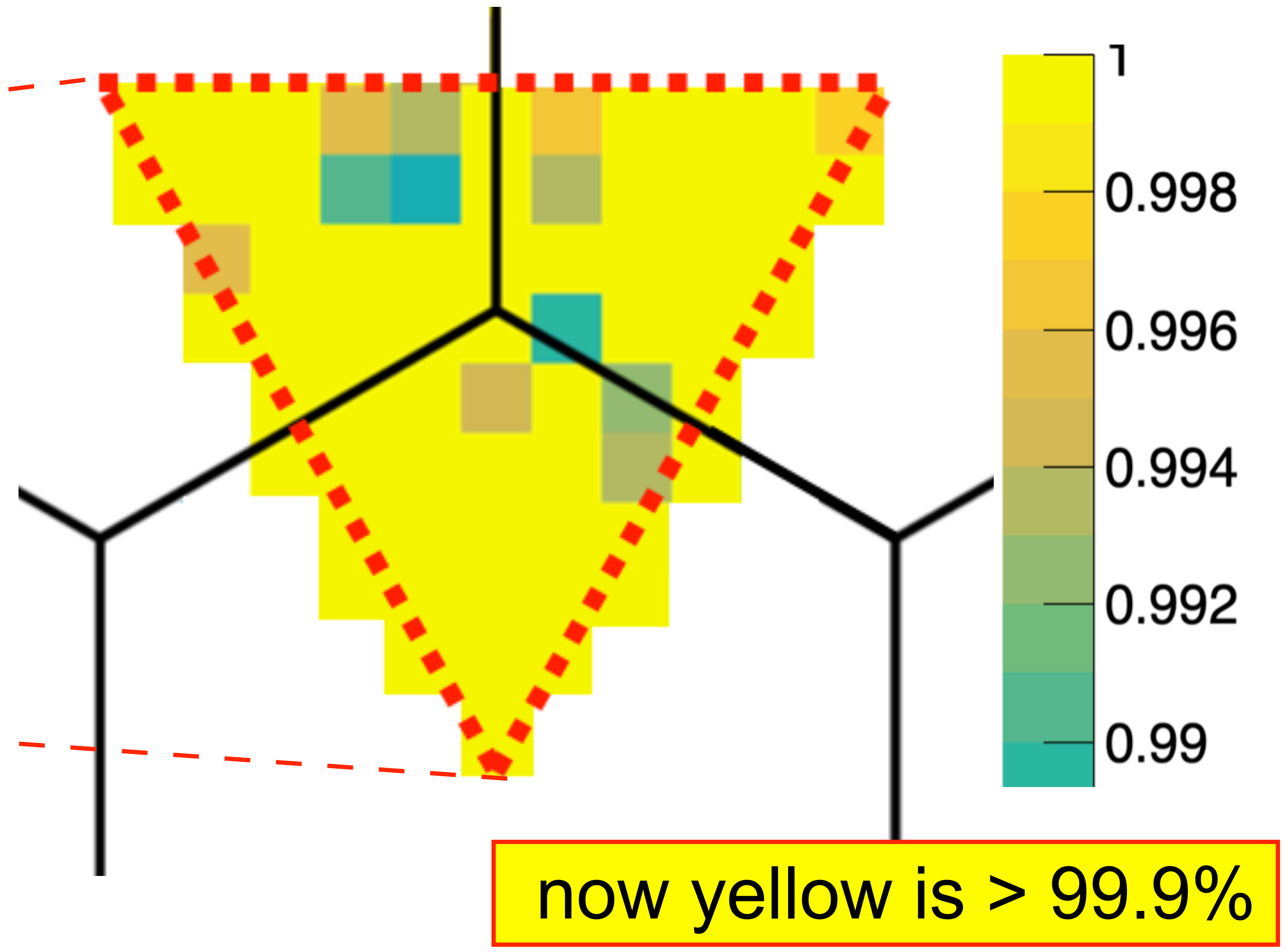


The “ATTRACT” prototype

Efficiencies measured at the SPS testbeam:



To get rid of the effect of the telescope precision, we can use the bins of the area inside the **red triangle**, that represents the entire pixel area **in the right proportions** :



Inside red triangle:
efficiency = **(99.87 ± 0.13)%**

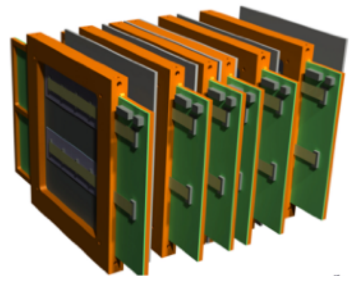
With these prototypes **the first phase comes to an end**:
R&D on monolithic SiGe BiCMOS very successful,
with results that exceed the initial goal of resolutions below 100ps

Second phase opening, with three funded projects:

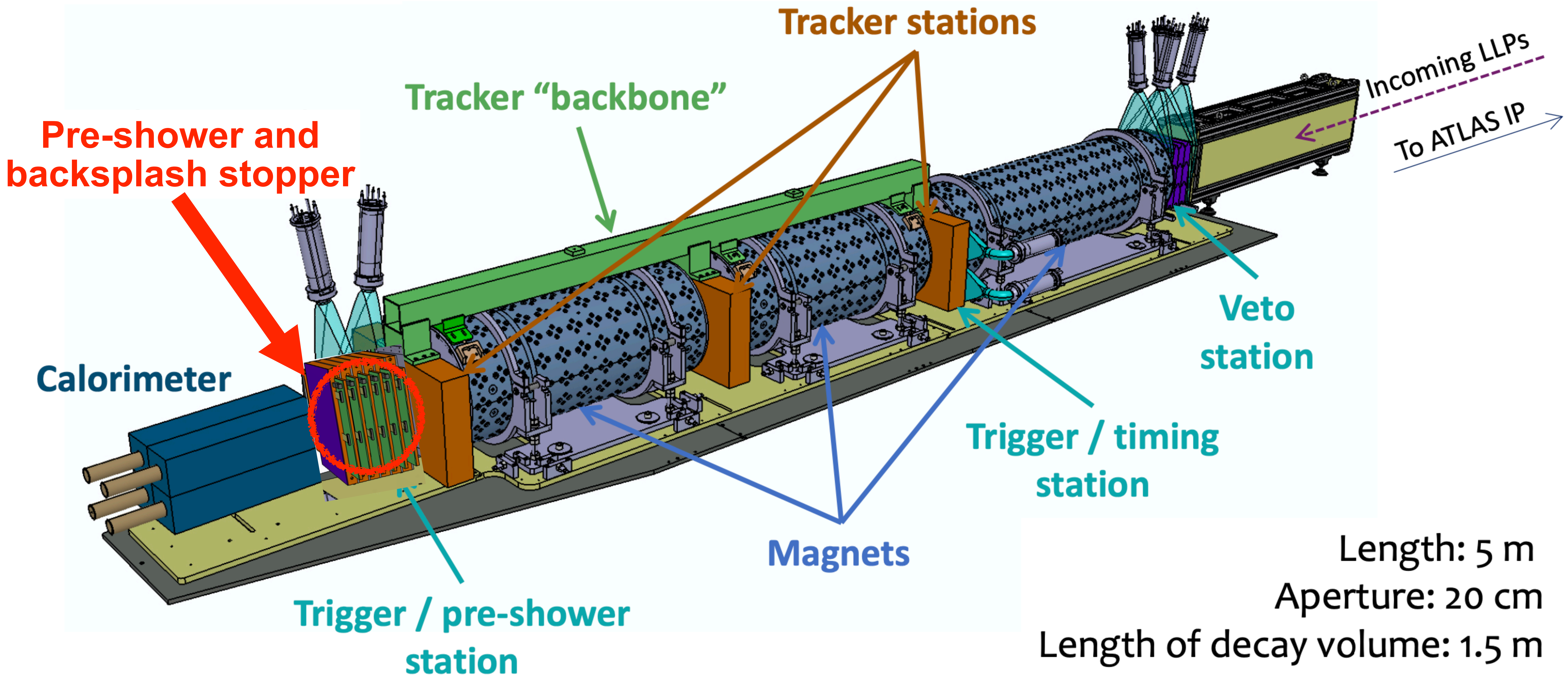
1. The FASER high-resolution W-Si preshower
2. 100μPET: ultra-high resolution molecular imaging
3. MONOLITH: monolithic PicoAD detector

1. The FASER high-resolution W-Si preshower

1. The FASER high-resolution W-Si preshower



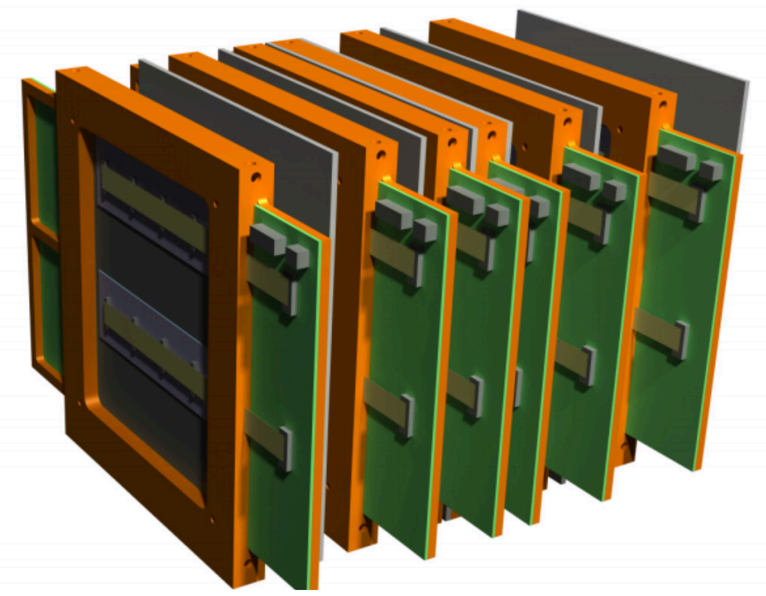
Present FASER detector very well instrumented to detect **charged-particles** pairs, but NOT YET for **photon pairs**



Length: 5 m
Aperture: 20 cm
Length of decay volume: 1.5 m

UNIGE groups of Anna Sfyrla & Giuseppe Iacobucci + FASER groups of MAINZ, CERN, JAPAN, TSINGHUA

1. The FASER high-resolution W-Si preshower

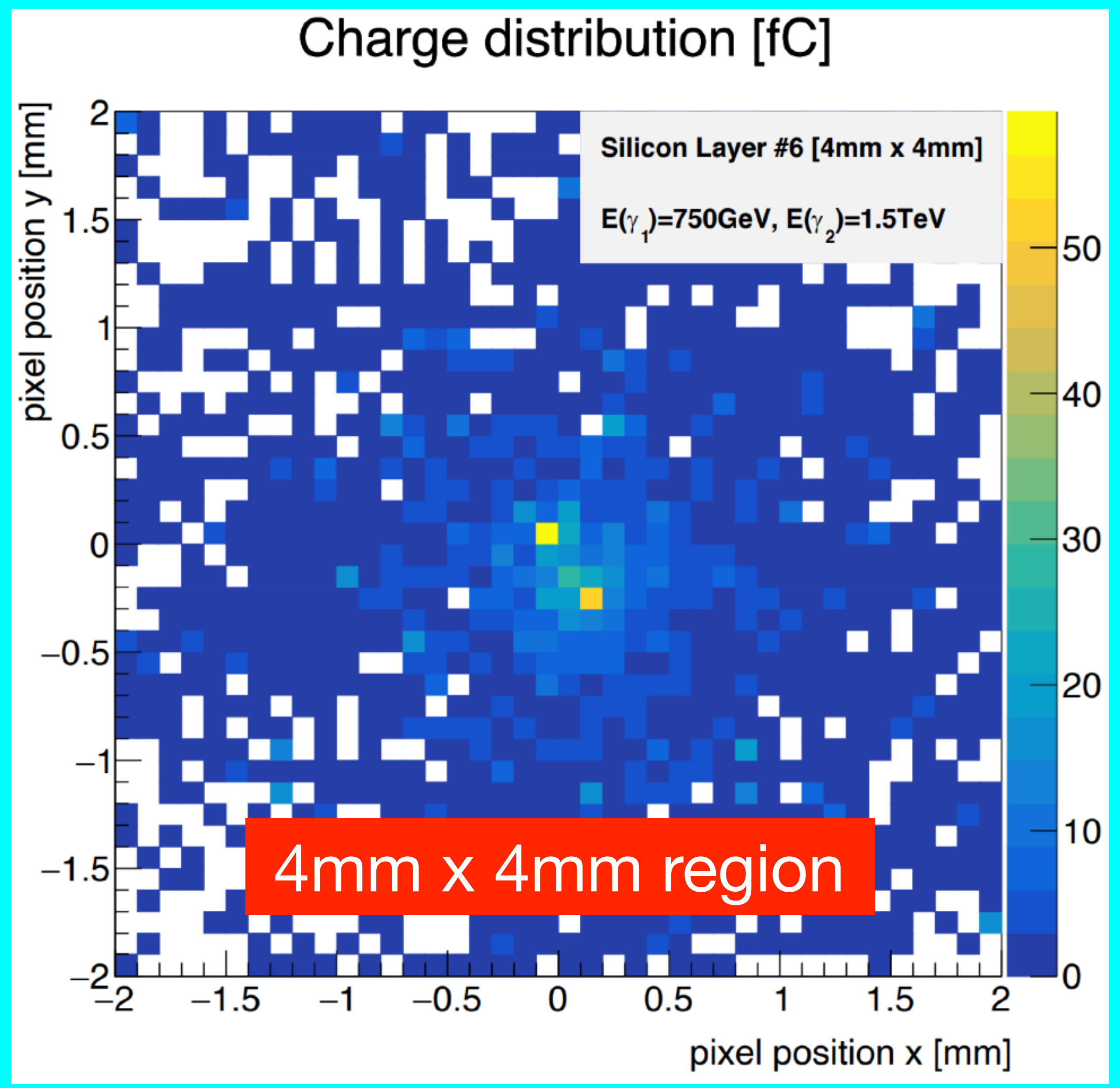


Several layouts studied. **Chosen baseline:**

6 planes of $1X_0$ tungsten + monolithic silicon sensors with **100µm pitch**

GEANT full **simulation**:

ALP production with F. Kling generator and **tracked** with GEANT4

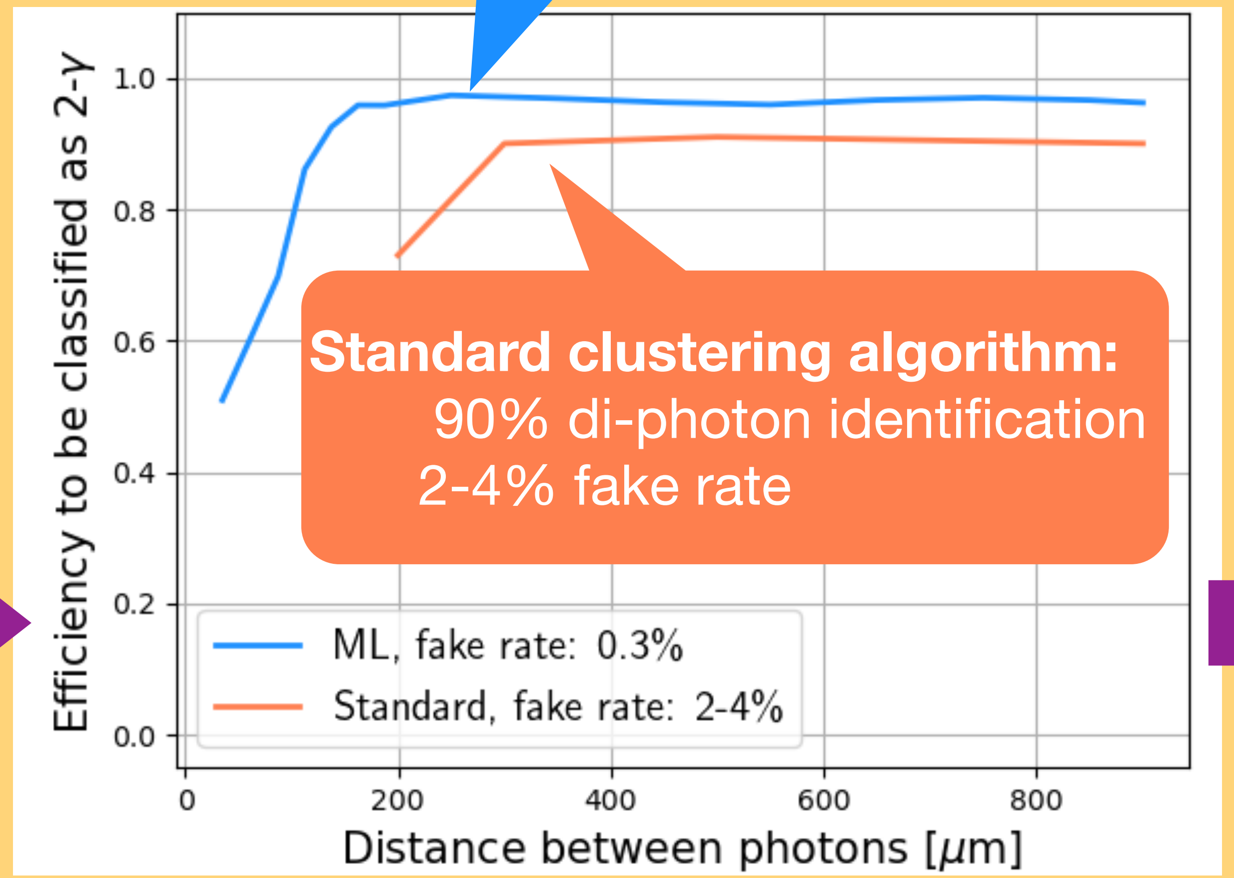


Two photons at 200µm distance ($E_{\gamma 1}$=0.75 TeV, $E_{\gamma 2}$= 1.5 TeV) : distinguishable due to the 100µm pitch

Cluster **reconstruction**:

Trained CNN:
95% di-photon identification
<0.5% fake rate

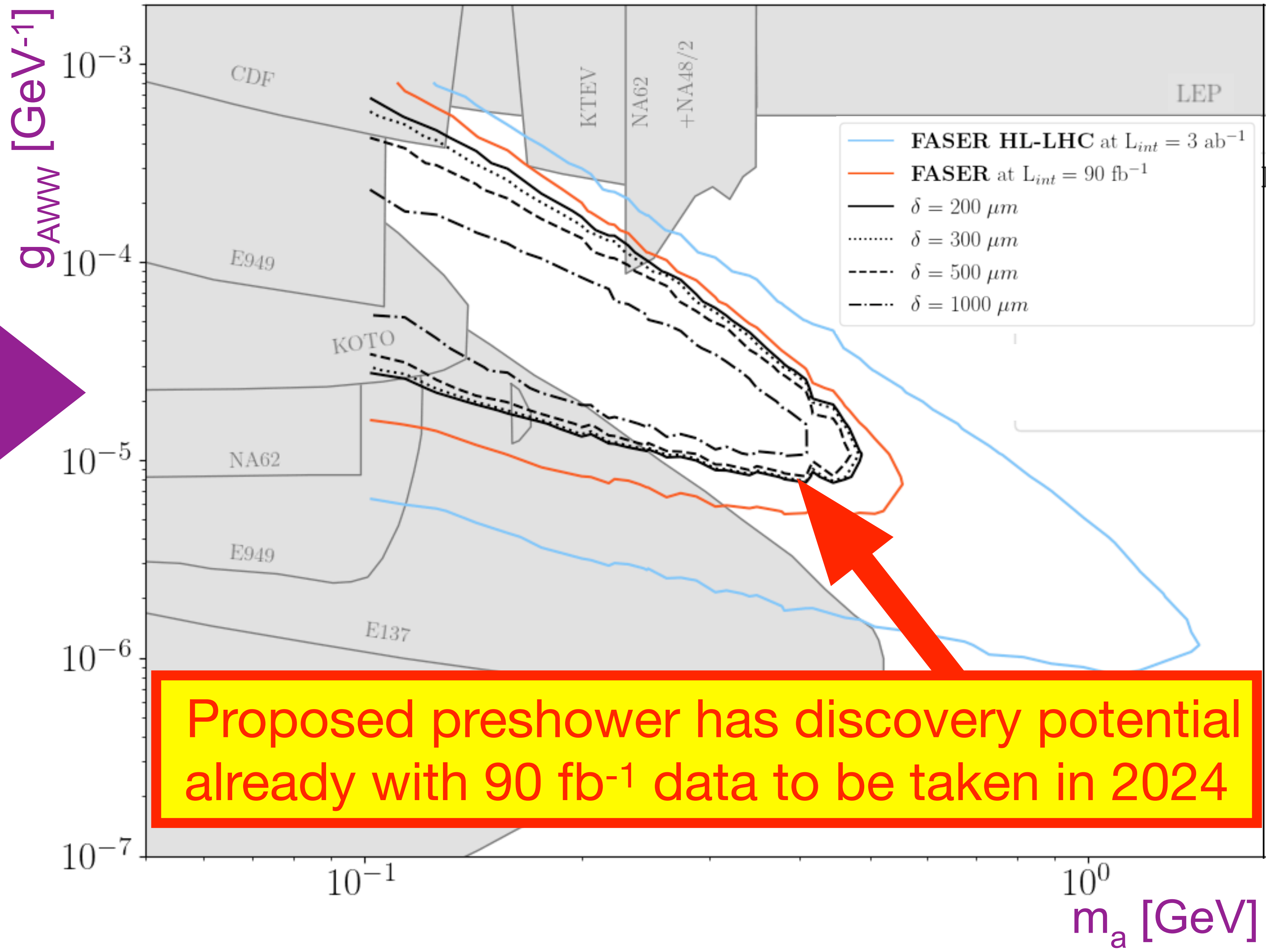
Standard clustering algorithm:
90% di-photon identification
2-4% fake rate



First attempt of **ML** provides higher efficiency and strong reduction of fake rates

Axion-like particle **sensitivity reach**:

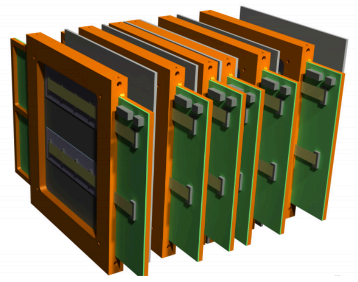
Grid of ~1500 (m_a,g_{aWW}) points from the ALP model, convoluted with the GEANT4 efficiency matrix across photon energies and separations:



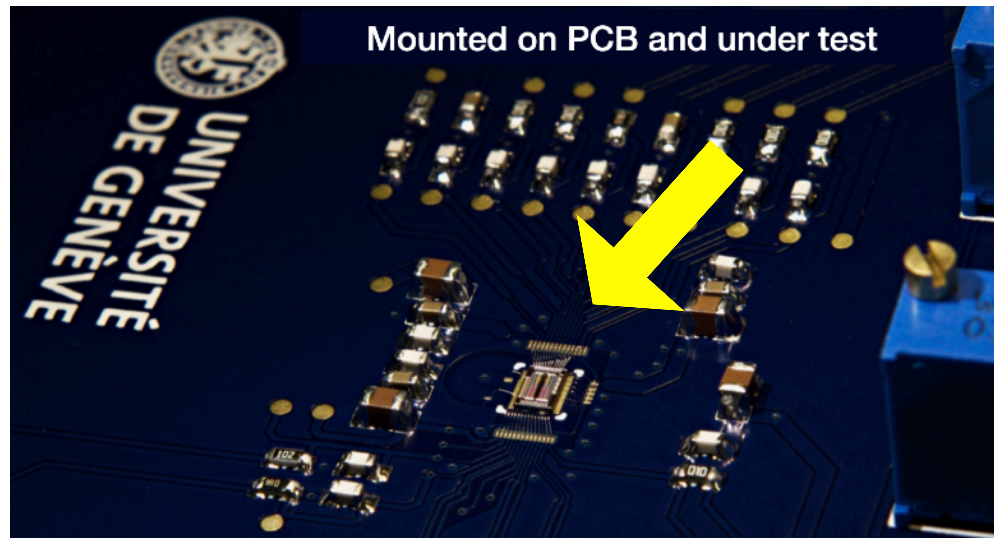
Proposed preshower has discovery potential already with 90 fb^{-1} data to be taken in 2024

UNIGE simulation&reconstruction team:
Carlo Pandini, Chiara Magliocca, Théo Moretti, Giuseppe Iacobucci, Lorenzo Paolozzi, Chiara Rizzi, Anna Sfyrla, Noshin Tarammum, Didier Ferrere, Frank Cadoux + help from Felix Kling for the generators

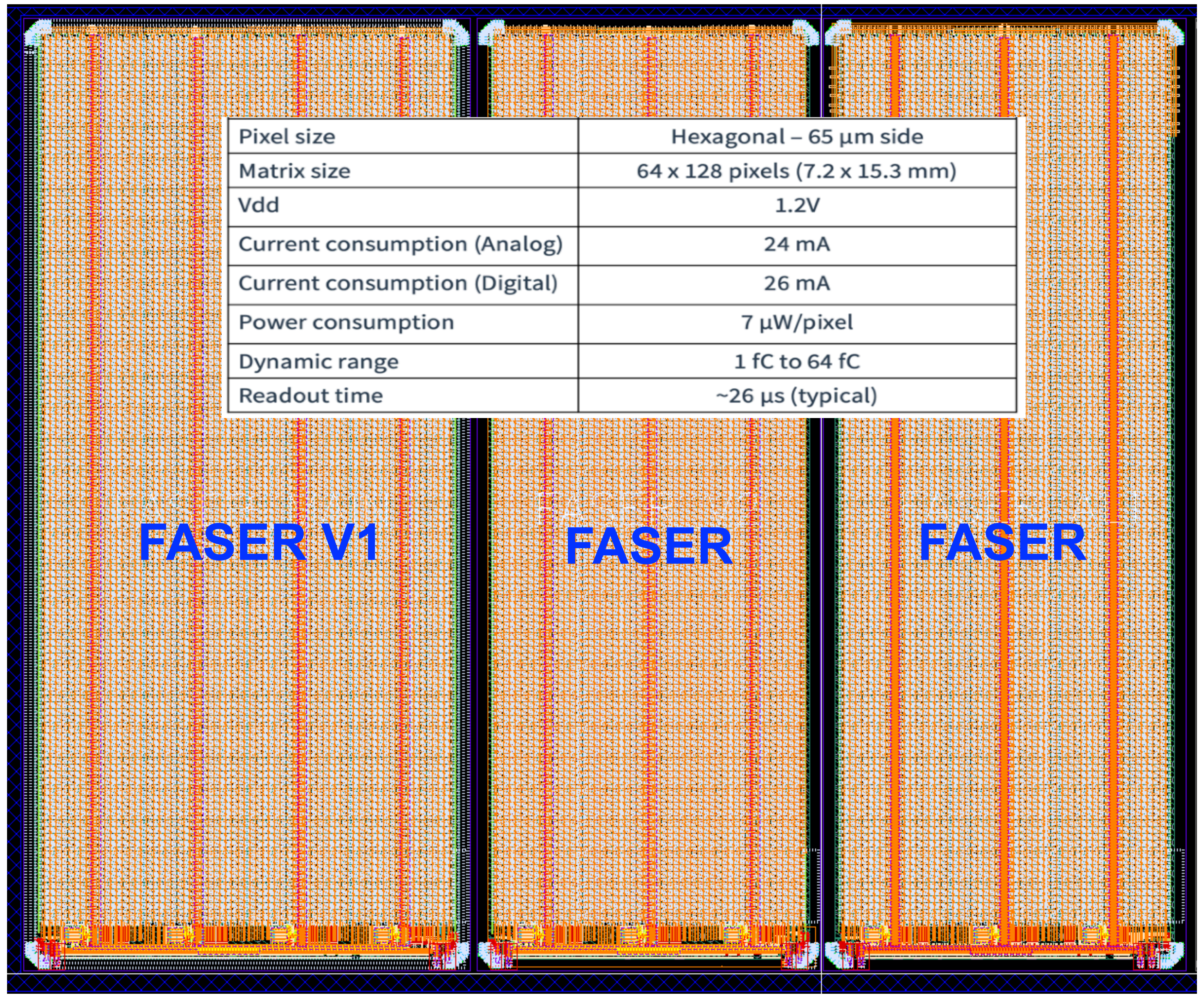
1. The FASER high-resolution W-Si preshower



- **Small-size FASER prototype** ASIC.
  Tests completed with **good results**:
  - FE electronics integrated in pixel works as expected
  - No cross talk observed



- **FASER full-reticle preproduction chip submitted:**
  (first large-area (2.0 x 1.5 cm²) chip by our group)
  - In IHP 130nm SiGe BiCMOS process
  - Chip divided in «supercolumns» (16x128 pixels) with a ~40μm inactive slice of digital logic in between
  - Three matrices (FASER V1/V2/V3) with different flavours
- **Huge dynamic range**: 1fC to 64 fC
- These chips will be used to build prototype modules



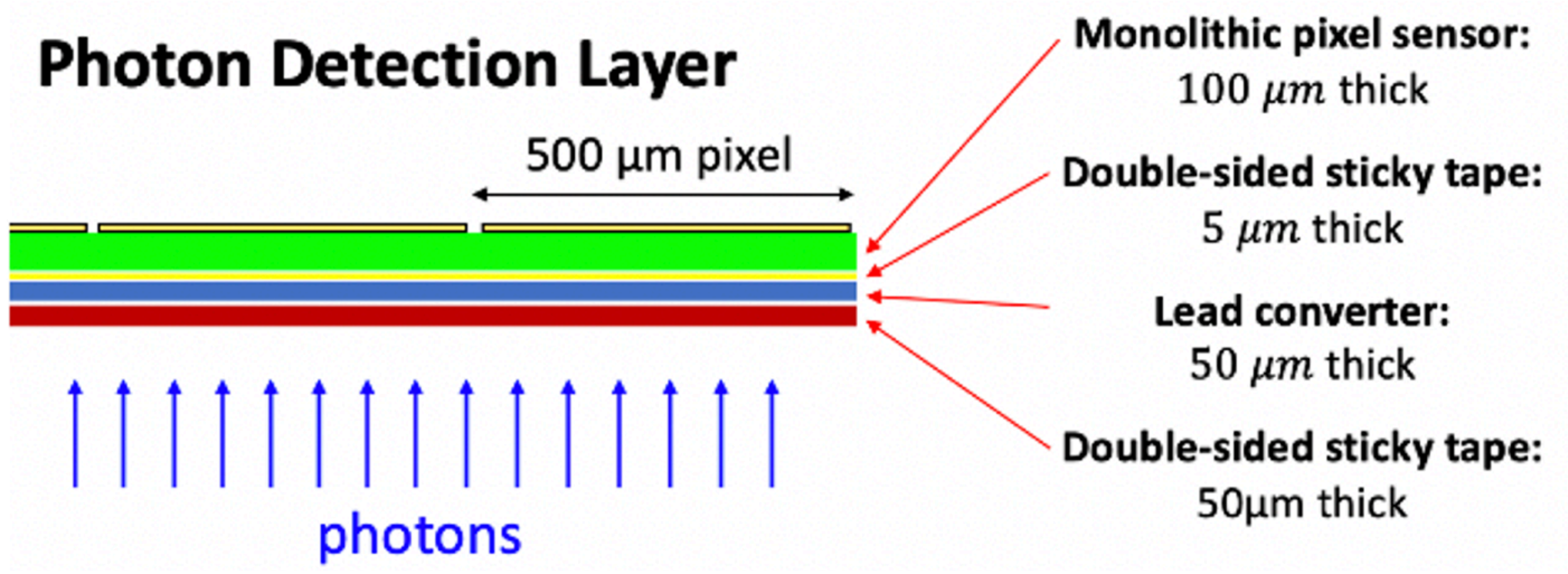
Pixel size	Hexagonal – 65 μm side
Matrix size	64 x 128 pixels (7.2 x 15.3 mm)
Vdd	1.2V
Current consumption (Analog)	24 mA
Current consumption (Digital)	26 mA
Power consumption	7 μW/pixel
Dynamic range	1 fC to 64 fC
Readout time	~26 μs (typical)

2. The 100µPET project:

pioneering ultra-high resolution molecular imaging

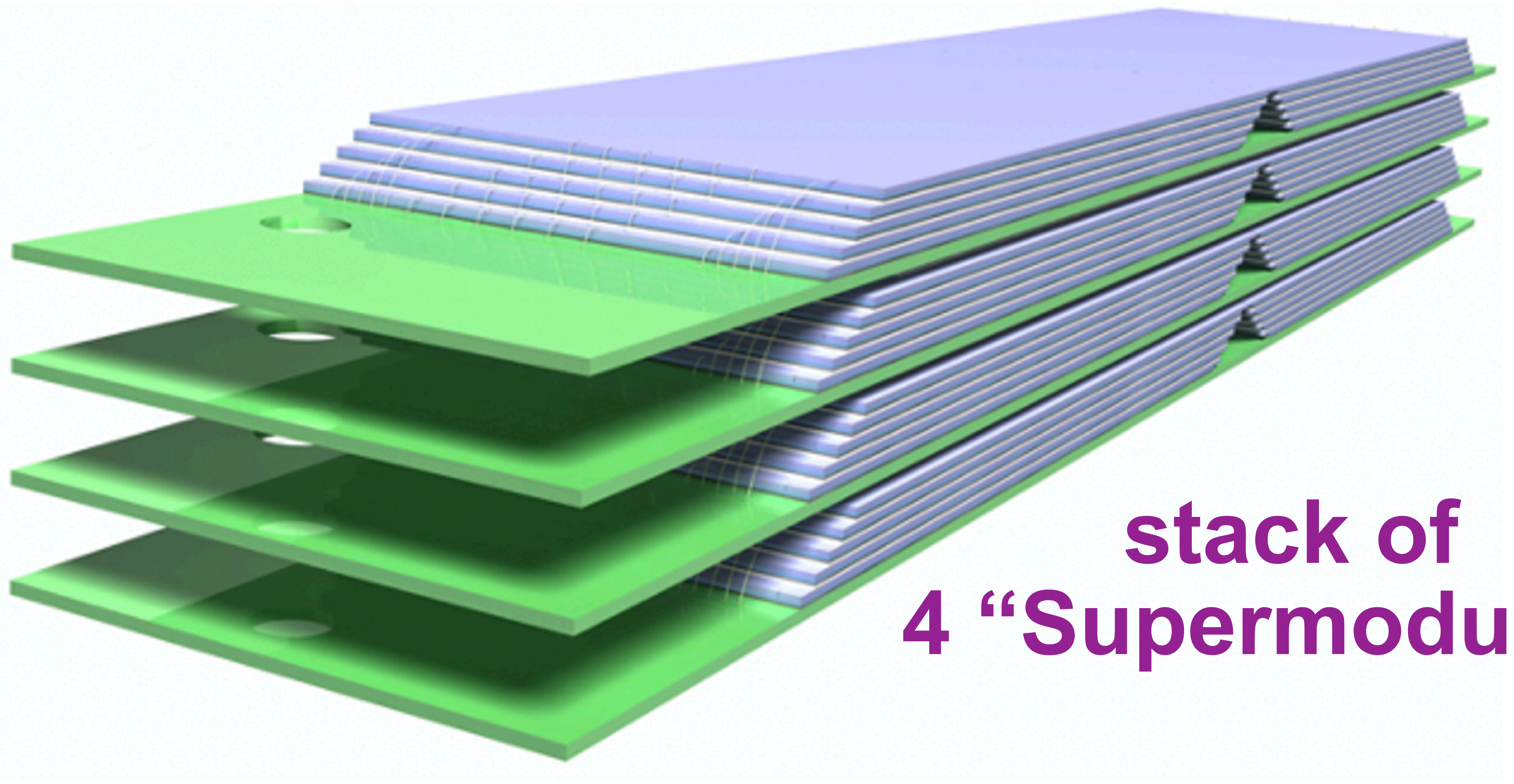
2. The 100µPET project

- SNSF SINERGIA project 2021-2025 (partners: **HUG** and **EPFL**)
  - **Idea**: multi-layer of silicon pixel sensors to detect photons converted in 50µm of lead
  - Pitch 100µm ⟹ ~200µm point-spread functions
  - 200ps resolution ⟹ reduce accidental coincidences

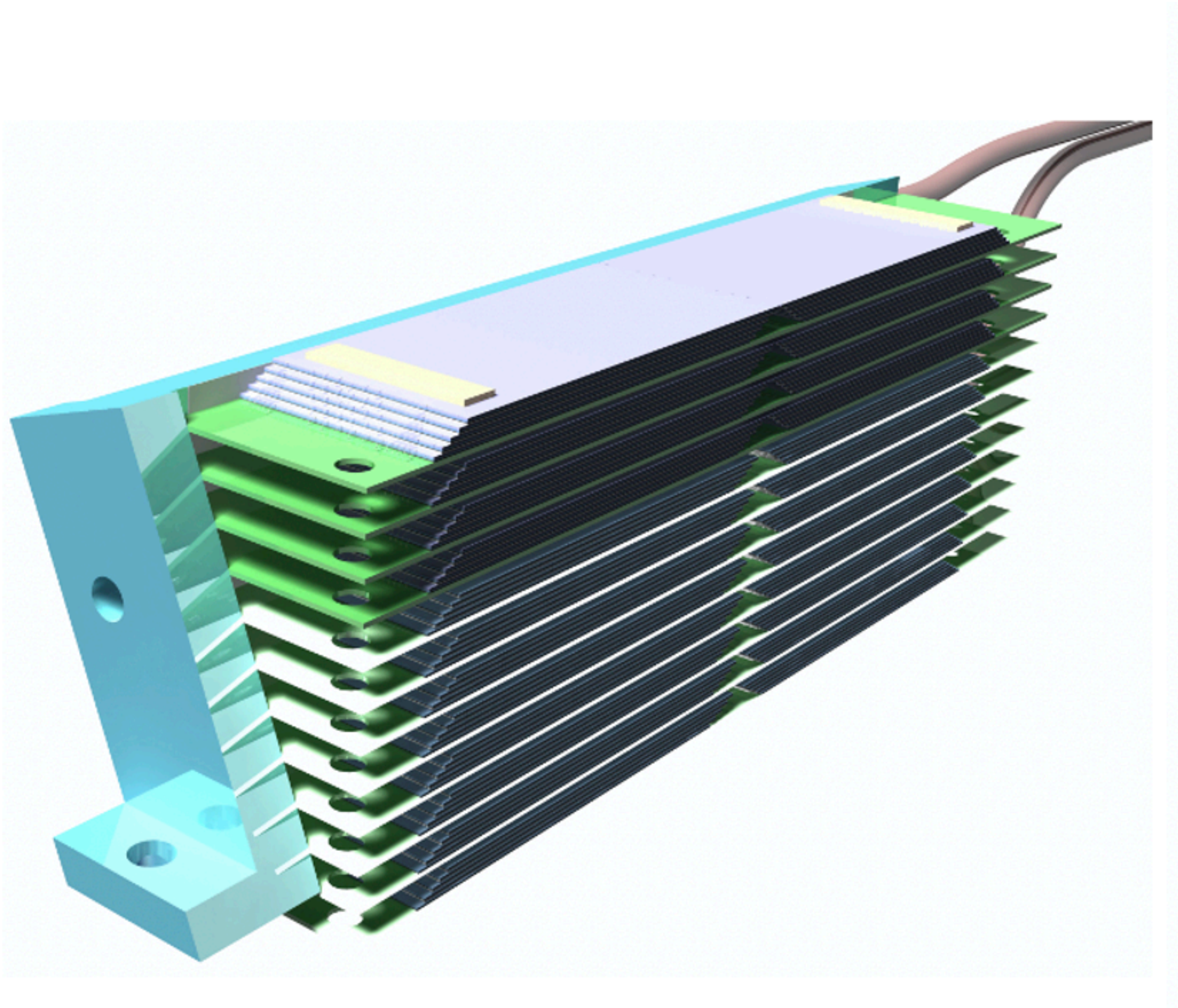


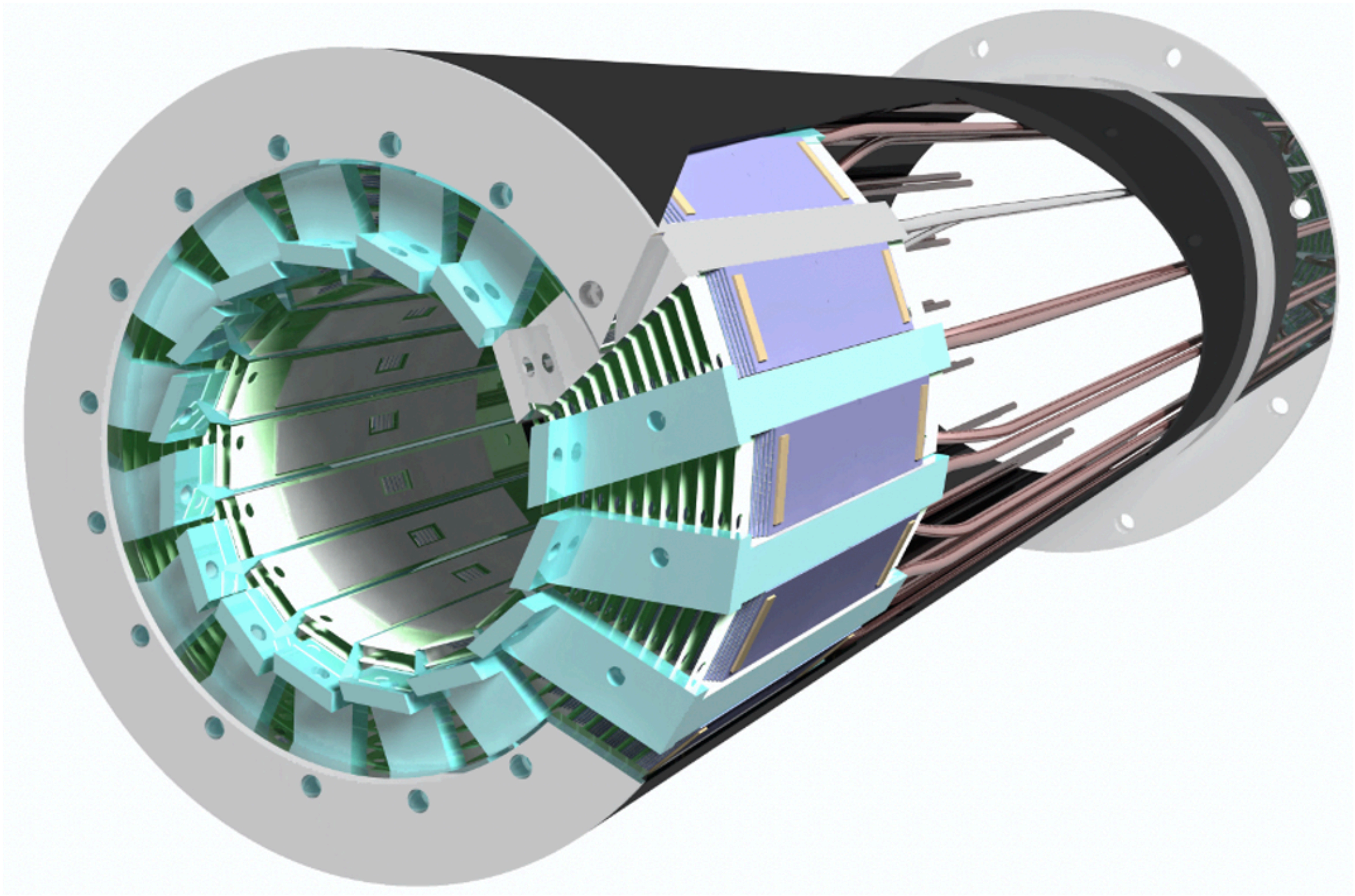
  - **"Supermodule"** (5 detection layers, in blue) on a electronics support board (in green) where the chips are wire-bonded for power and I/O

A similar system being explored by ALICE colleagues to prototype a **"silicon chamber"**



2. The 100μPET project

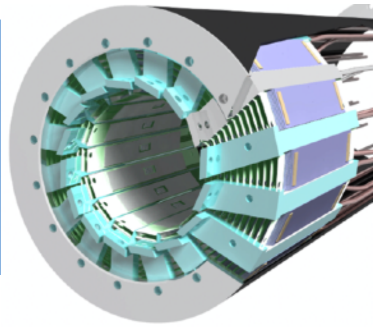




"Tower" of 12x5 = 60 detection layers

16 Towers all around to form the scanner

2. The 100μPET project



- Monolithic technology at last allows to realise the old idea to use silicon for PET:

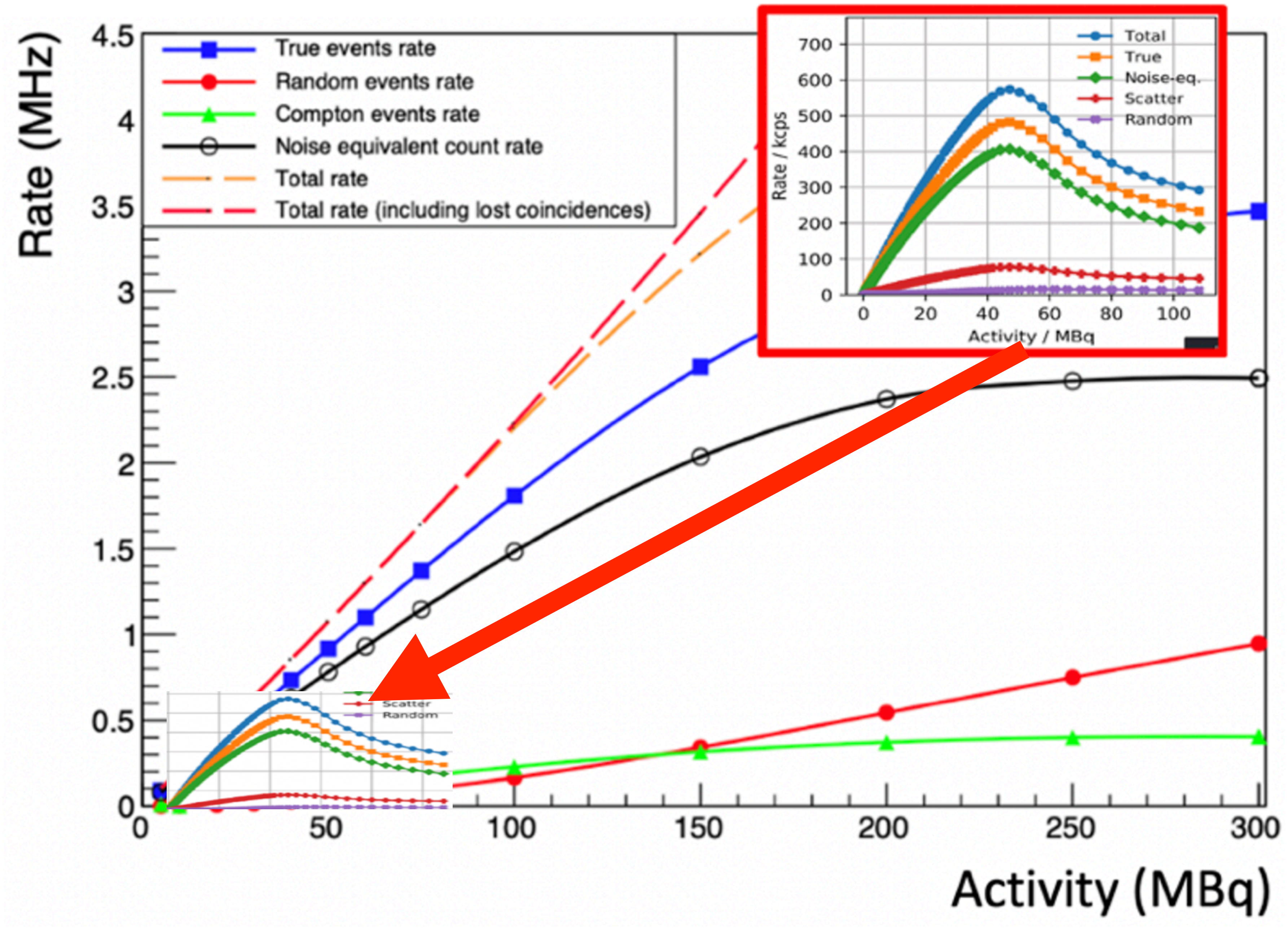
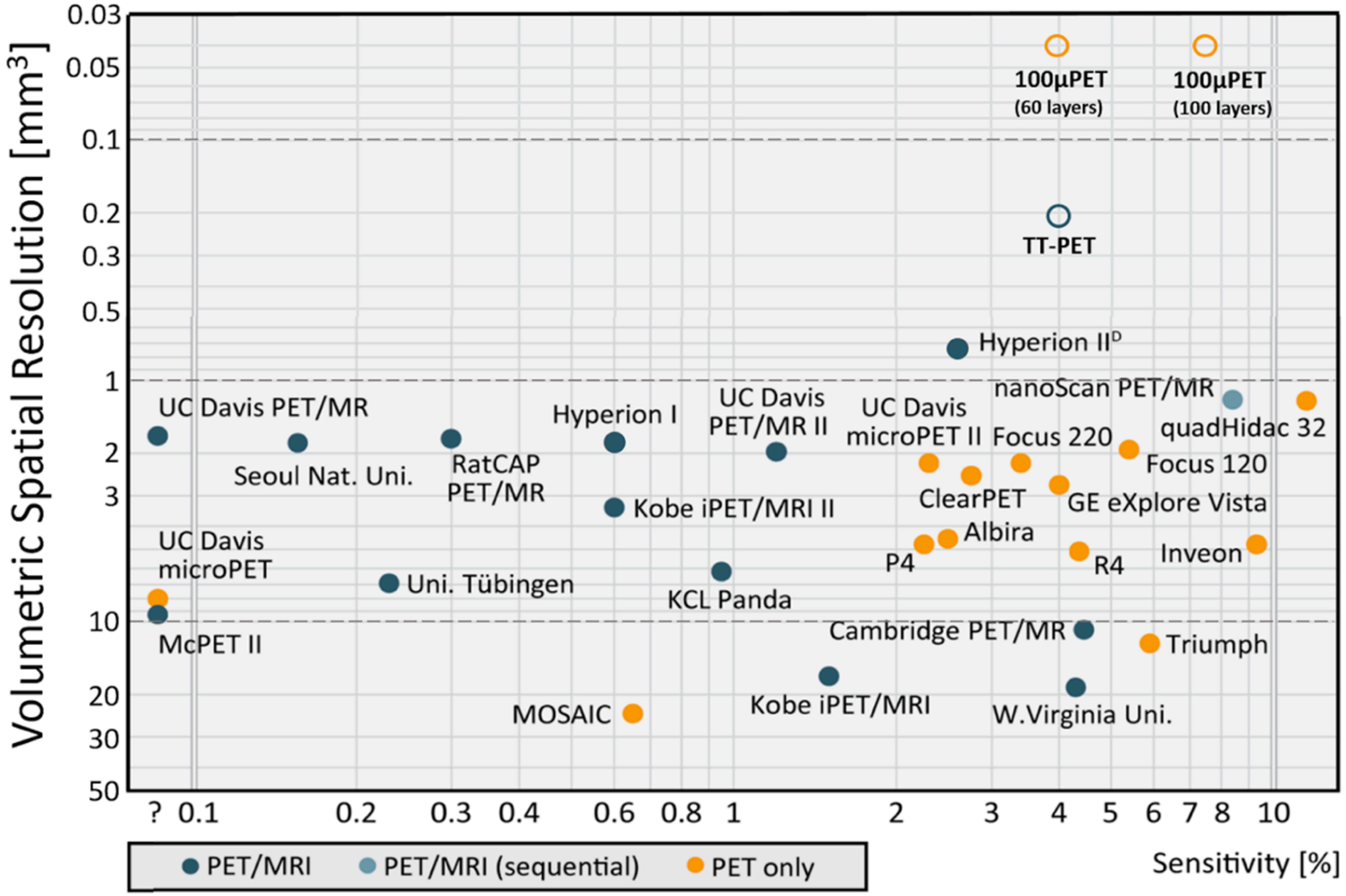


Figure 7: Expected coincidence rate and NECR vs. source activity. A cylindrical phantom as prescribed by [58] was used. For comparison, the insert shows the results obtained by the Hyperion IID [59] scanner.



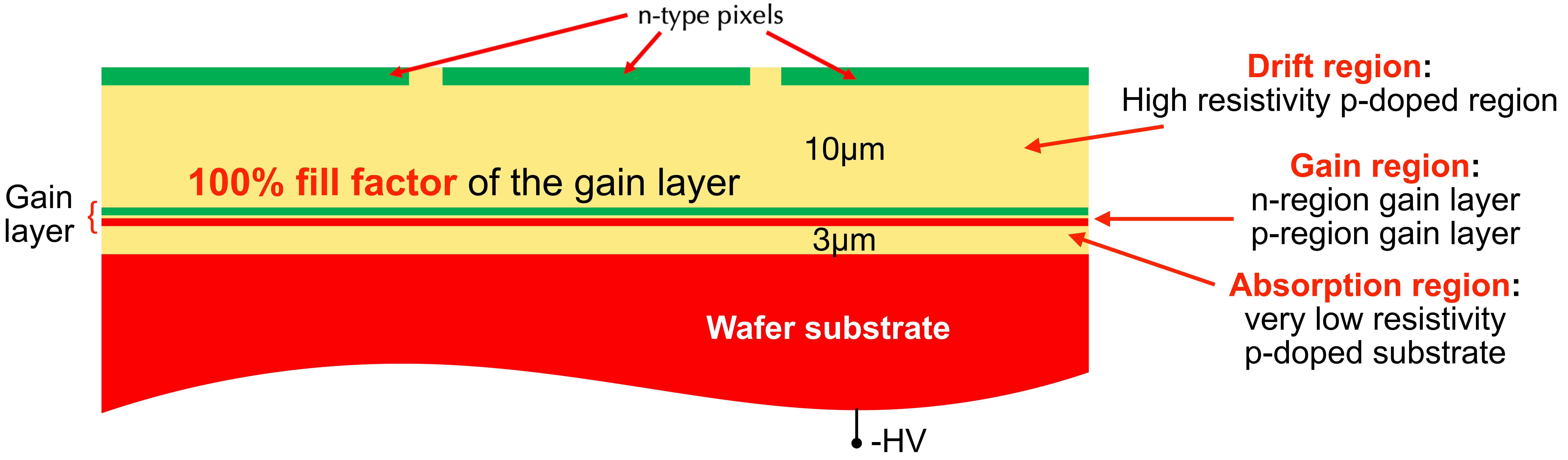
3. The MONOLITH

ERC project

MONOLITH: Monolithic Picosecond Avalanche Detector

AIM of the project:

monolithic implementation of our **low-noise ultra-fast SiGe BiCMOS electronics** with the **Picosecond Avalanche Detector** (**PicoAD, EU Patent EP18207008.6**), a **multi-junction pixelated avalanche detector** for ps time resolutions:



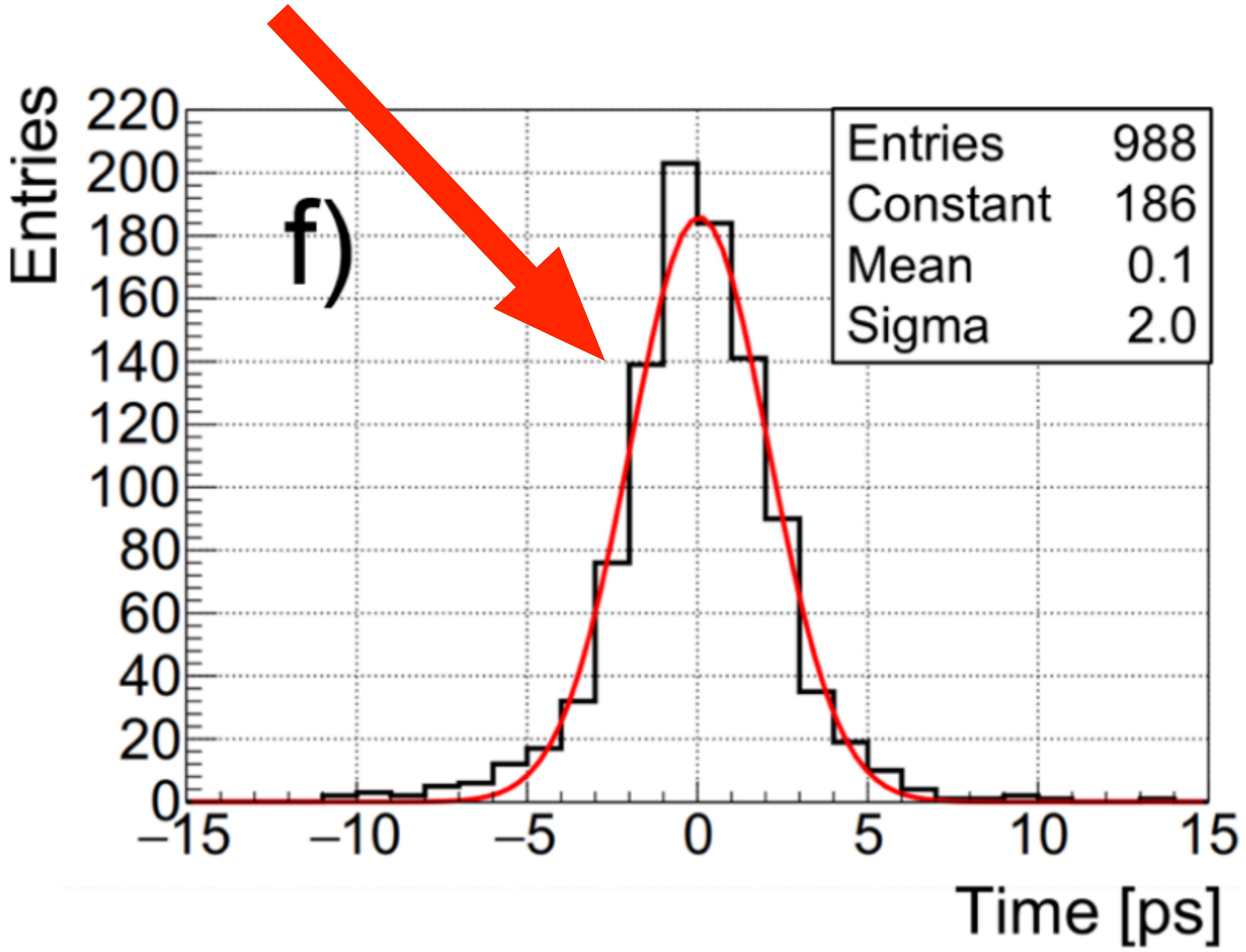
PicoAD devised to minimise Landau noise:
only electrons produced in the absorption region are multiplied ⇒ excellent timing

MONOLITH: Monolithic Picosecond Avalanche Detector

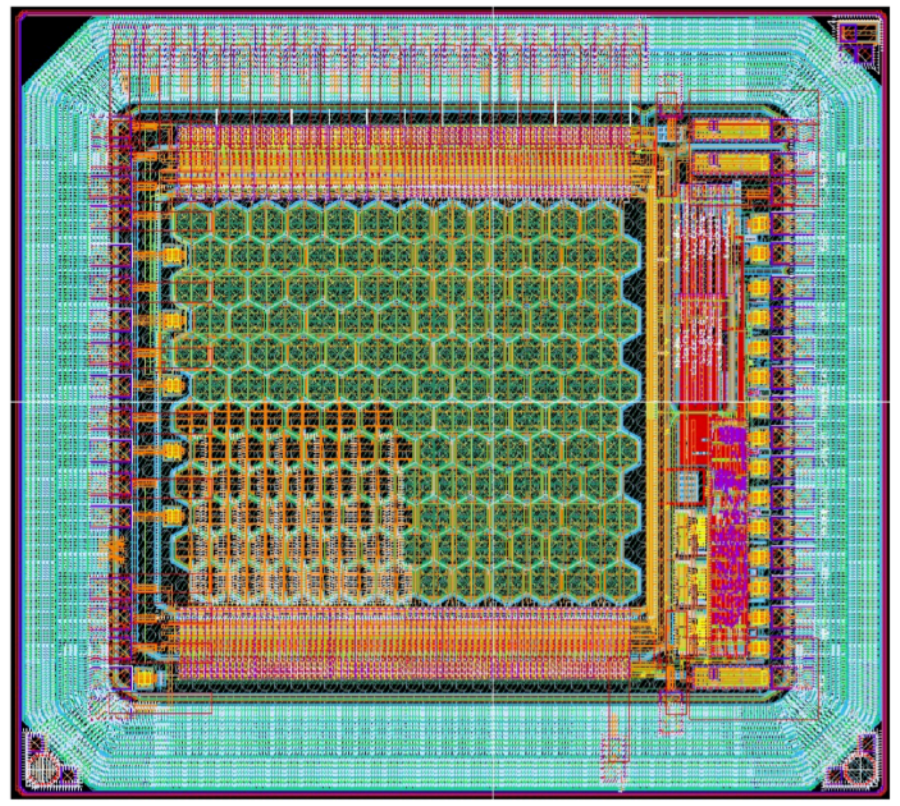
Multi-junction pixelated avalanche detector for ps time resolutions:

EU Patent EP18207008.6

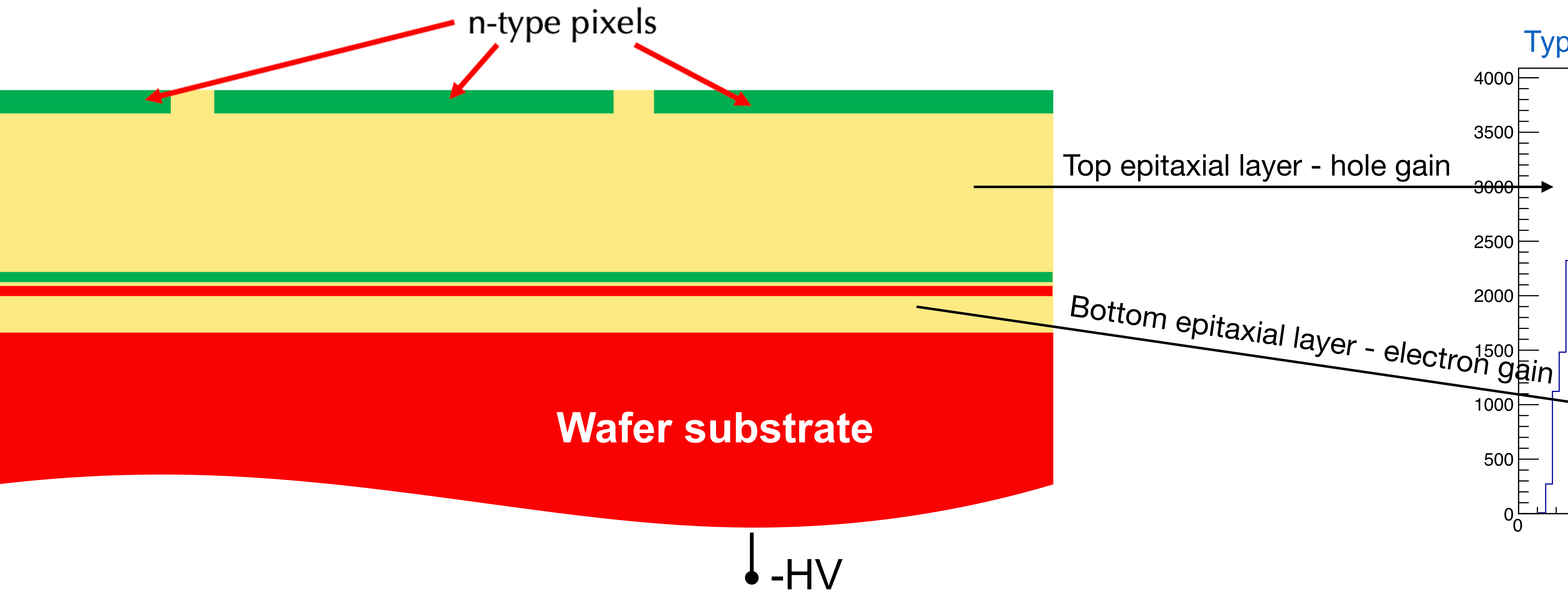
Unique timing performance:
GEANT4+CADENCE simulations show
2 ps time resolution
contribution from the sensor

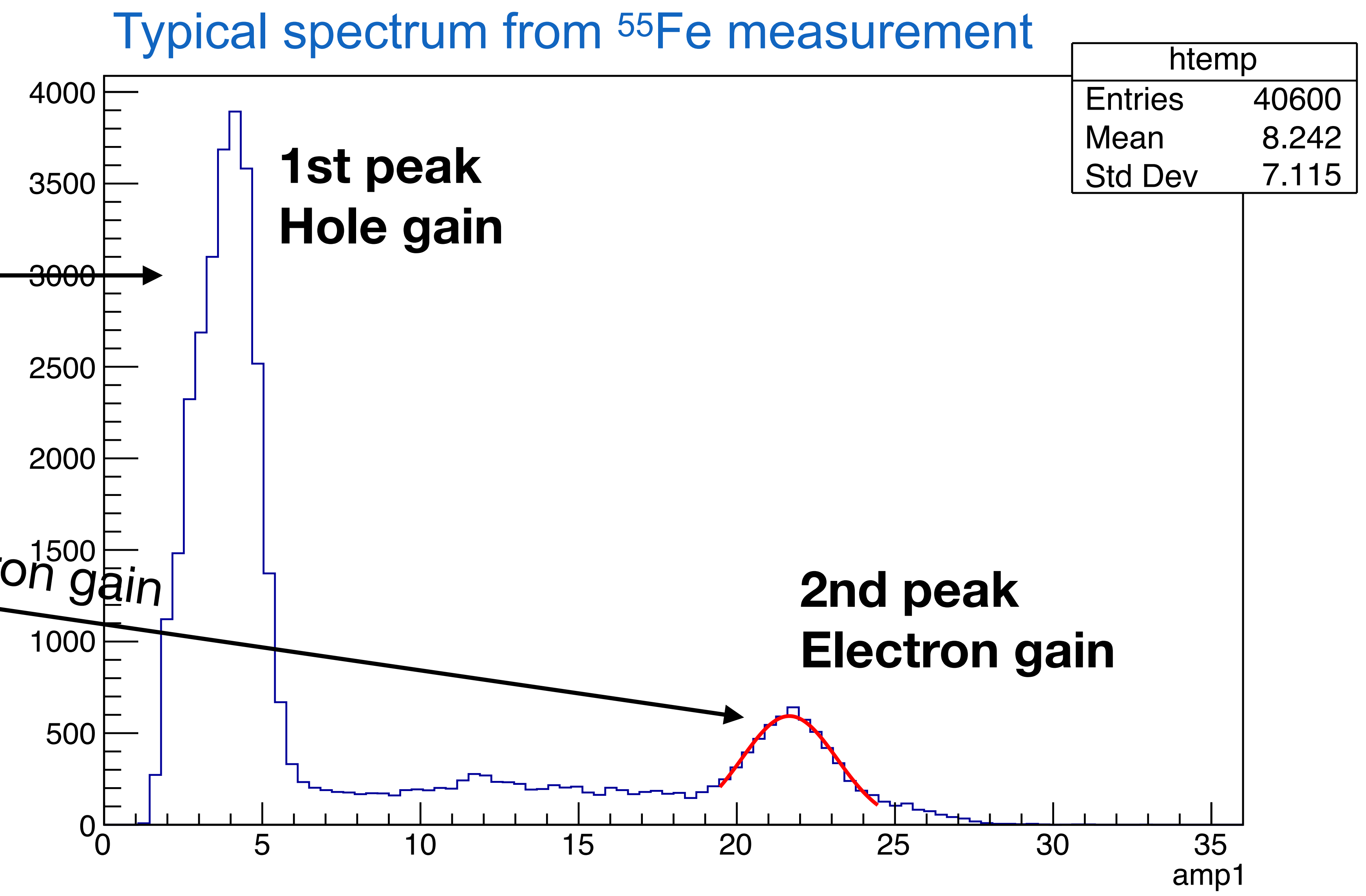


MONOLITH: Monolithic Picosecond Avalanche Detector

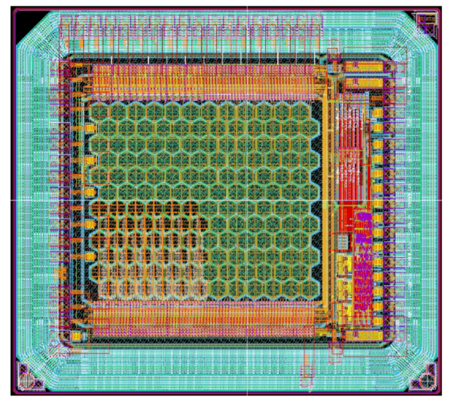


- **First PicoAD prototype**:
  - Integrated in a special wafer for the ATTRACT prototype.
  - Process design in collaboration with IHP
- Lab tests:
  - **Stable operation**, but small plateau due to non-optimal wafers processing
  - Test at low temperatures with **^{55}Fe sources**: two amplitude peaks measured

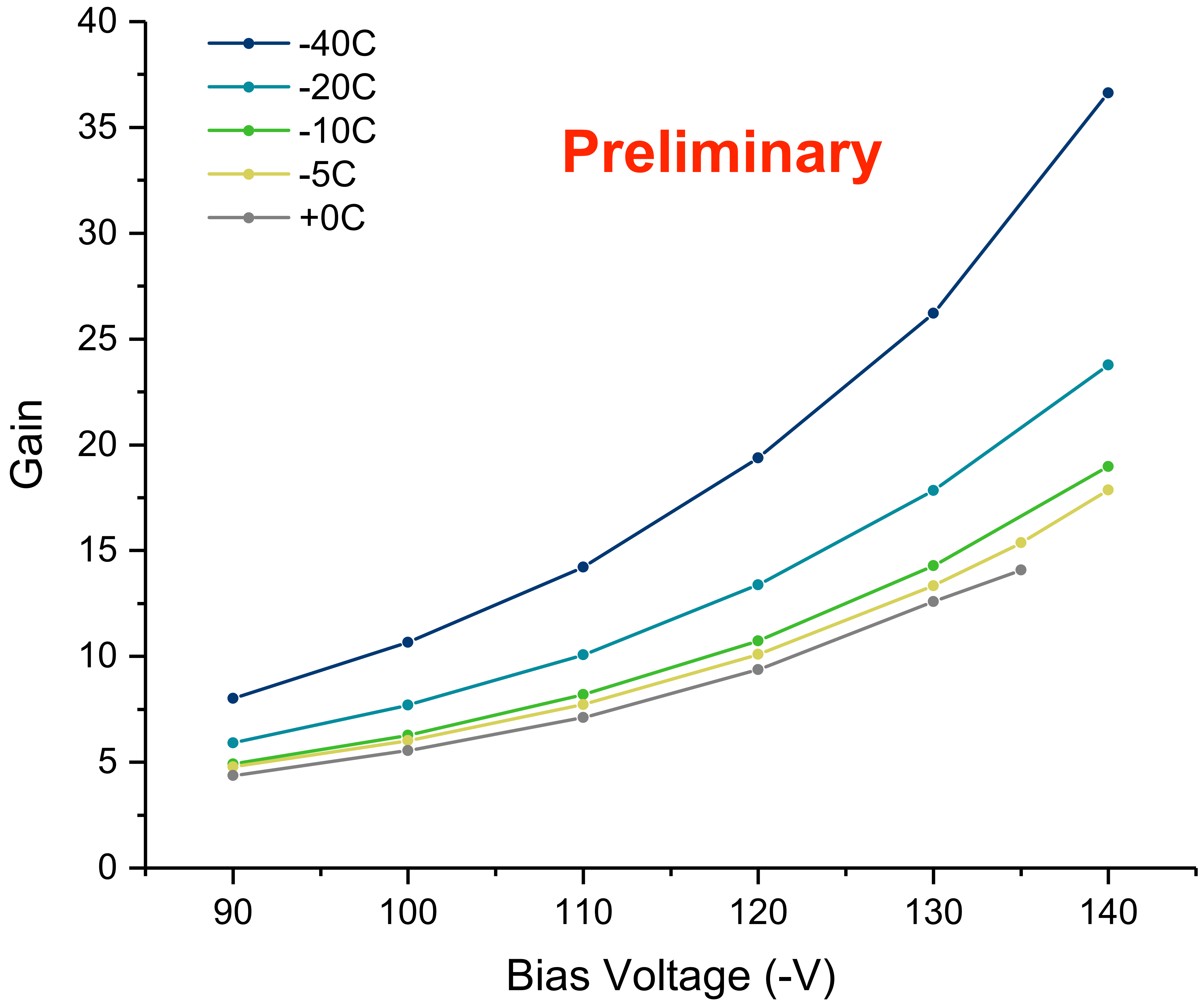




MONOLITH: Monolithic Picosecond Avalanche Detector



- **First PicoAD prototype**:
  - Measurement with ^{55}Fe source in UNIGE cleanrooms:



Measured gain: up to ~40

⬇ ⬇ ⬇

PicoAD concept works

Next steps:

1) **Testbeam at CERN** (Sept.-Oct.)
   to measure efficiency and time resolution
2) **Second prototype** (Q1 2022)
   on a wafer with better engineered epitaxial layers

Summary

- **SiGe BiCMOS technology** can be used to produce **ultra-fast**, **low-noise**, **low-power amplifiers**.

- We implemented these amplifiers in **monolithic sensors** with **100μm "pitch"** that are able to provide:
  - **Time resolutions < 40ps**
  - **Efficiencies > 99%** even in the inter pixel regions

- By 2025 the **MONOLITH** ERC project will implement a 100% fill-factor gain layer (**PicoAD** patented sensor) to achieve **few picoseconds** resolutions in monolithic pixels
  - Results from first prototypes are very encouraging: the PicoAD works and shows gain as expected

Conclusions

1. The exquisite time resolution provided by SiGe BiCMOS enables construction of **very precise 4D trackers** and **particle-ID.**

2. Our sensors were **thinned to 60µm** (including electronics)
   $\Longrightarrow$ trackers can be built with **very little material.**

3. The monolithic technology is affordable and will allow **control of the costs** of very large-area detectors. Several large-volume foundries offer SiGe BiCMOS.

4. SiGe BiCMOS is **inherently radiation tolerant**, at least until $10^{14} n_{eq}/cm^2$. The MONOLITH project will explore radiation tolerance beyond that limit.

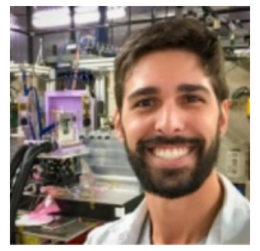
All the tiles seem to be in place to consider monolithic sensors with timing as **a key tool for FCCee trackers**

Silicon Team at UNIGE

Giuseppe Iacobucci
- project P.I.
- System design

Didier Ferrere
- System integration
- Laboratory test

Pierpaolo Valerio
- Lead chip design
- Digital electronics



Mateus Vicente
- System integration
- Laboratory test

Yana Gurimskaya
- Radiation tolerance
- Laboratory test

Yannick Favre
- Board design
- RO system

Théo Moretti
- Laboratory test

Antonio Picardi
- Chip design

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Sergio Gonzalez-Sevilla
- System integration
- Laboratory test

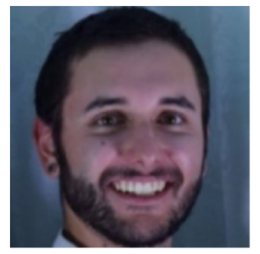
Magdalena Munker
- Sensor design
- Laboratory test

Roberto Cardella
- Sensor design
- Laboratory test

Fulvio Martinelli
- Chip design

Stéphane Débieux
- Board design
- RO system

Chiara Magliocca
- Laboratory test



Matteo Milanesio
- Laboratory test

Main research partners:

Roberto Cardarelli
INFN Rome Tor Vergata

Holger Rücker
IHP Mikroelektronik

Marzio Nessi
CERN & UNIGE

Mehmet Kaynak
IHP Mikroelektronik

Ivan Peric
KIT

Bernd Heinemann
IHP Mikroelektronik

Funded by:

FNSNF Swiss National Science Foundation

European Research Council (erc) – Established by the European Commission

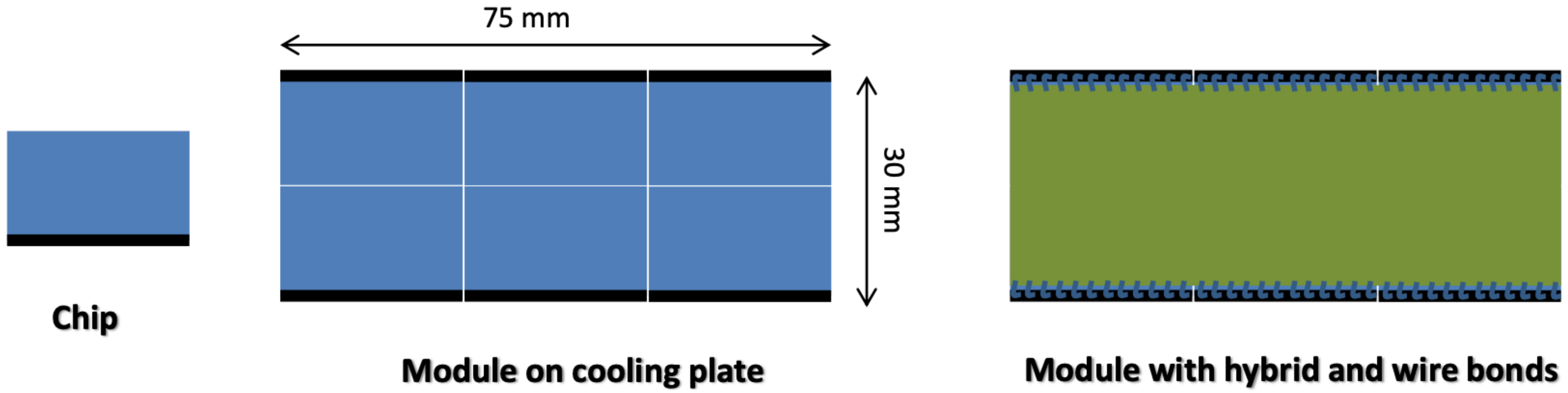
FNSNF Sinergia

ATTRACT

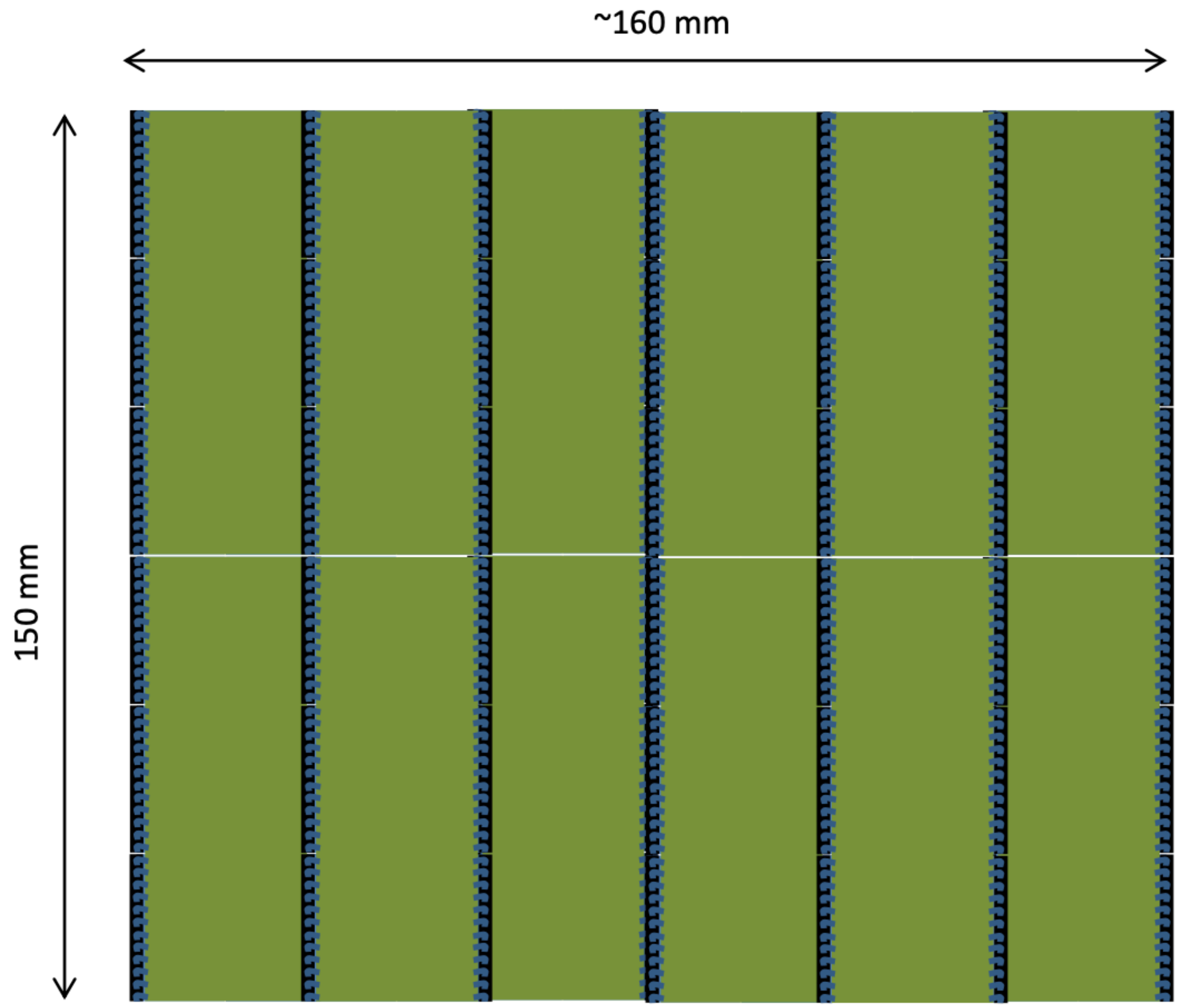
Université de Genève UNITEC

Extra Material

FASER preshower: module and plane layout and power



Plane: 6x2 modules



Superpixel = 16x16 =	256 pixels
Column = 8 superpixels =	2’048 pixels
Chip = 13 columns =	26’624 pixels
Module = 2x3 = 6 chips =	159’744 pixels
Plane = 2x6 = 12 modules =	1’916’928 pixels
Pre-shower = 6 planes =	11’501’568 pixels

- 2x6=12 modules/plane
- Power/plane = 48W
- Total pre-shower power = 288 W

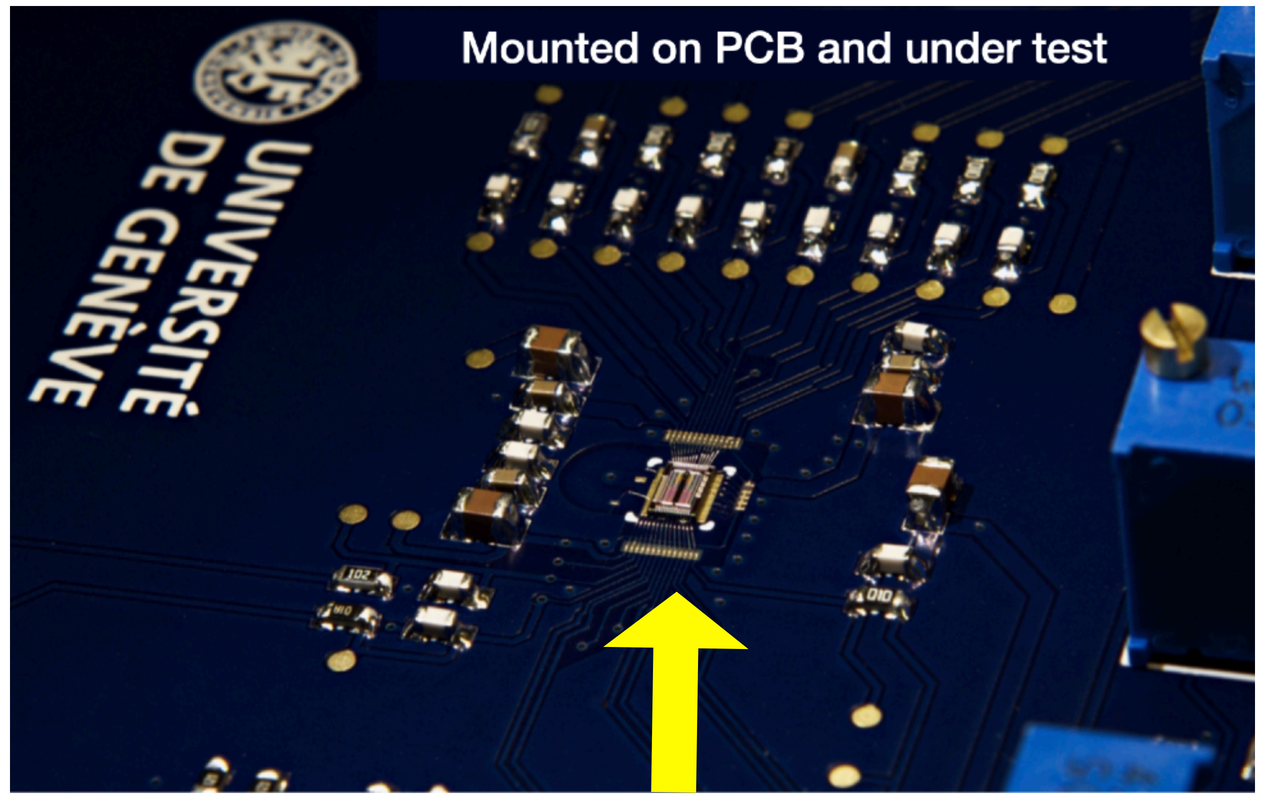
Module Power

Power	Voltage [V]	Current [A]	Regulator On PP	Power [W] including 20% from regulator
Analog	1.2	1.2	Yes	1.7
Digital	1.2	0.9	Yes	1.3
Driver	0.9	0.9	yes	1

Max total module power: 4 W

1. The FASER high-resolution W-Si preshower

Small-size FASER preshower prototype

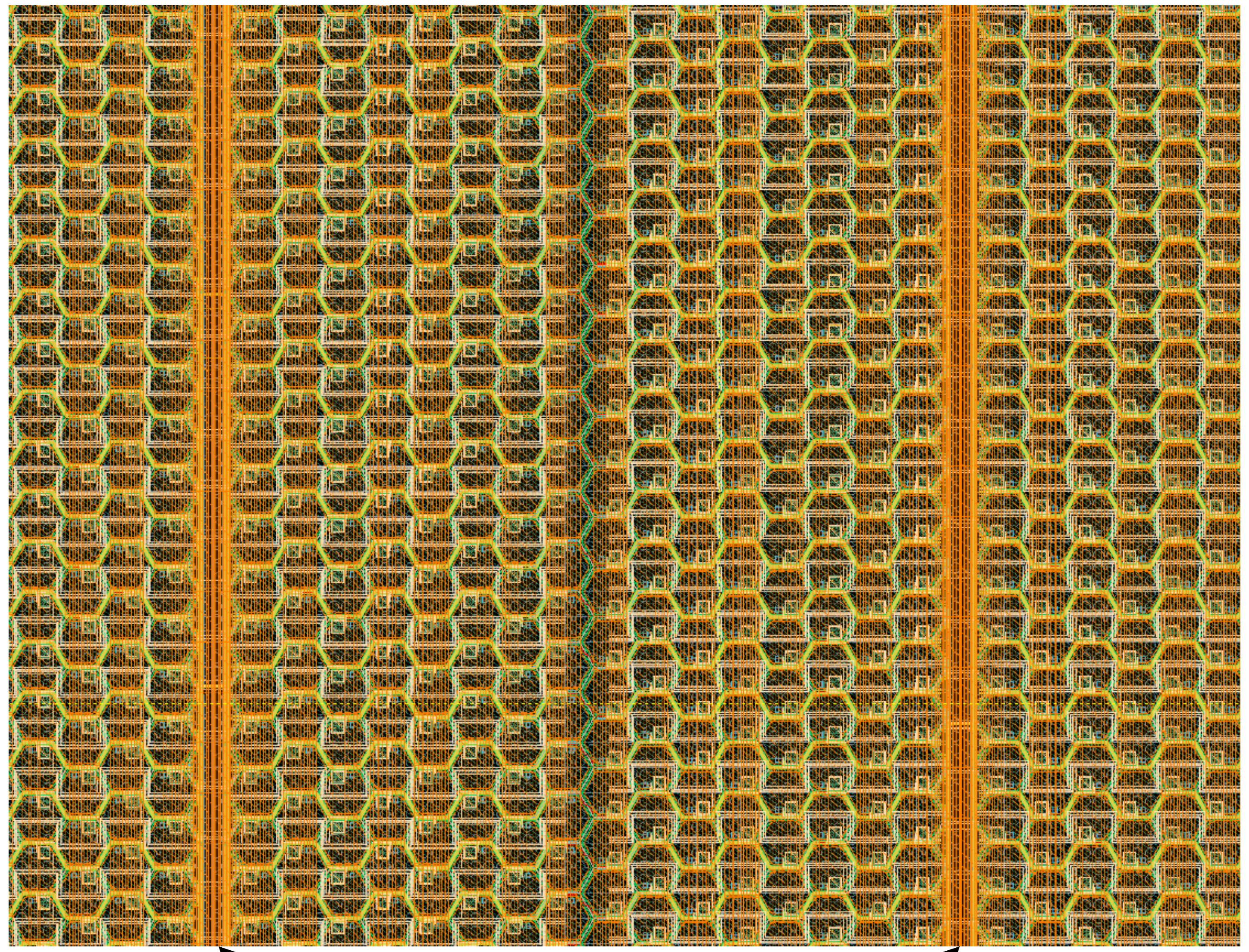


Prototype contains basic building blocks of final chip.
Studies ongoing on:

- Pixel noise level
- Front-end implementation
- Cross-talk for target pixel area
- Performance (power consumption etc.)

Engineering run with **full-column prototype chips** submitted **on June 29th**

UNIGE design in collaboration with KIT

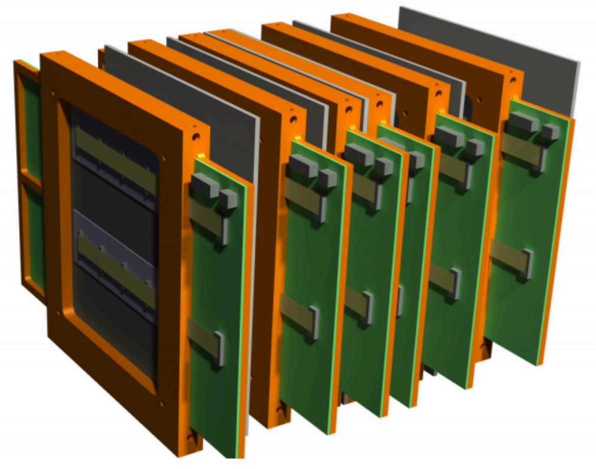


digital routing
of super-pixels

1/17 = 6% dead area

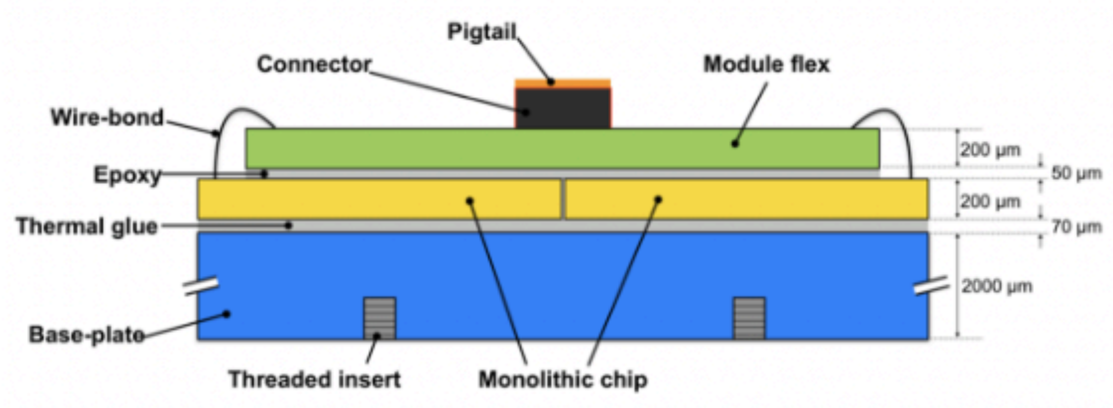
- Monolithic ASIC in **130nm SiGe BiCMOS** process by IHP
- Reticle size: 1.5×2.5cm^2
- Pixel size: hexagonal pixels, 65μm side
- Local analog memories to store the charge
- Ultra-fast readout with no digital memory on-chip to minimise the dead area
- In between an imaging chip and an HEP-detector chip

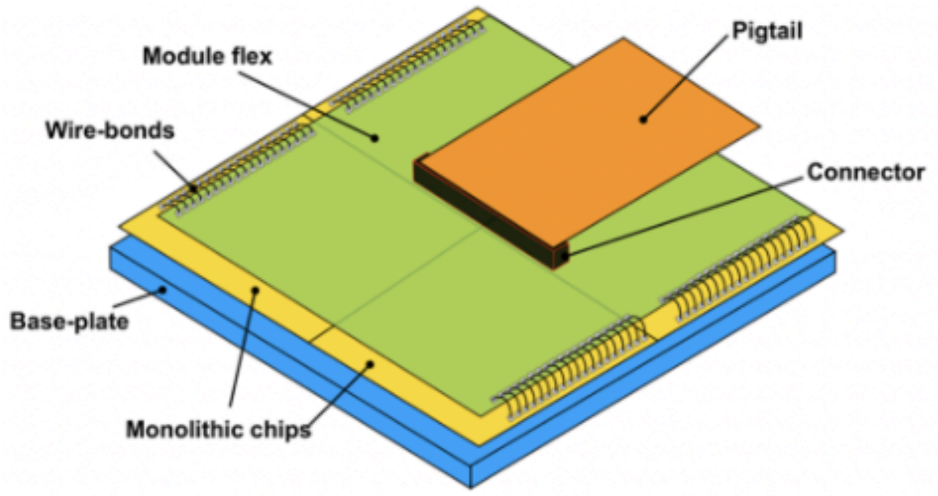
1. The FASER high-resolution W-Si preshower

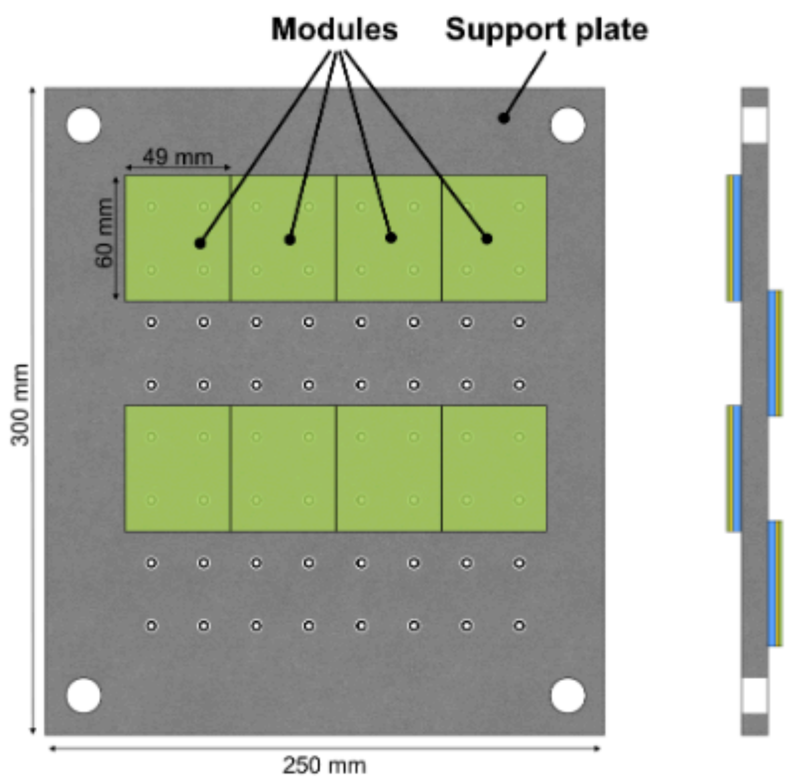


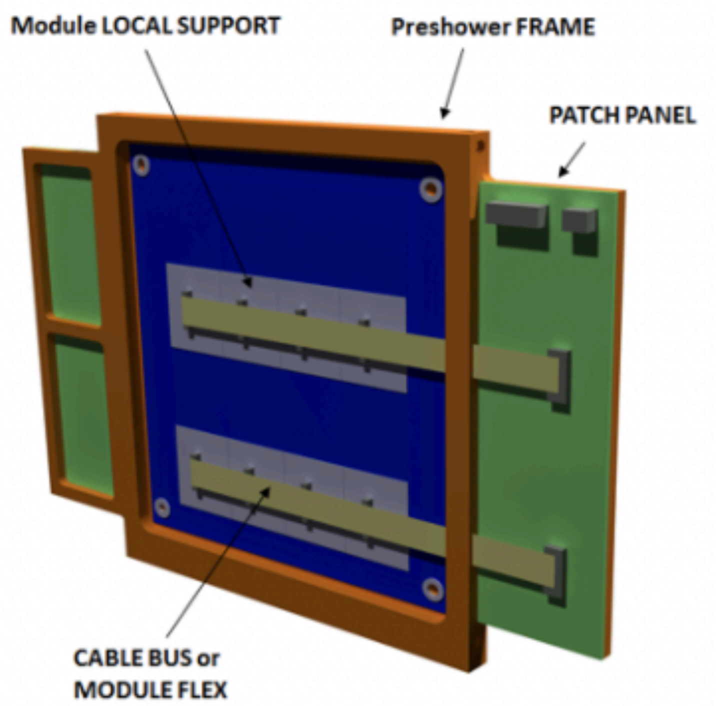
Several layouts studied prior to the funding request.
Chosen baseline:

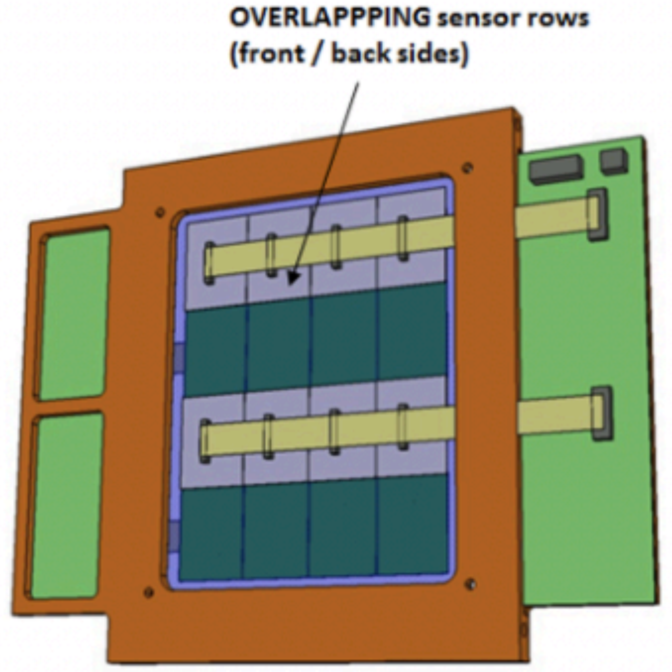
6 planes of $1X_0$ tungsten + monolithic silicon sensors pitch 100μm pitch

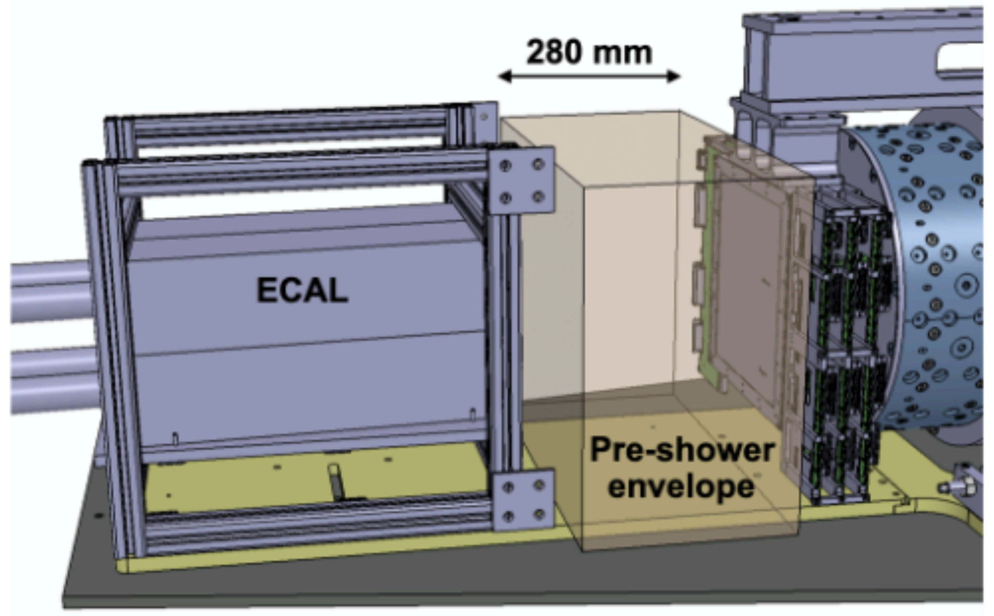


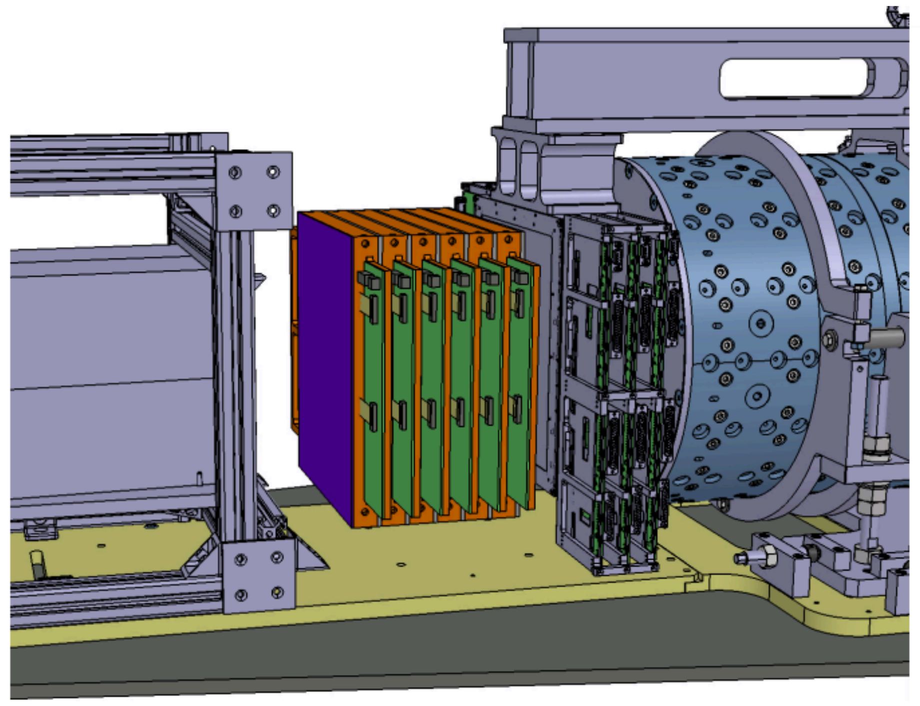






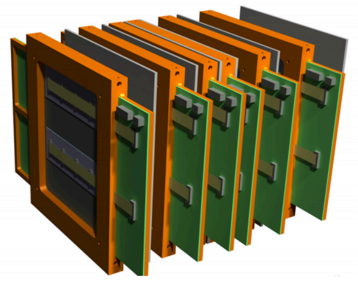






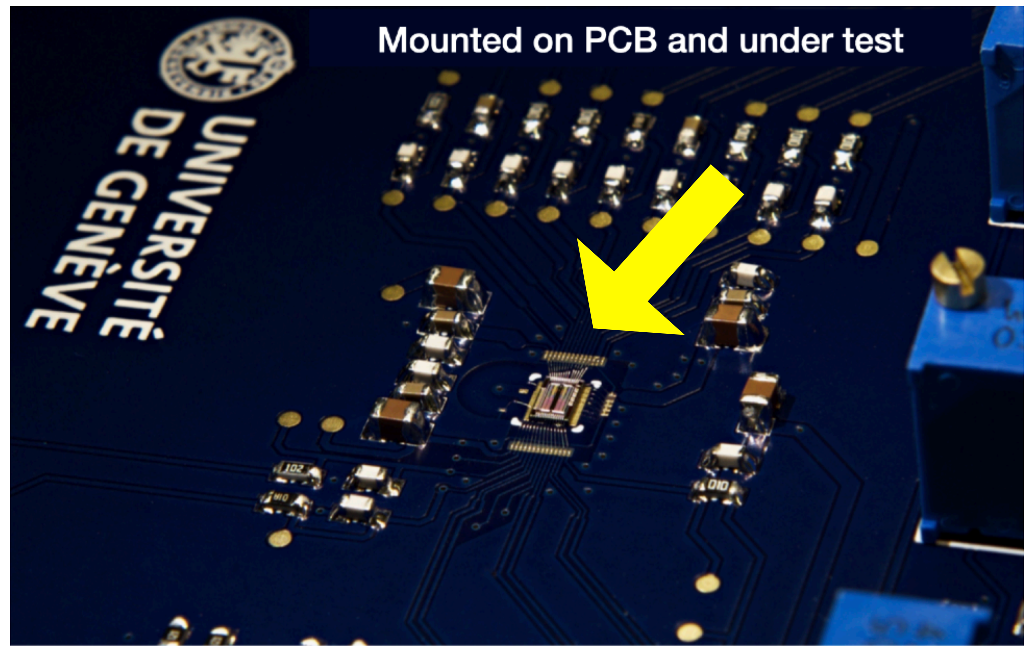
The new pre-shower will fit in the present volume between the tracker and the calorimeter.
Space available (28 cm (detector length: 24.6 cm)

1. The FASER high-resolution W-Si preshower



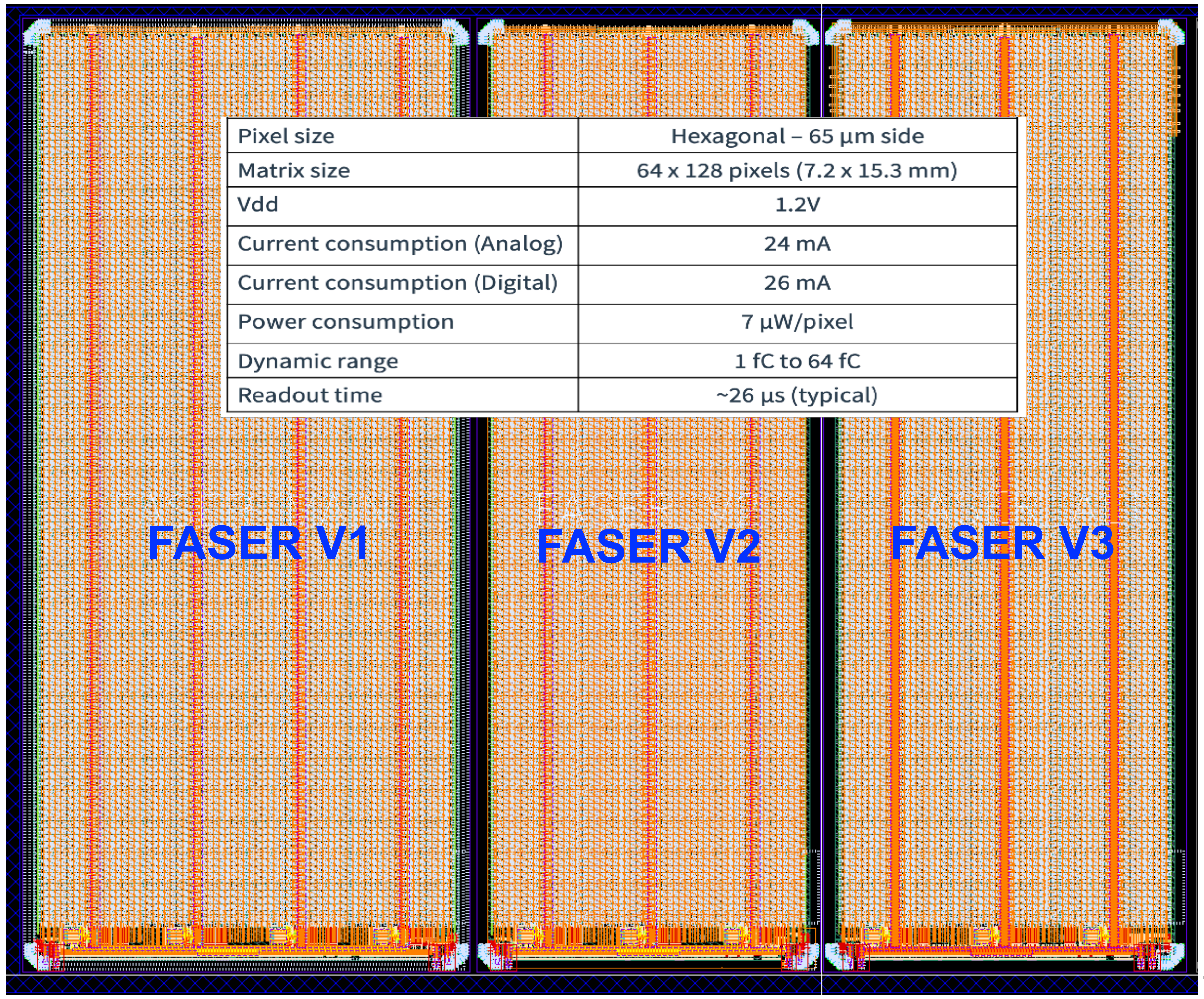
- Tests of the small-size FASER prototype ASIC completed with good results:
  - FE electronics integrated in pixel works as expected (and implemented in the large-size prototype)
  - No cross talk observed

Small-size FASER preshower prototype



- **Full-reticle preproduction chip submitted in June**
  - In IHP 130nm SiGe BiCMOS process
  - Total area: 2.0 x 1.5 cm^2
  - Chip divided in «supercolumns» (16x128 pixels) with a ~40μm slice of digital logic in between
  - Three matrices with different flavours:
    - ➡ FASER V1: 4 supercolumns, baseline design with FADC for TOT
    - ➡ FASER V2: 3 supercolumns with FADC and BJT discriminators to reduce pixel-to-pixel mismatch
    - ➡ FASER V3: 3 supercolumns with digital-logic counters for the TOT (more conventional but triple dead area)
- Huge dynamics range: 1fC to 64 fC
- These chips will be used to build prototype modules.

Full-reticle FASER preproduction chip



Pixel size	Hexagonal – 65 μm side
Matrix size	64 x 128 pixels (7.2 x 15.3 mm)
Vdd	1.2V
Current consumption (Analog)	24 mA
Current consumption (Digital)	26 mA
Power consumption	7 μW/pixel
Dynamic range	1 fC to 64 fC
Readout time	~26 μs (typical)