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Vitis accelerator backend development for HLS4ML

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Leveraging the current industry shift towards heterogeneous computing and the widespread adoption of FPGAs as accelerators to deploy machine learning algorithms, this project introduces the Vitis accelerator backend, a novel backend for HLS4ML. HLS4ML is a python package tailored for machine learning inference on FGPAs that translates traditional open-source machine learning package models into High-Level Synthesis (HLS) language. Vitis accelerator backend streamlines the creation of firmware implementations of machine learning algorithms using HLS and Vitis kernel acceleration flow, with a focus on automating project generation specifically for PCIe FPGA accelerators.

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