Overview of the Preliminary Data Transmission Chain Prototype for the Upgrade of the ATLAS ITk Pixel Detector for HL-LHC

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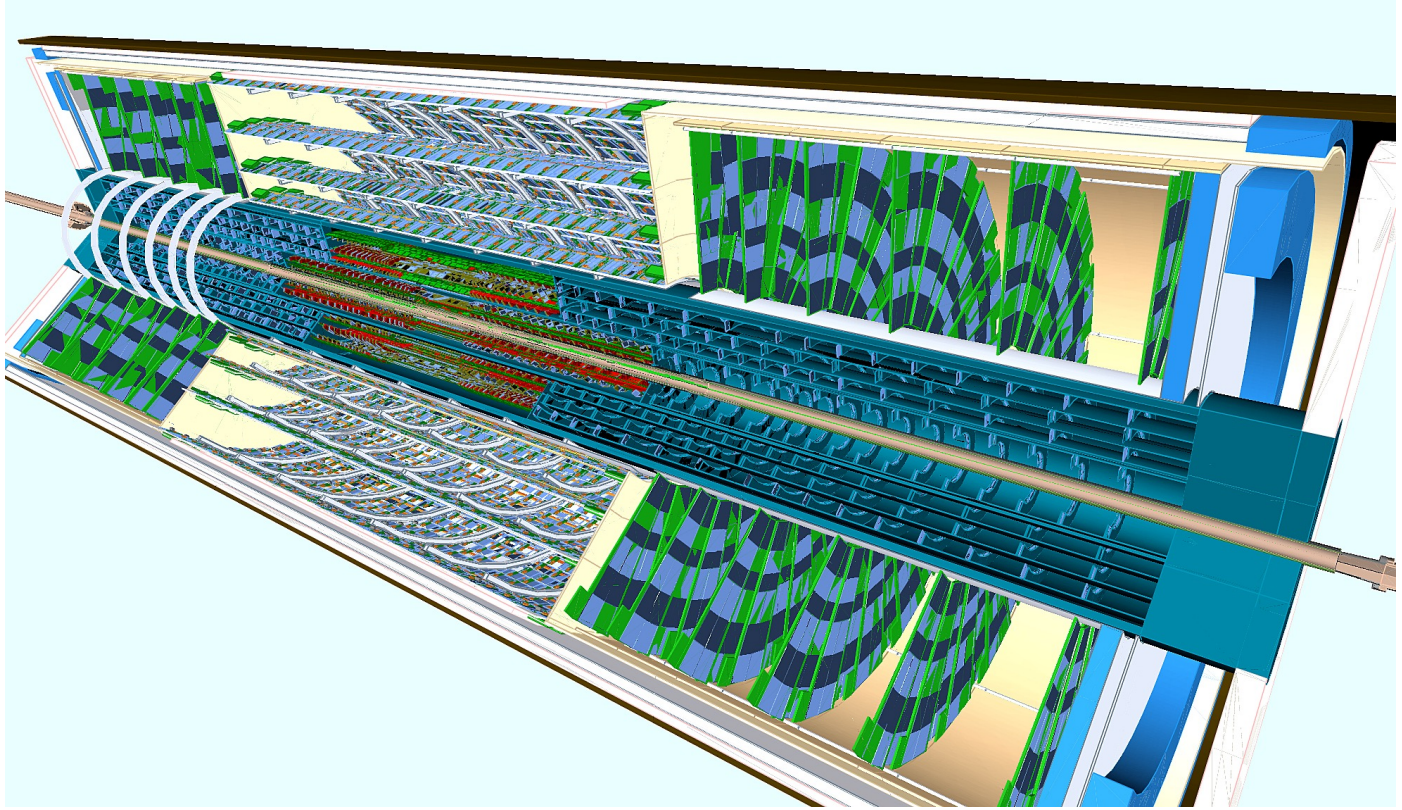
ATLAS
EXPERIMENT

Motivation: Upgrade of ATLAS ITk Pixel Detector for HL-LHC



HL-LHC expected performance:

- $\sqrt{s} = 14\ TeV$
- Instantaneous luminosity $L \sim 5x10^{34} cm^{-2} s^{-1}\ to\ 7.5x10^{34} cm^{-2} s^{-1}$
- Avg. interaction/bunch crossing = 200

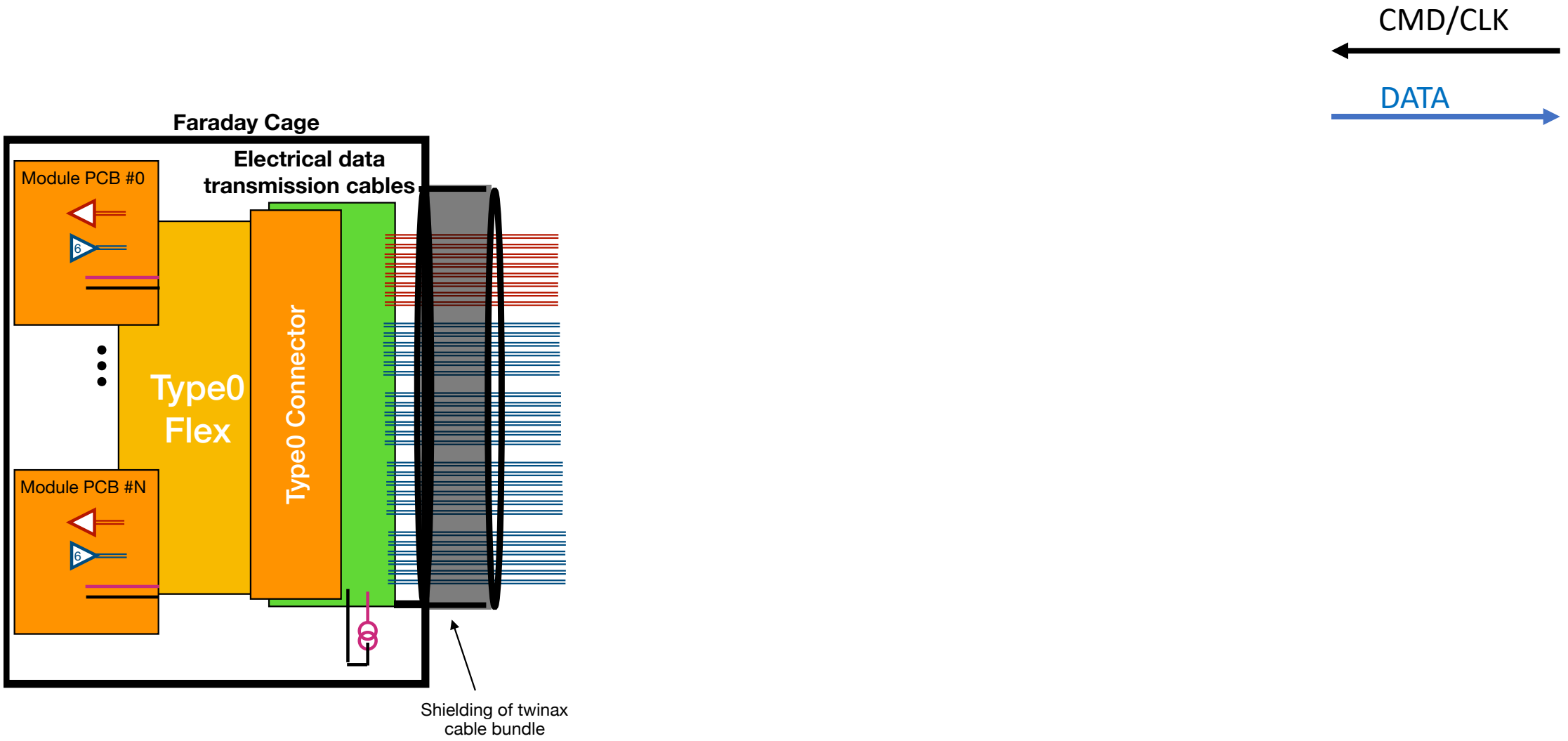
Some Detector challenges:

- Higher particle fluxes, larger event sizes
  - readout limitations
- Increasing fluences, close to beam pipe up to 10^{16} n_{eq} /cm^{-2}
  - increased radiation damage

New Inner Tracking Detector ITk: Strips and Pixels to meet the HL-LHC challenges with higher bandwidth and higher radiation hardness

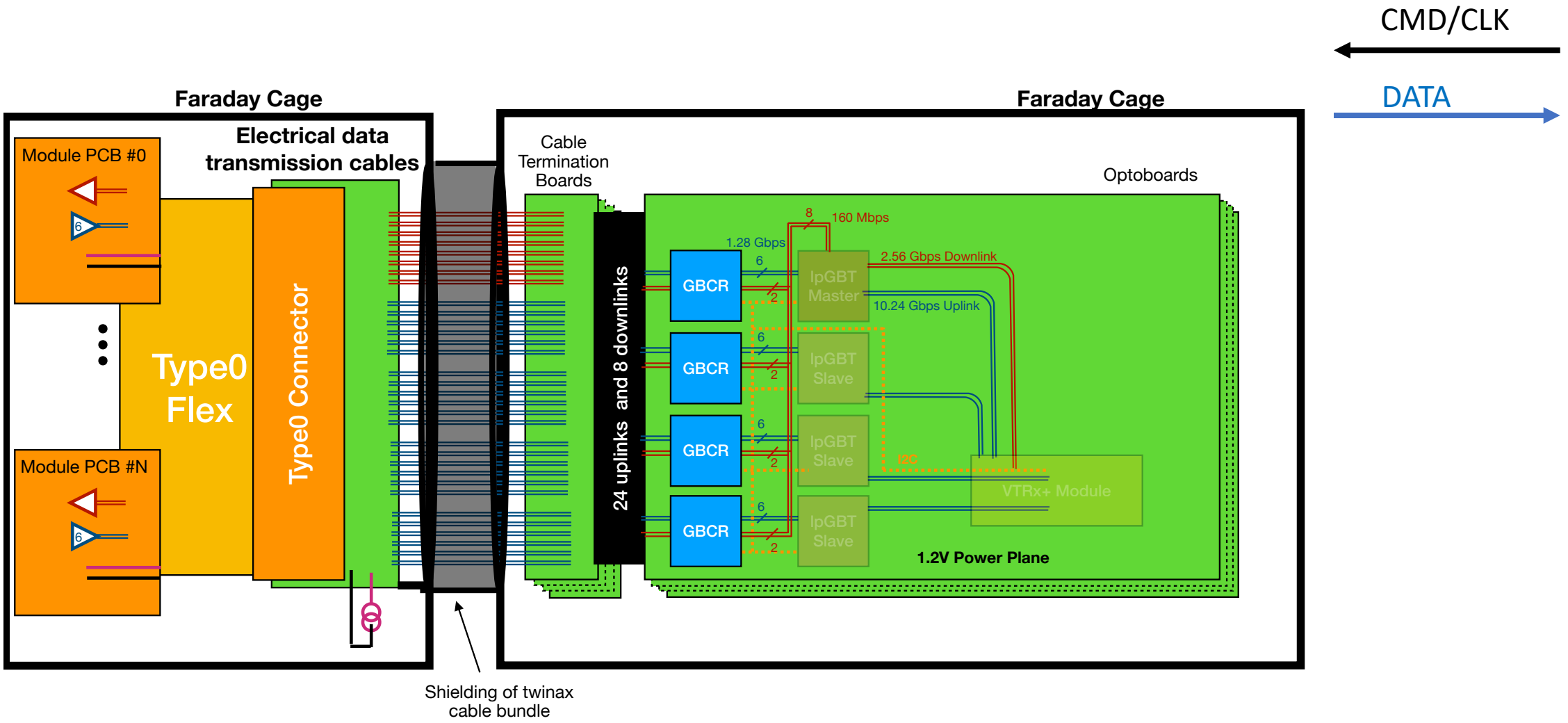
- Strips: 4 barrels and 6 disks
- Pixel: 5 flat barrels at small η, inclined layout at intermediate η, and ring geometry at large η (closest to beam pipe)

The envisioned ITk Pixel data transmission chain



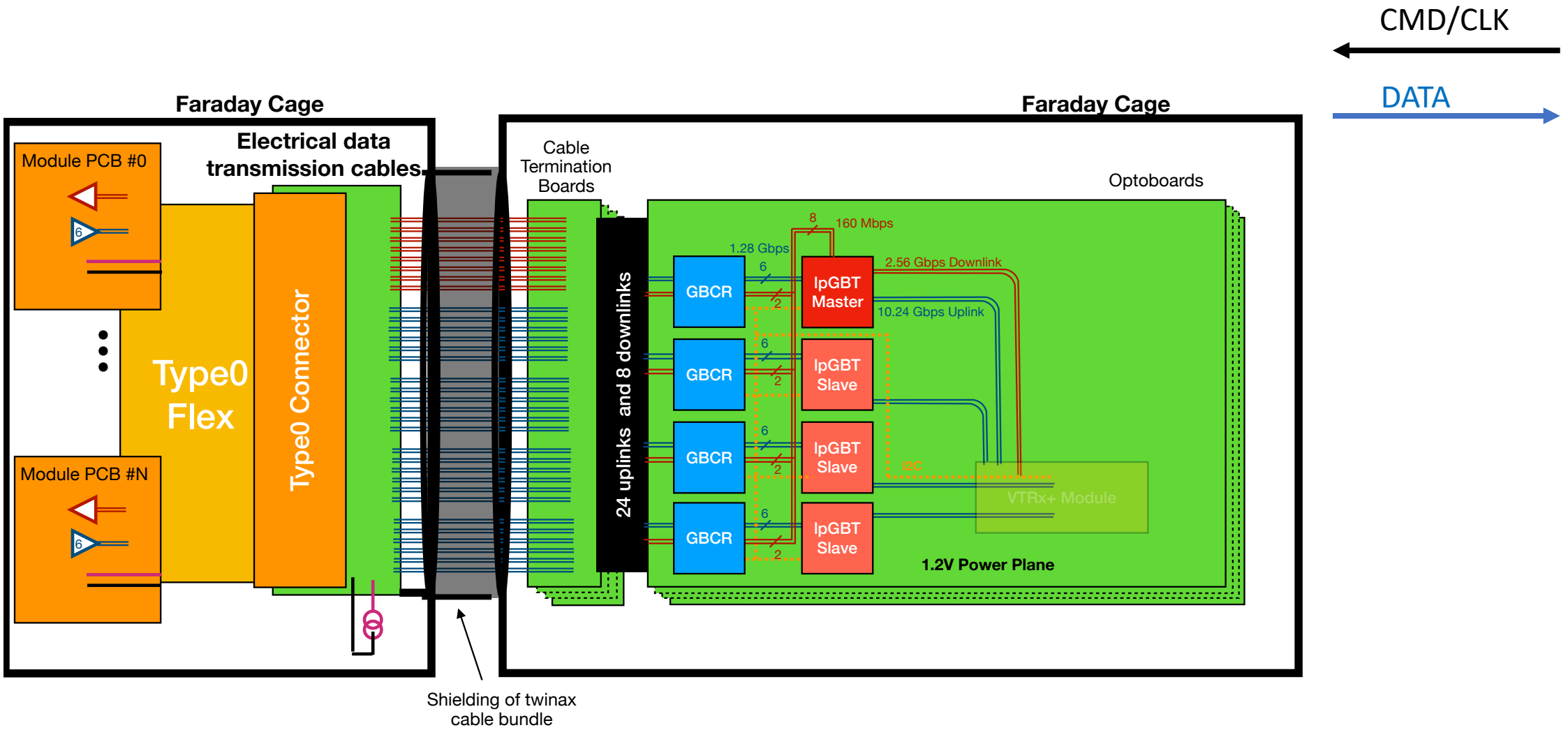
Modules of the ITk Pixel send signals and receive trigger and commands through electrical cables called Flex and twinaxes.

The envisioned ITk Pixel data transmission chain



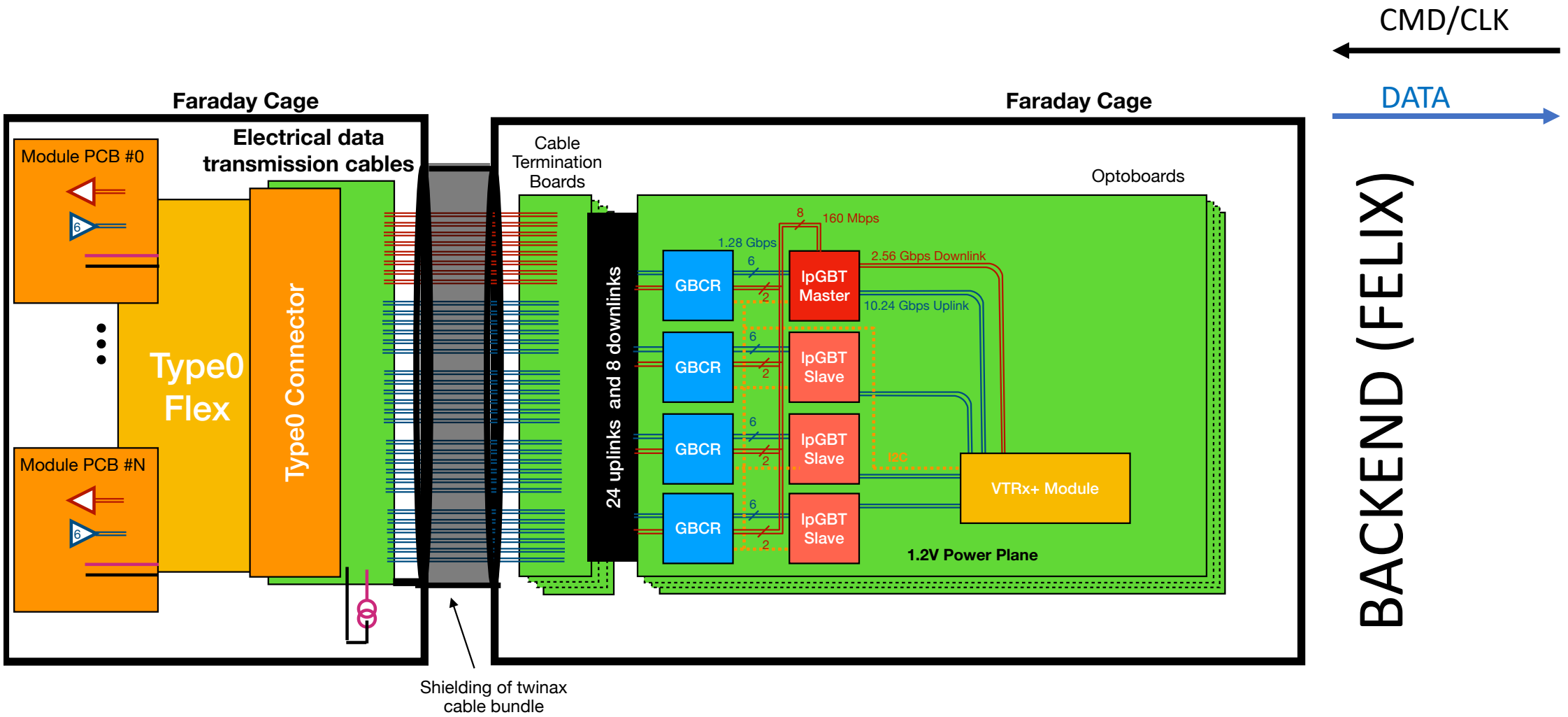
On the optoboard the data cables are terminated by Gigabit Cable Receivers (GBCRs) - that equalize the received signals from the modules to compensate any signal losses.

The envisioned ITk Pixel data transmission chain



- The data lines are aggregated into faster links by the Low Power Gigabit Transceivers (lpGBTs). Six 1.28 Gbps lanes are aggregated into one 10.24 Gbps lane.
- The CMD is received by one of the (lpGBT) “master” and split to a maximum of 8 downlinks running at 160 Mbps to the Front-End chips.

The envisioned ITk Pixel data transmission chain

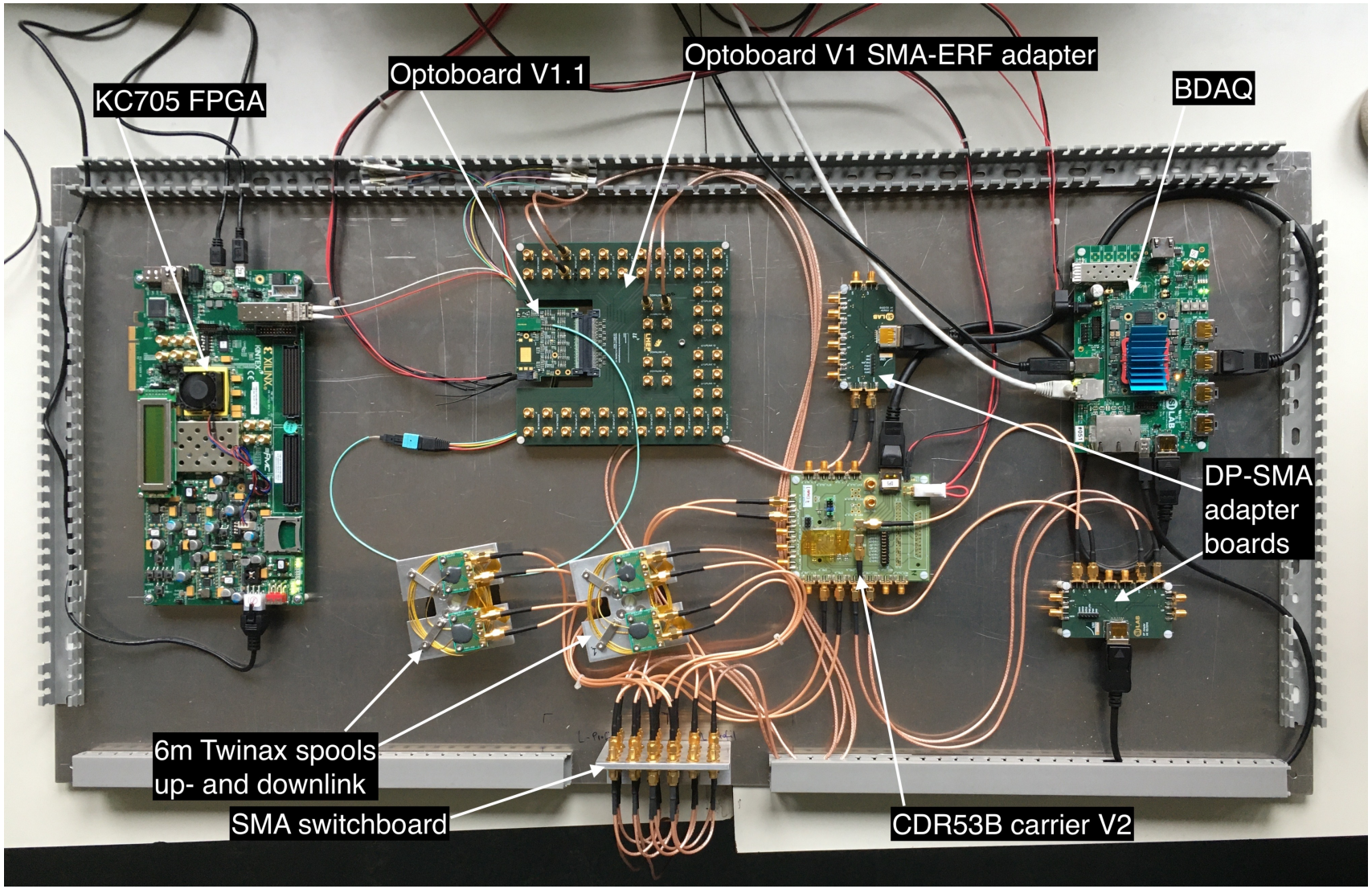


The Versatile Link - VTRx+ converts the electrical signal into optical signal. The optical signals are sent to the readout electronics (FELIX) from the optoboards.

Great expectations from the transmission chain on the uplink

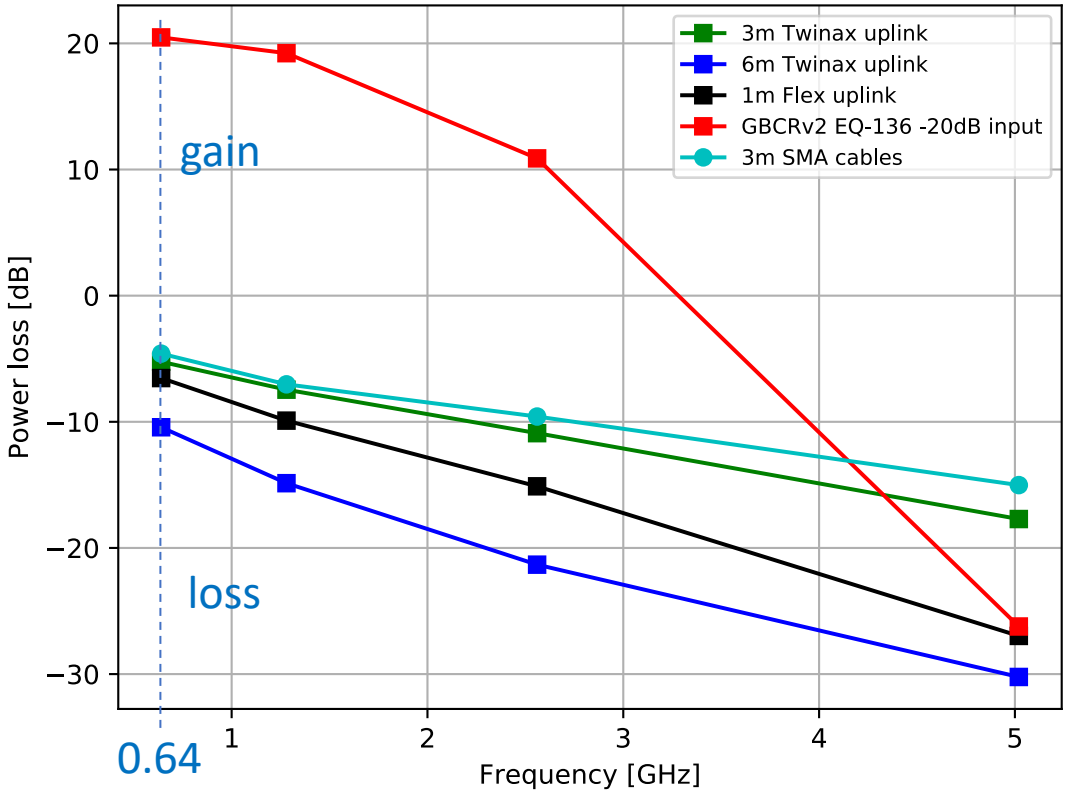
- The loss in electrical signal on the chain from module to backend (uplink) should be < 20 dB for data rate of 1.28 Gbps per channel. There are ~ > 4000 data channels
- The noise to the signal (total jitter) should be ideally < 100 ps entering the lpGBT to be aggregated
- The number of acceptable wrong bits (bit error ratio – BER) should be < 10^{-12} bits

The Preliminary Data Transmission Chain Prototype at Bern



Step 1: Any losses on the uplink?

Electrical signal loss of each component



Total loss in chain at 0.64 GHz w/o SMA cables ~ -17 dB, w/ SMA cables ~ -23 dB before GBCR.

The GBCR has a gain of ~ 20 dB for a input signal w/ -20 dB input signal. **So GBCR recovers the losses!**

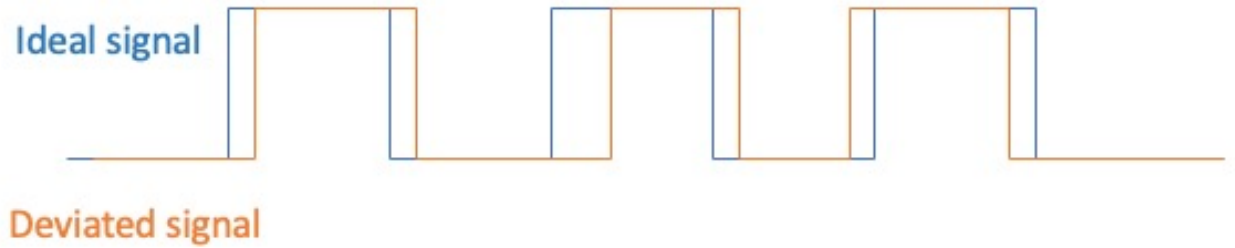
Step 2: What are Bit error ratio and jitter tests?

Bit error ratio (BER) test

- Electrical signal is read out in binary i.e. 1s and 0s
- Pseudo-random bit sequences tested (so we know the expected total no. of bits)

wrong bits / total no. of Bits

Jitter test



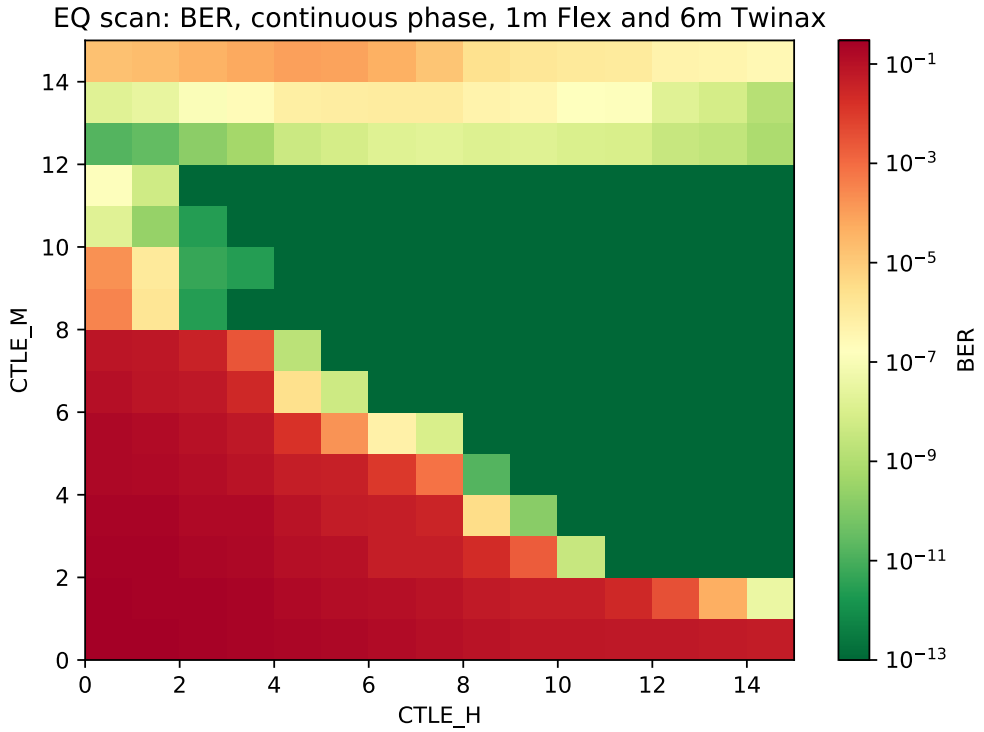
Actual deviation from the ideal clock period over all clock periods

Usually, jitter and BER correlate

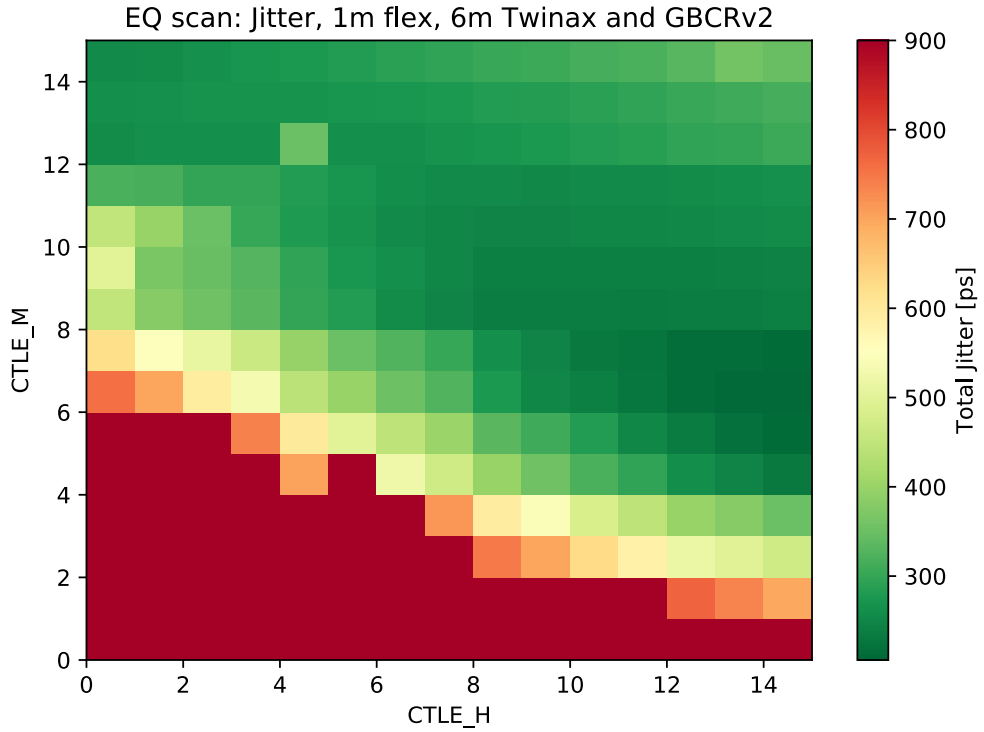
Step 2: BER and jitter tests on the uplink

Entire chain with GBCRv2 in Equaliser mode

Bit error ratio test:



Jitter test:

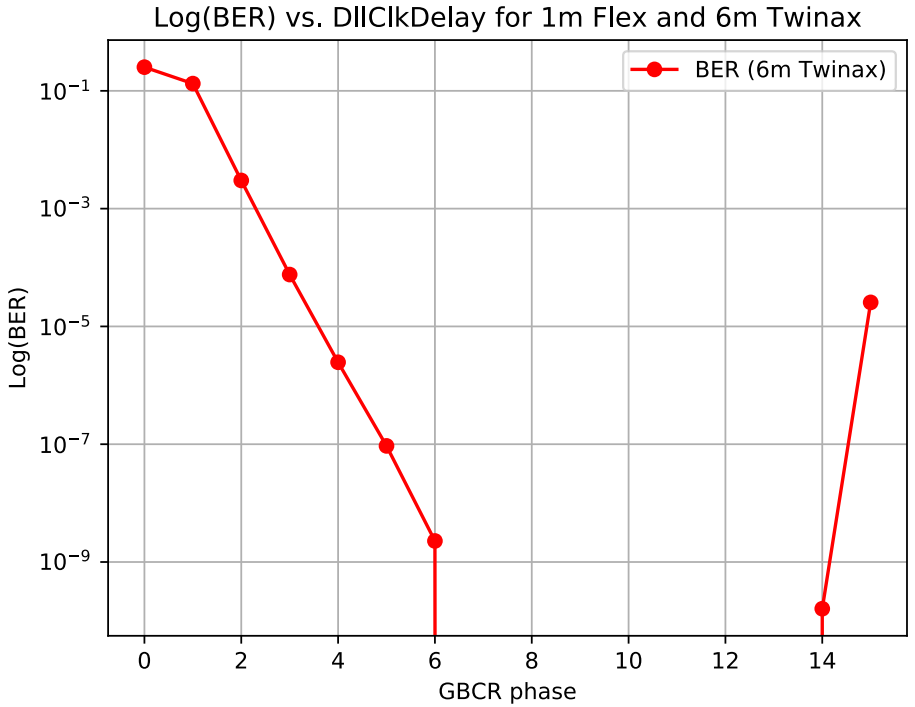


- Jitter and BER correlate
- BER for certain configurations of the devices is $<10^{-12}$ (dark green areas)

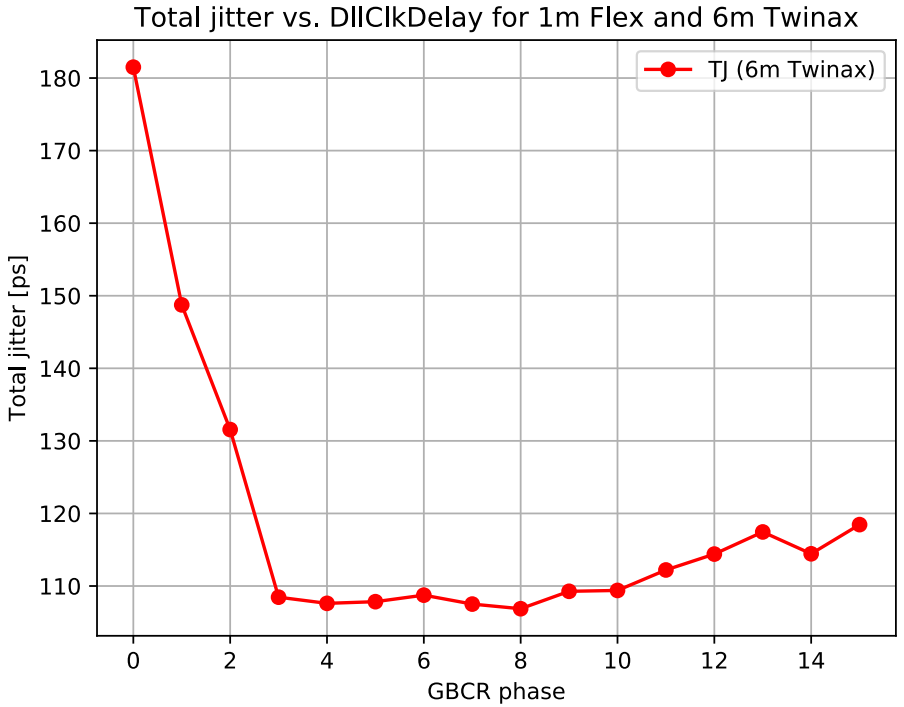
Step 2: BER and jitter tests on the uplink

Entire chain with GBCRv2 in retiming mode

Bit error ratio test:



Jitter test



- In the Retiming mode (i.e. additional clock fed to GBCR from lpGBT aside from recovered clock from data)
- For the right phase alignment of data with GBCR and lpGBT we get jitter ~ 100 ps

And finally …

Are we able to meet the requirements?

- The loss in electrical signal on the uplink < 20 dB
- The total jitter is ~ 100 ps in the retiming mode
- The bit error ratio < 10^{-12} bits in most configurations

We have a ROBUST chain :D

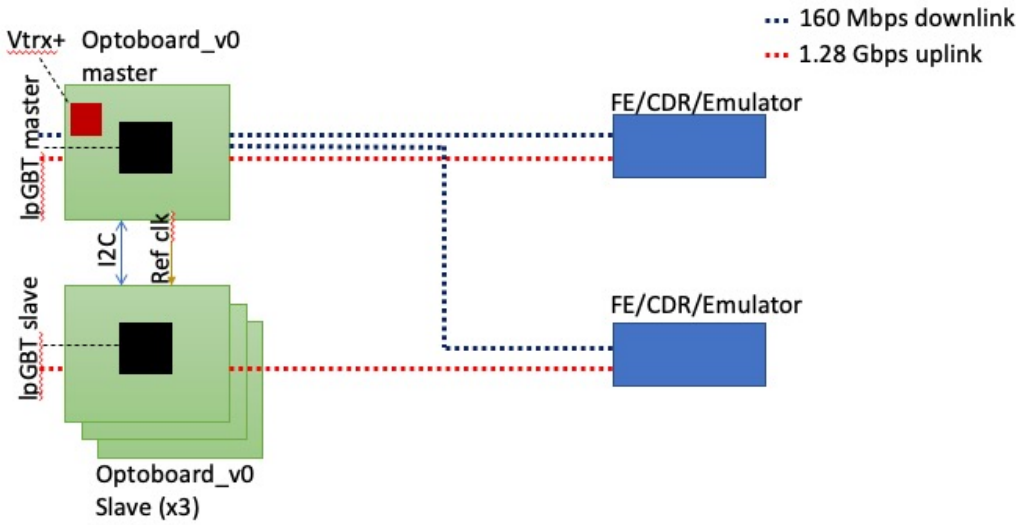
What to look forward to?

- Irradiation campaigns to irradiate all the cables and components on the optoboard (You might have seen Lea Halser's poster with information on the Bern Cyclotron and Irradiation)
- Final version of the optoboard (optoboard v2) to be tested and approved in the Final Design Review
- Integration in the data transmission chain of all the real components - specifically the readout card and the readout chip, to prove the final design in progress (You might have seen Roman Müller's poster with more information on the Opto-system and incorporation of more real components)

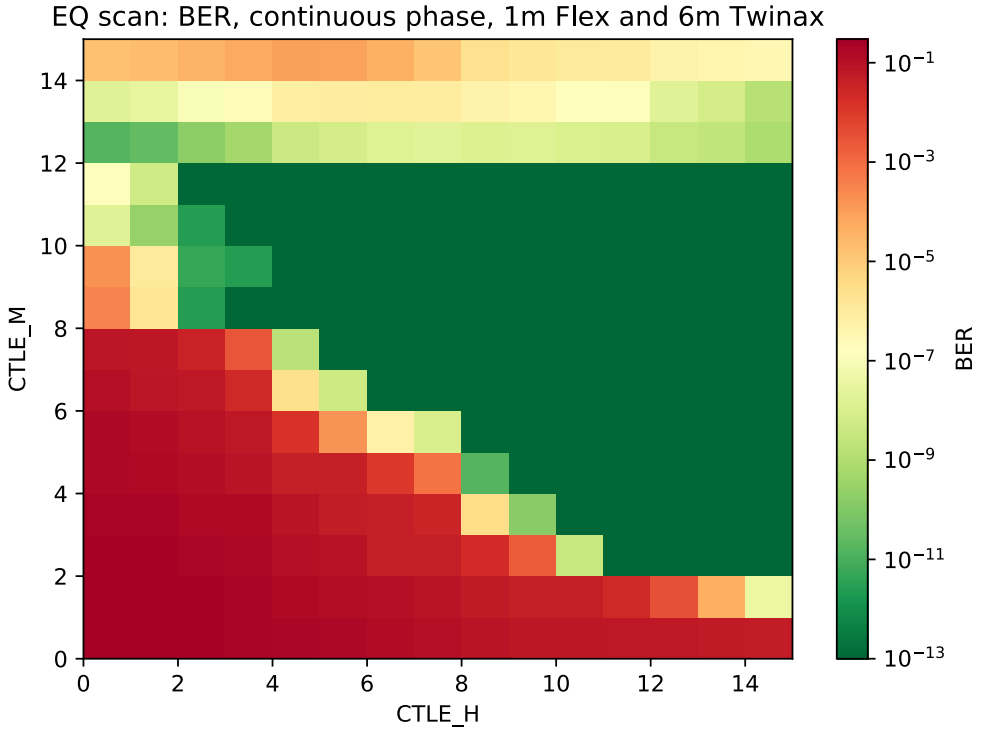
Back-up

Results

Schematics of Bit error ratio test chain



The Bit error ratio test



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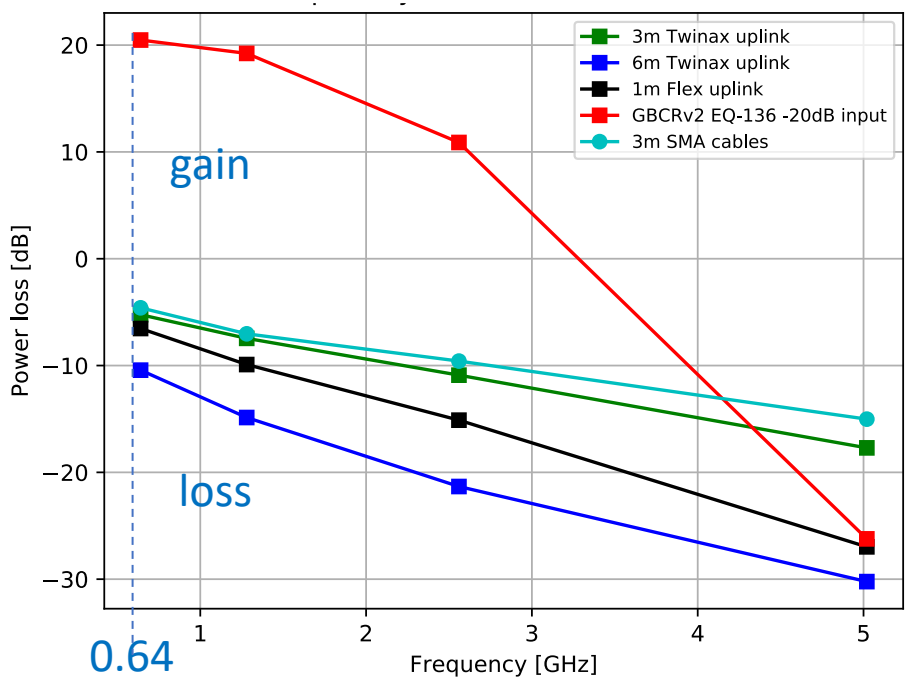
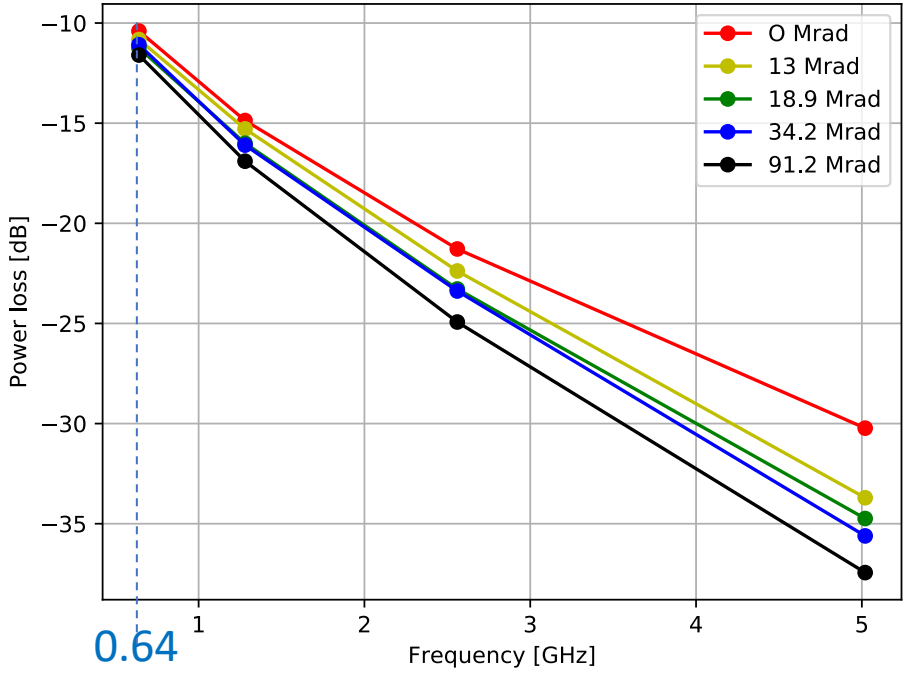


Total loss in chain at 0.64 GHz w/o SMA cables ~ -17 dB, w/ SMA cables ~ -23 dB before GBCR. The GBCR has a gain of ~ 20 dB for a input signal w/ -20 dB input signal.
So GBCR recovers the losses!

Electrical signal loss of 6m twinax at different initial irradiation steps



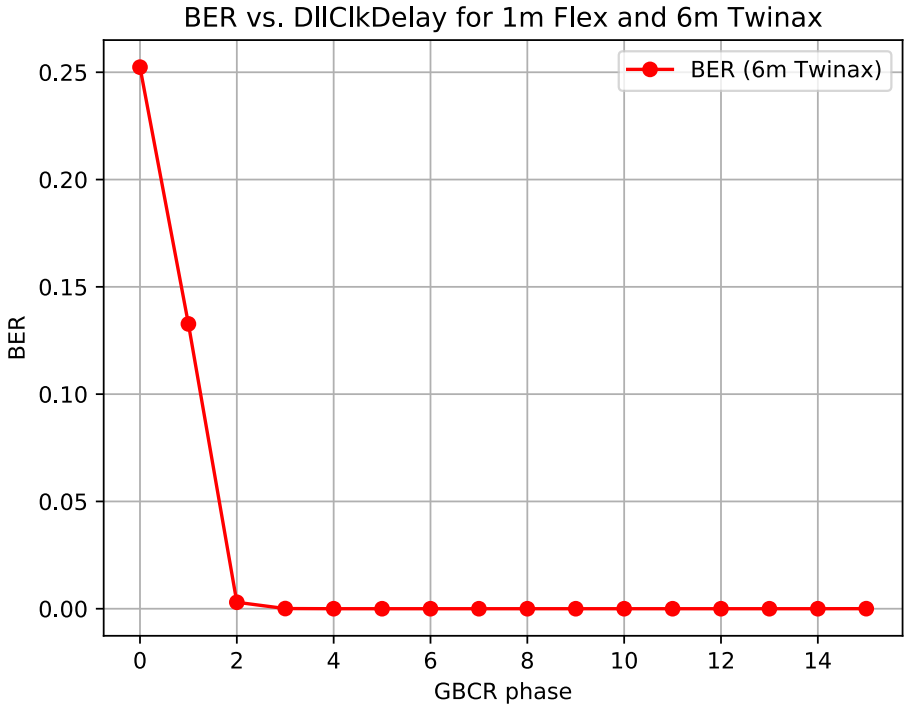
- For 0.64 GHz, the power loss is very small < 1dB comparing 13 MRad to 91.2 Mrad
- At higher frequencies, the power loss is more, and signal attenuates faster especially at higher irradiation doses

Signal loss increases with irradiation and data frequency

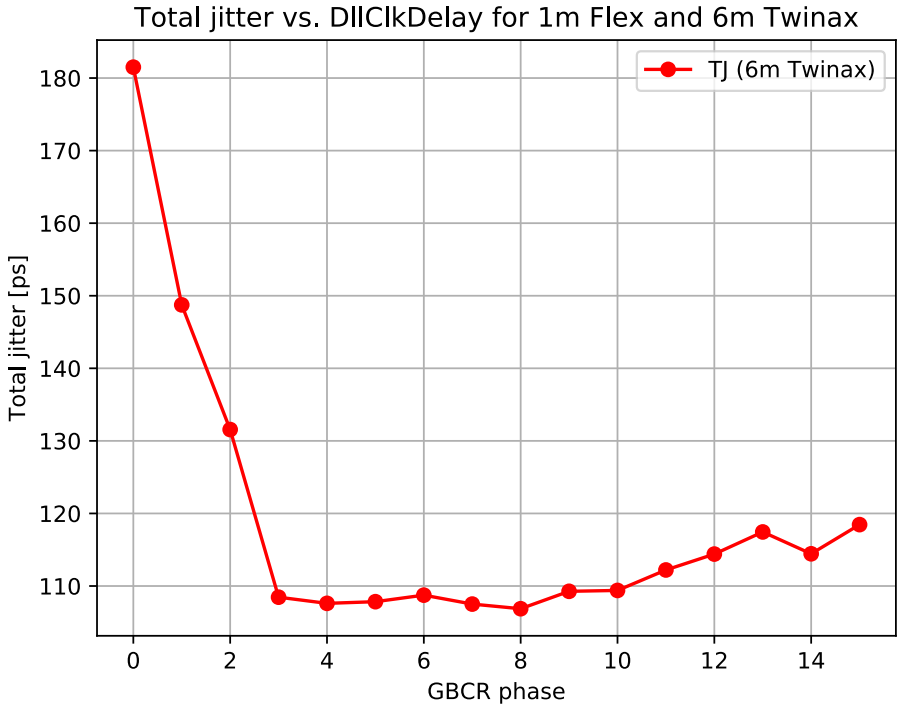
Step 2: BER and jitter tests on the uplink

Entire chain with GBCRv2 in retiming mode

Bit error ratio test:



Jitter test

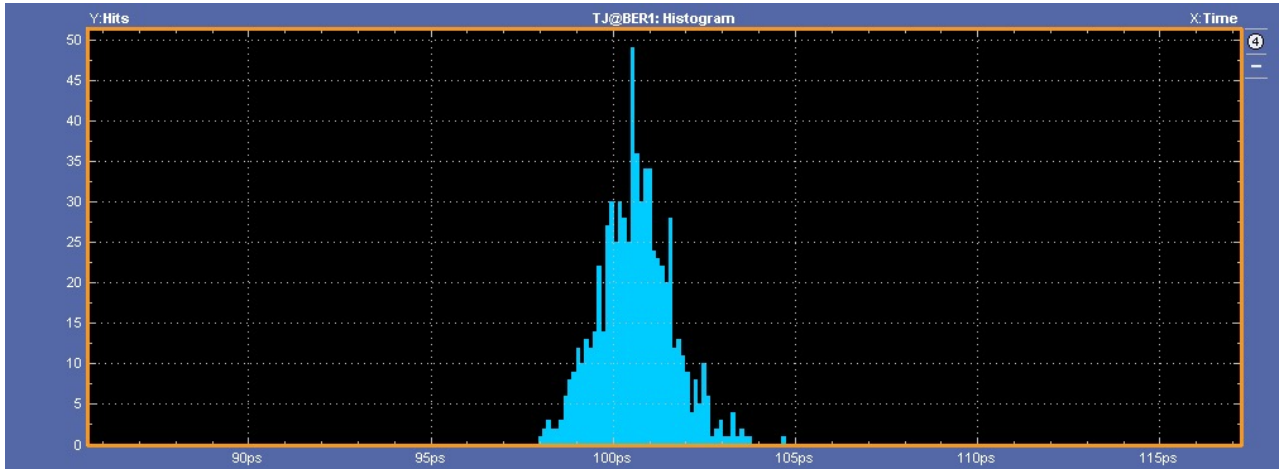


- In the Retiming mode (i.e. additional clock fed to GBCR from lpGBT aside from recovered clock from data)
- For the right phase alignment of data with GBCR and lpGBT we get jitter ~ 100 ps

Understanding the jitter tool

Total Jitter and Eye

TJ@BER is the convolution of the random and deterministic jitter at a specific BER.



Eye diagram show Bit and his friends arriving serially – separating the 1s and the 0s to see an open eye. The more open – the better ☺