Universidade do Minho
Departamento de Física

MAP-FIS REPORT

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Relatório de Tese, Doutoramento em Física (MAP-Fis)

Trabalho a ser efetuado sobre a orientação de Professor João Pedro Alpuim (UM/INL), Jérôme Borme (INL) e Bruno Costa (ICVS/UM)

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Summary

This year (2021) I have completed the following tasks of my work plan: (i) selection of the DNA sequences for biorecognition of each of the biomarkers for brain cancer that will be used in the subsequent phases of the work. This choice was based on an extensive literature review; (ii) During the same period, I optimized the manufacturing process in a clean room for graphene field effect transistors, which will be the basic devices for the sensors that it proposes to develop in my doctoral thesis. After this step, I successfully manufactured a 200 mm wafer with graphene sensors, a highly complex process that requires advanced knowledge in operating multiple tools and equipment in a clean room. The next stage of my work plan, which will occupy the second year, consists of the functionalization of the newly manufactured graphene transistors with synthetic DNA probes, with the sequences selected in the previous stage. All probes will be tested against their complementary sequences and also against sequences showing one or more nucleotide polymorphisms. In the third year of work, calibration curves will be established, as well as the detection limits and the dynamic range of the sensors. The last step, already close to the main objective of the thesis of providing an economical alternative for the diagnosis of brain tumors, is to test the sensors with DNA extracted from surgically resected brain tumor tissue and compare with the results of DNA extracted from blood and samples of plasma and unprocessed blood.

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1.1 Experimental Procedures

1.1.1 CAD design of graphene EGFETs

The graphene electrolyte-gated field effect transistor (EGFET) was designed using AutoCad 2020 software. The design involves a wafer with 1764 graphene chips, each with 20 individual sensors, 10 of which share the same source but different drains and the other 10 share another source and again drains always different (Figure 1.a), thus providing a mirror appearance. A receded gate (area comprised within the red lines) was included in the spaced design of the current lines with a large area to further increase the contact between the electrolyte drop and the gate and provide an even distribution of the potential within the drop of water and a very uniform gating field.

The area committed by the graphene channel (area comprised within the orange lines) in each transistor is 1875 µm2, having a length of 25 µm and a width of 75 µm. Large gold pads were designed to facilitate the process of bonding the aluminum wire to the PCB. These gold pads were only designed on two sides of the chip to facilitate their characterization with the aid of an automatic probe station that allows us to measure the graphene resistance at the end of the process in order to check which sensors are good to use.

a. b.

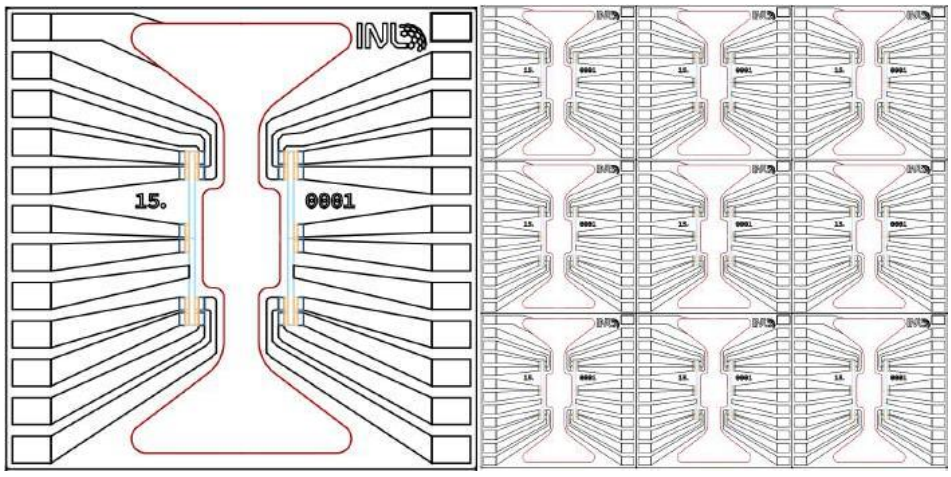


Figure 1- CAD design of the graphene EGFET.

a. Source and drain current lines are marked in blue (dark blue for drain and white blue for source), whereas the gate electrode is represented in red, and orange lines represent the graphene channels to ease sensor design comprehension. b. A die with 9 chips is shown, indicating the relative distribution of chips along the wafer.

1.1.2 Fabrication at wafer scale - overview

Figure 2 represents the resume of the process that have the main goal to develop a process for the wafer-scale fabrication of high electronic quality devices for biosensing applications. The final devices produced at the 200 mm wafer scale are resistant to all the solvents used for graphene functionalization and have low ion permeability, which increases their electrical stability. After the previous study, in which each step of the fabrication process is optimized using small area substrates, a complete microfabrication process is performed on a 200 mm Si wafer covered with 100 nm of thermal SiO2. The chip design is for 20 graphene transistors per chip, with a common source electrode for each group of 10 FETs, a top gate electrode in the center of each chip, and a back-gate access pad to allow double- gating of the transistors.

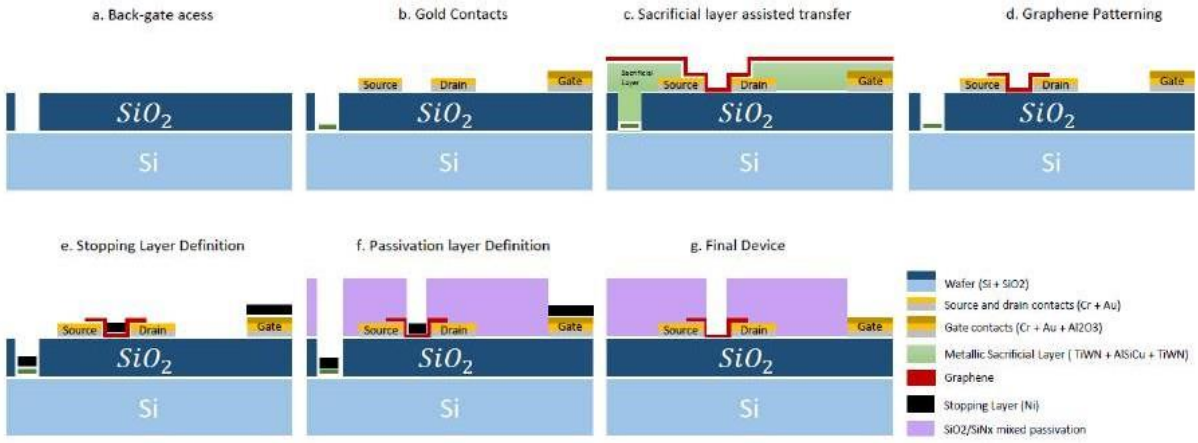


Figure 2 - Graphical overview of the optimized fabrication process for wafer-scale production of EG-GFETs for biosensing.

a. back gate definition and patterning. b. Conductive material and passivation material definition. c. sacrificial layer used during graphene transfer to avoid transfer-borne residues on gold surfaces (e.g., gate electrode). d. graphene is patterned by dry etching, and the sacrificial layer removal. e. stopping layer prepared on top of graphene, based on Ni. f. deposition and dry etch patterning of the passivation stack. g. stopping layer dissolved, and the final device achieved.

The first step is to open the back-gate access using optical lithography and reactive ion etching (Figure 2.a). Then, a contact layer stack is sputtered on the wafer: 3 nm of the Cr adhesion layer, 35 nm of the Au conductive layer, and 20 nm of the Al2O3 protective layer. The contacts are patterned using optical lithography and ion milling (Figure 2.b). The sacrificial layer for graphene transfer is prepared by lift-off, using TiW(N) in the top layer to ensure the sacrificial layer's stability during the multiple graphene transfer steps. Optical microscopy is used to confirm the lift-off process's completion. The processed

PMMA/graphene films are transferred onto the wafer's desired regions until full coverage is achieved (see Figure 2.c). After PMMA removal, graphene is patterned with low power ECR-O2 plasma (Figure 2.d). After removing the sacrificial layer, graphene quality is accessed by optical microscopy (film continuity).

Previously to the passivation, Al2O3 is selectively removed to improve adhesion of the passivation to the chips' surface. Al2O3 is kept only at the gate and pads to prevent contact with the stopping layer by patterning 2200 nm thick AZP4110 photoresist and wet etching with alkaline solution (AZ400k 1:4). A hard coating for passivation is chosen. The next step is the stopping layer and passivation layer deposition with Ni-based stopping layer (black layer in Figure 2.e) and SiO2 and SiNx dielectric passivation (Figure 2.f). The final wafer (Figure 2.g) is analyzed with EDX to discard the presence of process contaminants. Characterization using Raman spectroscopy after processing the wafer is used to confirm the achieved final quality of graphene.

1.1.3 **Fabrication at wafer scale Step-by-step**

Back-gate Definition

A 200 mm diameter crystalline silicon wafer (Siegert Wafer GmbH) with 200 nm of deposited SiO2 by plasma enhanced chemical vapor deposition (PECVD) was used as a substrate for the chip fabrication. The backgate is a contact to silicon, where we intend to apply voltage through a pad. If the pad is metal directly deposited on silicon, the air-exposed silicon is covered in oxide that present a Schottky barrier effect (non-linear and asymmetric). To restore the ohmic behavior of the metal/silicon contact, two approaches have been previously tested (A. Chícharo, March 2021):

1. Expose a silicon wafer to HF vapor etching (Primaxx), transfer it quickly to vacuum and deposit gold.

2. Perform a long sputter etch followed by aluminum sputter deposition without break-in vacuum.

Measurements were performed using two contacts present on the test samples. The samples with sputtered metal (Al or AlSiCu) on Si without pre-processed showed rectifying behavior also strongly dependent on exposure of the silicon sample to light.

1. The HF-exposed Si wafers with sputtered gold showed good linearity with the applied voltage, as well as ohmic I/V behavior.

2. The Si sample processed with sputter etch and AlSiCu deposition showed linear voltage behavior, but non-linearities in I/V.

To applying back voltage (not passing current), both results are acceptable. The process with pre-sputter and AlSiCu is easier to realize and was chosen for this wafer.

The process is performed in two lithographical steps. In a first step, a hole (in the photoresist) is defined at the place of the backgate. Reactive ion etching is used to etch the thermal silicon dioxide of the wafer, down to the silicon wafer. Photoresist is removed using plasma asher. A second lithography defines the area of the pad, slightly larger than the one defined previously. The sputter etch is applied for 600 seconds to the opened area, and a layer of AlSiCu 100 nm / TiWN 15 nm is deposited. This deposition is followed by lift-off. In order to improve the lift-off, the lithography is performed with the assistance of the Soak process.

Gold Deposition and Patterning

Here we have the step of conductive material deposition and passivation material deposition. A thin layer of chromium (Cr, 3 nm) was sputtered onto the wafer to form an adhesive layer for the gold deposition (Au, 40 nm) and a protective layer was next sputtered (Al2O3, 20 nm). The source, drain and gate electrodes were patterned by DWL using AZ1505 600 nm as a positive photoresist using a dark exposure and an ion milling was used to etch the unprotected gold sites with Argon at an angle of 130 ° for 411 sec. The end of the process was confirmed by a mass spectrometry of the residual gases in the chamber. After that the photoresist was stripped by action of Oxygen Plasma, 3 times 13 minutes of plasma, with a maximum temperature of 85 degrees.

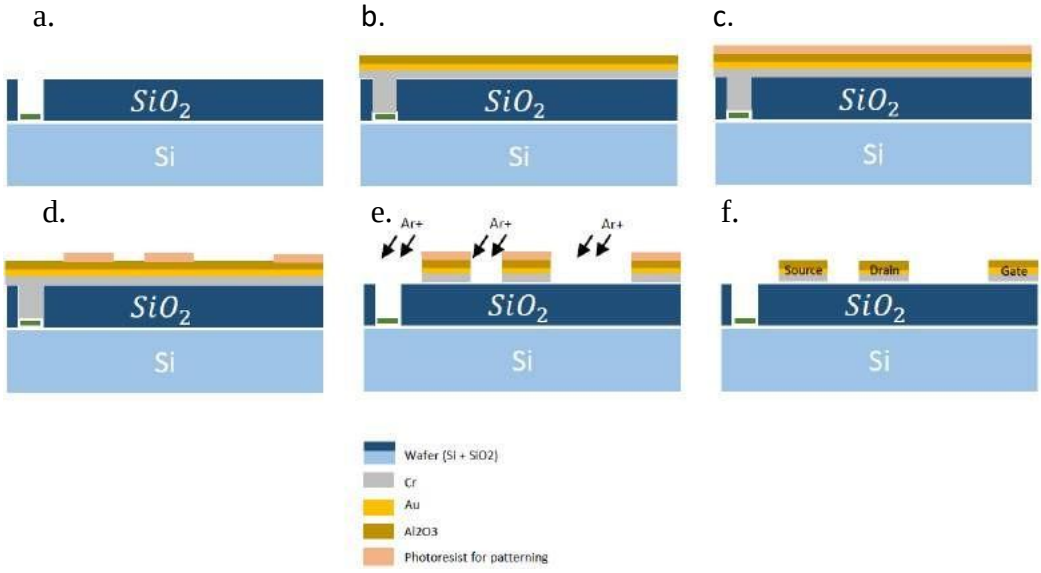


Figure 3- Schematic representation of the gold deposition and patterning by ion milling.

a. Silicon dioxide (SiO2) deposition. b. Chromium (Cr), gold (Au) and alumina (Al2O3) deposition by magnetron sputtering. c. Optical lithography of the gold current lines, electrodes and gate using a positive photoresist (AZ1505). d. Photoresist development. e. gold physical etching by Ion milling with Argon (Ar+) plasma. f. Photoresist strip.

Via Opening

Like in previous processes, gold is protected by aluminum oxide. This oxide will be used to protect gold during graphene patterning by plasma process. This oxide must be removed from the places where graphene will be in contact with source and drain. The oxide is etched by the developer, at rate of 3 nm/min, which corresponds of 3 min overdevelop for each 10 nm deposited. We execute this as 4 min each overdevelopment so that there is 25% over-etch (we never can be sure of the thickness of the oxide, and its cleanliness level will also impact the initial etch rate). The resist is 1 µm, and needs to be of sufficient thickness to allow the over-develop procedure in dark erosion. With some tests, we saw that 20 nm of oxide removed by 6 min development leads to a quite eroded resist layer to the point that the protective nature of resist is not ensured, however we kept 20 nm in this process, and we do 2 lithography's to have the certainly that Al2O3 it just removed were we want without affecting the areas need to be.

Sacrificial Layer Definition

In this step a hard mask is used, not to pattern graphene but to protect the substrate during graphene transfer and patterning by O2 plasma using a photoresist mask. Any contaminants not removed by the oxygen plasma are removed together with the hard sacrificial mask. The contaminants possibly deposited with graphene on the source and drain are not avoided. Still, they do not significantly affect the device performance, since they are not in contact with the biological solutions.

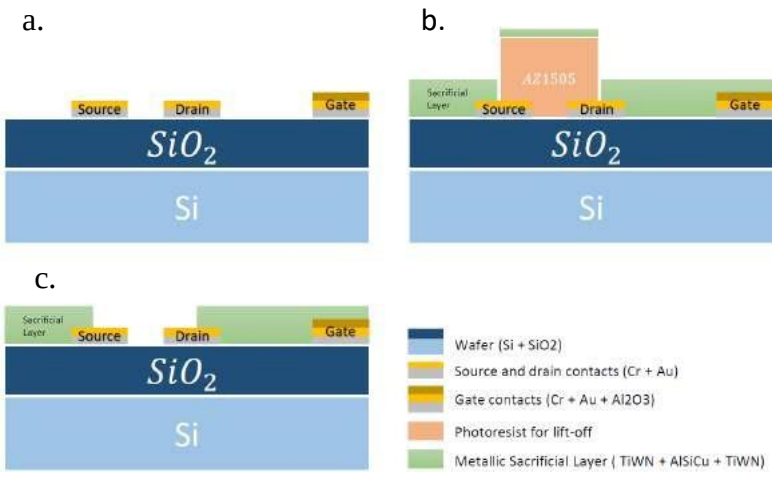


Figure 4- Schematic representation of the sacrificial layer definition follow by lift-off.

a. Conductive material and passivation material after definition. b. Preparation of the sacrificial layer via lift-of. c. Lift-of sacrificial layer, leaning only the channel region and source and drain electrodes exposed for the graphene transfer.

The sacrificial layer should withstand the standard transfer process and patterning of graphene, and it should also be easily removed (e.g., dissolution), leaving the graphene intact. With that in mind, it was designed as follows: 5nm TiWN, 100 nm AlSiCu and 15nm TiWN by lift-off following. At the point of the fabrication sequence where the sacrificial layer is added, only the contacts have been patterned, and so a standard lift-of can be used with no risk of damaging underlying layers. Thus, after a lithographic step that leaves the photoresist protecting the source, drain, and channel, the sacrificial layer stack is deposited by sputtering followed by lift-of using acetone and ultrasonic bath.

Graphene Growth and Transfer

Graphene is grown by CVD in a hot-wall reactor (First Nano ET3000, New York, NY, USA) on high-purity Cu catalysts and then transferred. The process is optimized to achieve monolayer films with low defect density. The 10 x 10 Cu foils were previously chemically treated using a mixture of a solution of FeCl3, HCl and Di Water for one minute in ultrasound.

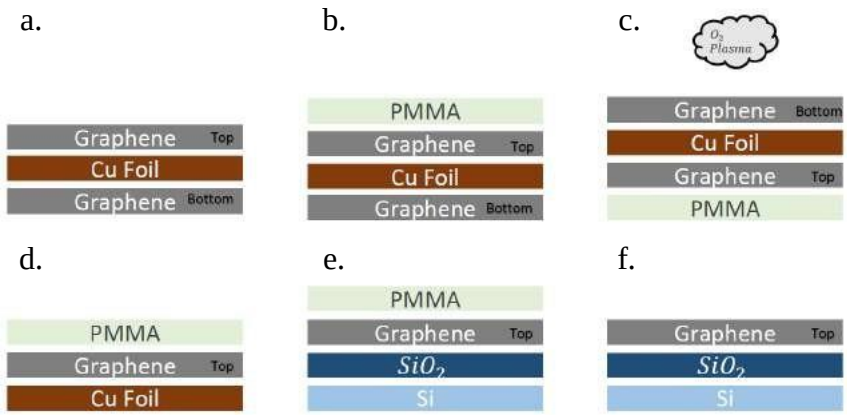


Figure 5- Graphene growth and preparation for transfer process

a. Graphene growth in the chemical vapor deposition machine on the top and bottom sheets of the copper foil. b.PMMA spin-coating of the top-quality graphene to assist its handling and protect it from the physical etching process. c. Etching of the graphene from the bottom by oxygen plasma. d. Copper foil dissolution and graphene transfer for SiO2. f. Graphene transfer for SiO2.

The Cu substrates were placed into a three-zone quartz tube furnace (EasyTube ET3000, CVD Corp.) and the system was evacuated to approximately 2mTorr and then filled with 250-sccm Argon (Ar, 99.999% purity) and 60-sccm Hydrogen (H2, 99.999% purity) gas mixture. Once the growth temperature and pressure were reached, the carbon precursor, methane (0.5 sccm) was introduced into the chamber. The growth was carried out at 1040 °C with 6 torr for 50 min. During the CVD process, graphene grows on both sides of the copper foil. At this point, Raman spectroscopy analysis was performed to identify the side with higher graphene quality. Posteriorly, the side with highest

quality was coated with poly(methyl methacrylate) (PMMA) to protect it from the oxygen plasma etching and aid the transfer process. The low-quality graphene was etched by the action of O2 plasma and copper dissolved by action of FeCl3 (0.5M) for 2h min at room temperature. The graphene was cleaned by repeated cycles of HCl (2%, 1h) and DI water (10 min) and then transfer for the wafer. To remove PMMA the wafer is immersed in acetone for 3h, followed by 1h in isopropanol and 30 min in Di Water. Graphene transfer and patterning are crucial steps in the fabrication of graphene devices. Except for automated, continuous transfer systems, which are not universally available yet, the wet graphene transfer limitations are mostly user-related, requiring a trained hand to achieve reproducible results.

Graphene patterning and sacrificial layer removal

After PMMA removal, graphene is patterned with low power ECR-O2 plasma and the sacrificial layer is removed with H2O2 for etch TiWN, and AZ400 to remove AlSiCu. The photoresist was stripped with acetone for 2 hours, cleaned with IPA, DI water and N2 dried, after that graphene quality is accessed by optical microscopy (film continuity) and Raman spectroscopy for structural quality and continuity.

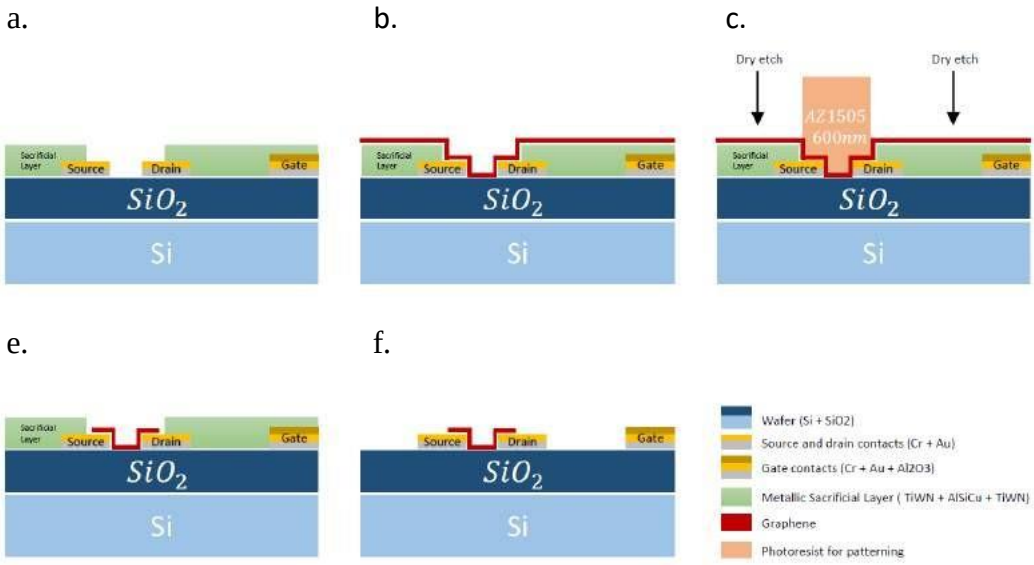


Figure 6- Pre-transfer sacrificial layer to protect the chip surface from residues.

a. Preparation of the sacrificial layer via lift-of, leaning only the channel region and source and drain electrodes exposed for the graphene transfer. b. Graphene transfers over the protected devices, where it only contacts the actual surface where desired. c. Graphene patterning using O2 plasma (dry etching). d. The exposed sacrificial layer is removed by wet etch, removing the residues left on the transfer process's surface. e. Finalized graphene transfer and patterning process, leaving the gold surfaces free of residues. f. After graphene patterning the sacrificial layer is removed.

Previously to the passivation, Al2O3 is selectively removed to improve adhesion of the passivation to the chips' surface. Al2O3 is kept only at the gate and pads to prevent contact with the stopping layer by patterning 1200 nm thick AZP4110 photoresist and wet etching with alkaline solution (AZ400k 1:4).

Dielectric Passivation Layer

When a plasma etching is performed on graphene, a stopping layer must be prepared on top of it to prevent the etching from damaging graphene. For this a new lithography was used to pattern the stopping layer (SL) by lift-off to protect the Au (from the source, drain and gate) and the SiO2 from the ion milling step ahead. A hard coating for passivation is chosen. Niquel was chose for stopping layer followed by a lift-off because can protect graphene for further depositions of varied materials and higher powers can be successfully performed without damaging graphene. Thus, an effective stopping layer for dry etching of the passivation layer without compromising graphene integrity is achieved. Next, the passivation layer is deposited as a stack of two 50 nm films of SiO2 and three 50 nm films of SiNx with 250 nm of final thickness. The passivation stack is patterned using 1035 nm of AZ1505 photoresist and optical lithography, followed by Ion Milling using previously optimized parameters. After removing the remaining photoresist, the channels and the gate electrode are released by wet etch of the stopping layer (FeCl3 for Niquel remove). The removal of the stopping layer was followed by EDX, allowing the final devices to be process contaminants free. The EDX spectrum will show the stopping layer's condition after patterning the passivation.

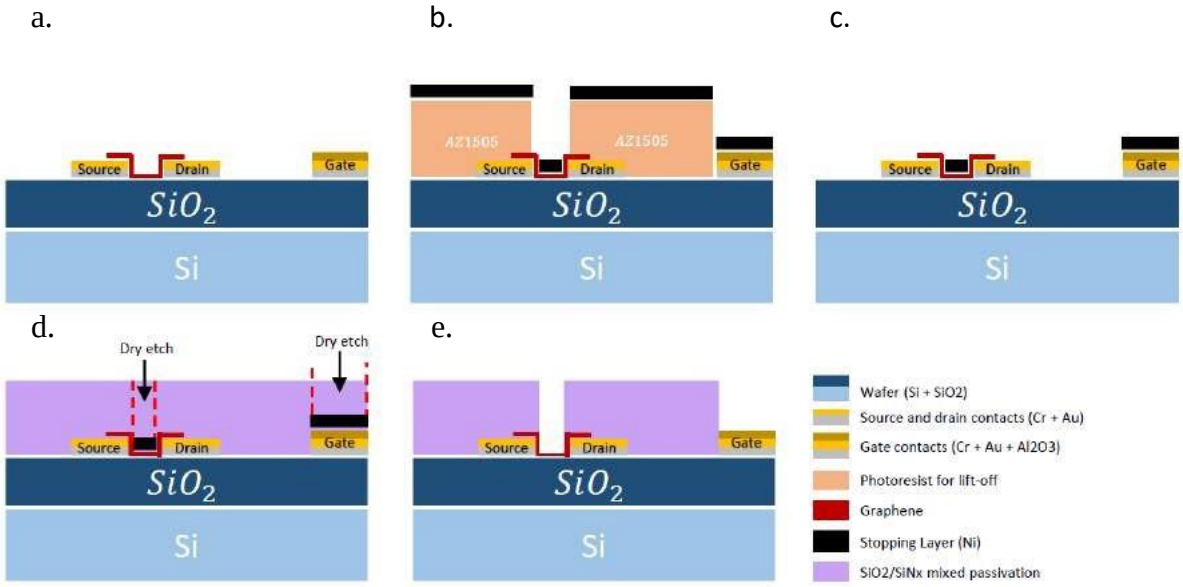


Figure 7- Patterning of the dielectric passivation by RIE using a sacrificial/stopping layer.

a. Sample after graphene transfer and patterning, ready for dielectric passivation. b. Preparation of the metallic stopping layer by ultrasonication-free lift-of. c. Stopping layer after patterning covering the graphene channel and the gate electrode. d. Deposition by PECVD of SiO2 and SiNx dielectric passivation and standard RIE patterning. e.after wet, final device etch of the stopping layer, with only the graphene channel and the gate electrode exposed for contact with the electrolyte.

Dicing

After all the steps, the wafer was cut into individual chips with a dicing saw machine with a 250 µm blade. Each chip was posteriorly cleaned with acetone, IPA, ethyl-acetate and DI water before use.

Wire bonding

Finally, each chip is mounted on a fibre glass chip designed for the printed circuit board (PCB) used for the project. The connections between the two chips were made by wire bonding which makes use of ultrasonic vibrations to weld a thin aluminium wire between the pads of the two chips. A silicone gel was used to protect the fragile wires to corrode or break.

1.1.4 Sensor Characterization

Scanning electron microscopy

The microfabrication process was evaluated by scanning electron microscopy (SEM) (NovaNanoSEM

650). Images were collected in secondary electron imaging mode at operating voltages and working distances as presented in the SEM microphotographs.

Raman Spectroscopy

Raman analysis was carried out on a Witec Alpha300 R Confocal Raman microscope using a 532 nm Nd- YAG laser for excitation at an output laser power of 1.5 mW. Samples were measured using a 50x objective and an integration time of 2s.

Dry etch resistance

For the devices' electrical characterization, an automated probe station is used to measure either the current or the voltage drop in the channel between source and drain contacts at a fixed voltage of 1 mV or a fixed current of 1 uA, respectively. Then, the measured values are converted to resistances to provide information on the homogeneity of the devices' process and quality. For the geometry of the transistors (W/L = 3) and the unintentional doping level of processed graphene, a channel resistance, R, below +/- 1000 W is expected in successful devices, while values up to +/- 2500 W are still acceptable. Transistors with R > 2500 W were rejected and discarded.

1.2 Results and Discussion

1.2.1 Back Gate Definition

E1C lithography- Back-gate definition

In a first step, a hole (in the photoresist) is defined at the place of the backgate. Reactive ion etching is used to etch the thermal silicon dioxide of the wafer, down to the silicon wafer. Photoresist is removed using plasma asher.

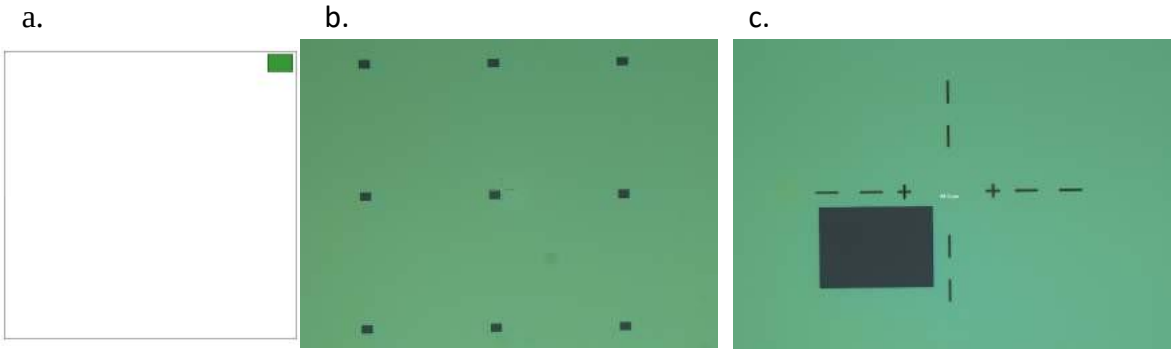


Figure 8- E1C lithography

a. mask representing one chip and the respective hole for back-gate definition. b. optical images of the process with a total of 9 chips. c. Marking the lines in the center of the wafer for future alignments.

E2D lithography – aluminum etch

A second lithography defines the area of the pad, slightly larger than the one defined previously. The sputter etch is applied for 600 seconds to the opened area, and a layer of AlSiCu 100 nm / TiWN 15 nm is deposited. This deposition is followed by lift-off. In order to improve the lift-off, the lithography is performed with the assistance of the Soak process.

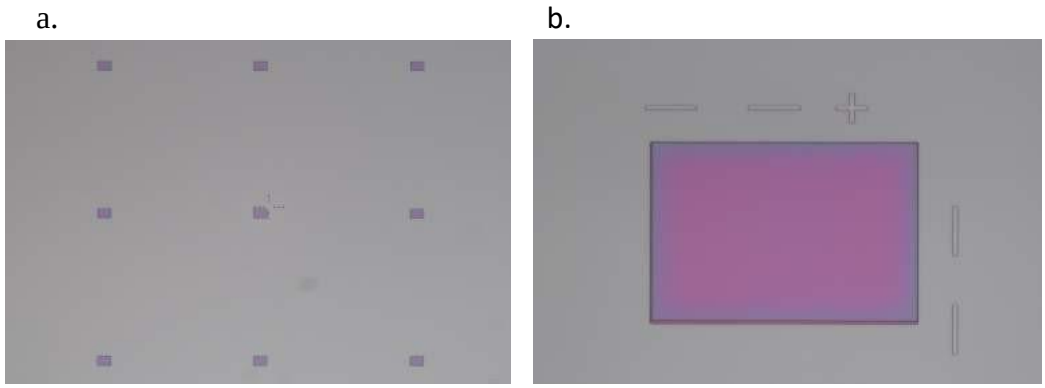


Figure 9- E2D lithography

a. optical images of the process with a total of 9 chips. b. optical image showing the center of the wafer and the mark of lithography inside the previous one.

1.2.2 **Gold deposition and patterning**

Conductive material Deposition

For conductive material the choice was Cr 3nm and Au 35 nm. Chromium is used as an adhesion layer; it needs to be continuous (> 2 nm). It could be made thicker (5-10 nm) but this increases the total thickness, which is to be avoided. Gold is used as a conductive material due to its high conductivity and its stable nature (does not oxidize easily). With another material, the transfer inside water could always lead to oxidation of the metal (even a very thin nanometric layer) and the graphene would be transferred onto a non-conductive oxide. The total thickness must be kept under limits, because graphene is sensitive to the gap between the gold and the silicon oxide in the bottom of the layer. By using 30 to 40 nm of gold, we never had problems, but we know that with ≈ 100 nm, graphene would break. For this reason, we should limit the total thickness. The deposition of gold is done with an exclusion ring. This exclusion ring makes sure no gold is deposited in the extremities (within 8 mm) of the border of the wafer. This is necessary to avoid damaging the gold during the plasma asher. Indeed, gold is damaged by oxygen plasma, so at a later step we protect the gold by aluminium oxide. But the aluminium oxide machine does not deposit in the whole area. Therefore we must avoid that there is gold in the outer regions of the ring.

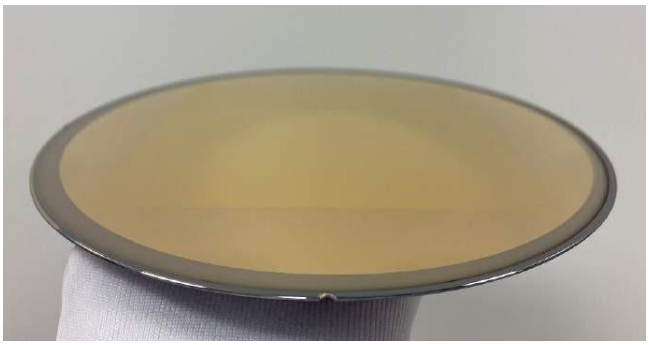


Figure 10- Picture of the wafer after conductive material deposition.

Passivation Material Deposition

Immediately after depositing gold, it is necessary a deposition of Al2O3. This oxide passivates the gold, which can then be exposed to oxygen plasma for cleaning and etching steps. However, aluminium oxide is easily removed by the developer. We should avoid repeating exposures (development) or over- developing except when it cannot be avoided.

In previous processes, we used 10 nm as aluminium oxide thickness, however this layer had to be increased since with only 10nm the alumina ends up being attacked during the process (existence of

multiple lithographic steps and a step of AlSiCu removal which is attacked by the same solutions), so our choice fell on 20nm which worked out quite well. Although Al2O3 is physically separated from AlSiCu by 15 nm TiW there is no guarantee of film homogeneity due to the low thickness, implying that Al2O3 could still be partially attacked during AlSiCu removal. The time required to remove AlSiCu is half of the time for removal of 20 nm Al2O3, meaning the film should stay even if there is partial contact between these two layers.

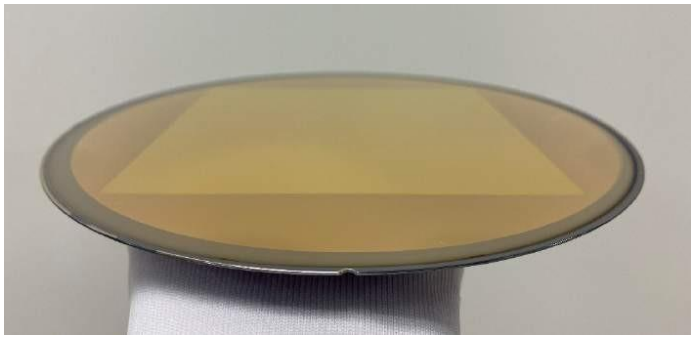


Figure 11- Picture of the wafer after passivation material deposition.

E3D lithography – contacts definition

E3D lithography contains the contacts and helper layers. Different kinds of helper layers are included in different names CTC: the contacts for the device, plus the dicing marks. Dicing marks are like the central cross, but shorter in size. At (0,0), the short dicing mark of CTC is superimposed with the longer central mark present in MRK MRK: markers, the central cross at (0,0), the left and right crosses for horizontal alignment. Placement crosses (±62900,0). LTR: Additional text, currently informing that the space for dicing is limited to 160 um, placed on the left edge at every line. The left corner of the wafer is illustrated below:

a. b.

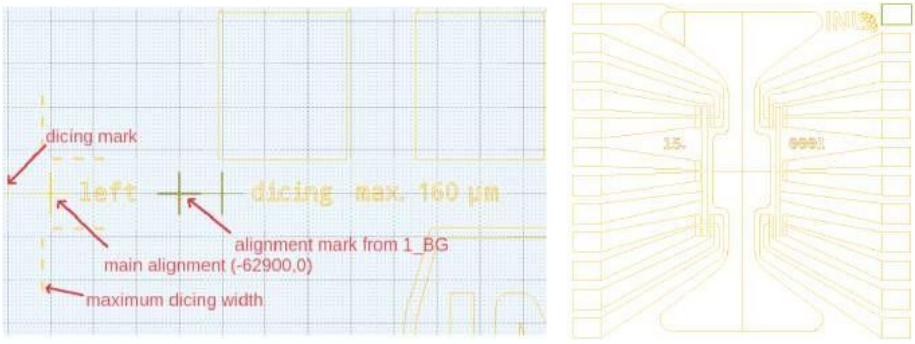


Figure 12 – E3D lithography mask.

a. new alignment marks with higher precision. b. mask used for E3D lithography (representing one chip).

The source, drain and gate electrodes were patterned by DWL with a 1035 nm AZ1505 positive photoresist using dark exposure. Lithography is on Al2O3, this allows better photoresist adhesion as compared to exposing on gold. Photoresist (600 nm) is sufficient to protect Cr, Au and Al2O3 (3+35+20) during the etch and possibly provides better definition of the gaps for the ion milling. The exposure conditions are as given by the machine technician. We should avoid over-development or exposure repetition, as this slowly damages the thin aluminum oxide. As opposed to processes with individual dies, we expose a single mask, centered, no alignment and no offset.

a. b.

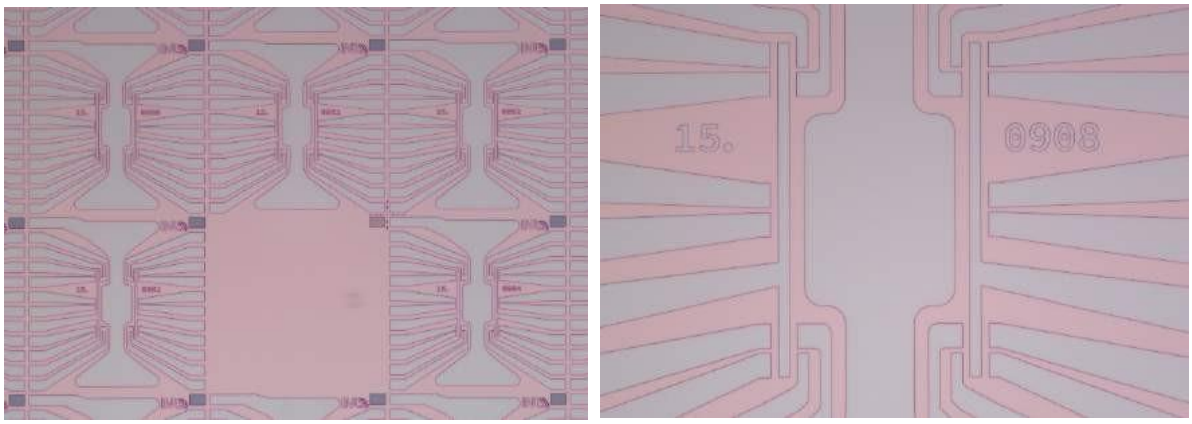


Figure 13- a. Optical images after lithography (center). b. optical images of chip 15.908 after lithography.

Ion Milling

The etching is performed at 130° of incidence (40° from normal), in order to create a canted edge which allows the transfer of graphene without breaking it. Using SIMS technique, the analysis shows the progress of etching of Au and Cr, successively (usually Al is not easy to see). We need to avoid over- etching because it can remove the silicon oxide, which is only 100 nm and is etched quite fast. Over- etch also increases unnecessarily the height of the gap on which graphene will sit. For this reason, the criterion is to not (anymore) wait until all chromium is removed, rather wait for chromium to reach past the maximum and back to half if its initial level. Any remaining chromium below 1 nm will be oxidized and will not short circuit graphene.

It can contribute to graphene doping, hopeful not more than silicon oxide. Also, the SIMS analysis gives the impression that a long time is needed to remove chromium, but this may be due only to the non- uniformity of the etch; only external areas will be with some Cr left. Sidewall cleaning 45 s is helpful to finish removing Cr residues.

In last process, etch time was 411 s (130°) + 80 s (165°). However, the etch rate of the machine has increased, and we look to reduce the over etch, such that the new time is going to be shorter this time.

a. b.

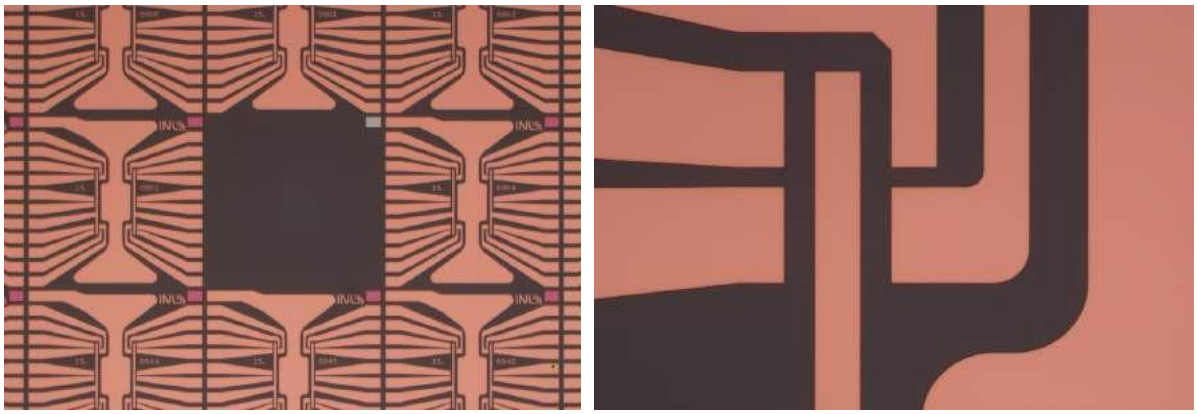


Figure 14- a. Optical images after ion milling (center). b. optical images of chip 15.908 after ion milling (source, drain and channel).

Resist Strip

Thanks to the use of Al2O3 on top of gold, the resist strip can be performed by plasma asher, a technique faster and cleaner than chemical methods. Suggested recipe is LowTemperature Resist Strip 13 min, which works well and avoids heating too much, which could well damage gold features or create thermal stress due to different dilatation parameters in silicon and metal structures. Due to unstable etch rate, the resist strip completion must be verified visually, and the recipe can be repeated if not sufficient.

1.2.3 Via Opening + overdevelopment

E4C lithography – via opening

The L3 layout performs via opening and sacrificial layer, the first as dark and the second as clear. It is slightly inside the L2D gold contacts. This way, the area exposed does not depend of the existence or not small misalignment of less than 1.5 um along Y. The layer is called CD because it is exposed successfully clear and dark identically.

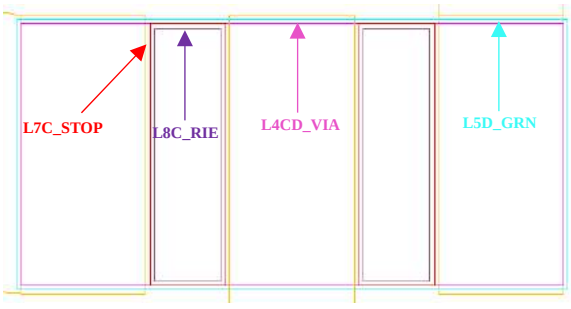


Figure 15- Resume of some masks used in the process. L4CD_via (via opening and sacrificial layer definition), L5D (graphene patterning definition), L7C_STOP (stop layer definition), L8C_RIE (ion milling definition)

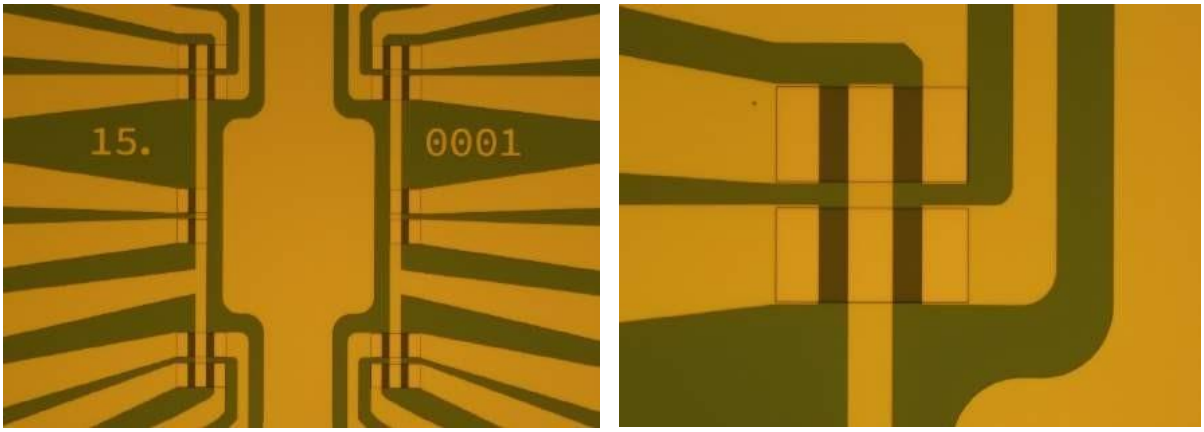


Figure 16- Optical images of the lithography after development + overdelopment (chip 15.001).

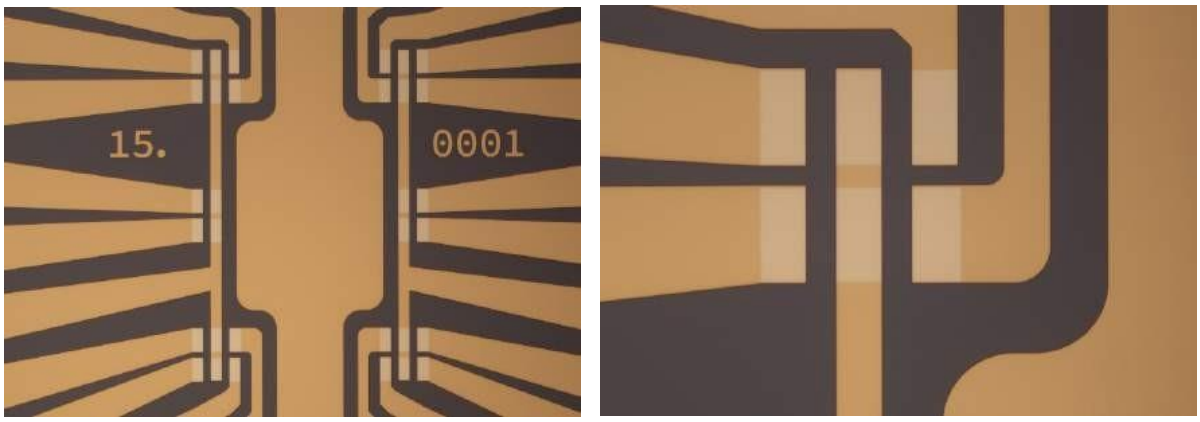


Figure 17- Optical images of the lithography after development + overdelopment (chip 15.001).

1.2.4 Sacrificial Layer Definition and Deposition

A novel approach to improve the surface cleanliness of the chip surface after graphene transfer is demonstrated. An effective sacrificial layer is developed, allowing the patterning of graphene while protecting the pristine gold surfaces. This optimization is of high importance for using the devices as biosensors. It promotes better inter-device homogeneity and less random molecular adsorption responsible for the sensor signal's random response and noise. The process is general and suitable for other applications or devices with similar requirements.

E4D lithography – sacrificial layer

At the point of the fabrication sequence where the sacrificial layer is added, only the contacts have been patterned, and so a standard lift-of can be used with no risk of damaging underlying layers. Because of that a lithography is created that leaves the photoresist protecting the source, drain and channel (Figure 18) to be able to deposit the sacrificial layer by sputtering followed by lift-off using acetone and ultrasonic bath.

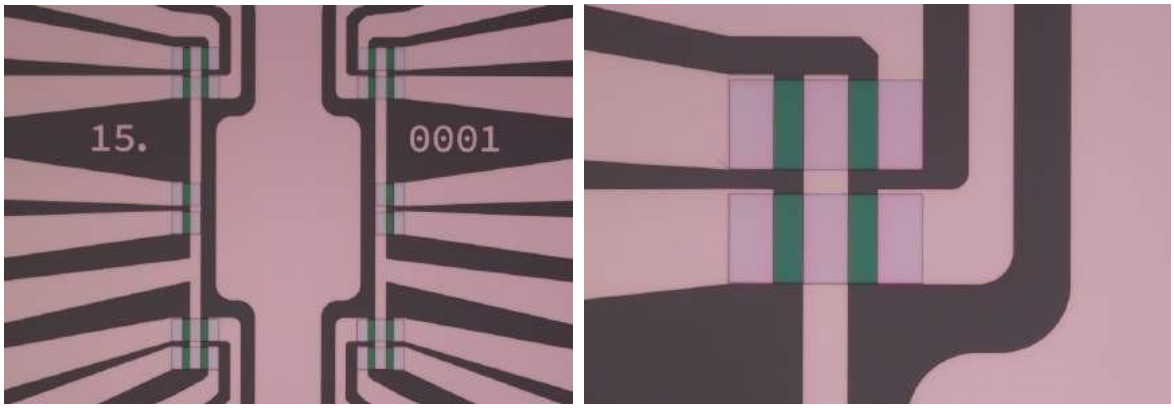


Figure 18- Optical images of the lithography after development (chip 15.001).

Sacrificial Layer Deposition

The sacrificial layer should withstand the standard transfer process and patterning of graphene, and it should also be easily removed (e.g., dissolution), leaving the graphene intact, for this reason 3 layers have been chose (5nm TiWN, 100 nm AlSiCu, 15 nm TiWN). The first layer of TiWN is used to prevent contact between Al2O3 and the sacrificial layer of AlSiCu, avoiding diffusion between this two layers. The low thickness of 5 nm is required to reduce the etching time for this layer, since the solution of H2O2 used to etch TiW can attack graphene if it is to be exposed. In principle graphene will still be protected by the photoresist used for patterning (L5D), still exposure to H2O2 should be reduced to a minimum. The next layer is AlSiCu and this is the effective sacrificial layer that provides physical separation between the wafer surface and graphene.

Figure 19- Picture of the wafer after sacrificial layer deposition.

It is thick enough to ensure that particles and residues adsorbed on its top surface leave together with this layer, once it is removed. AlSiCu is easily etched by the developer AZ400k, with only 4 min being enough etch away completely the layer. Since AlSiCu provides poor adhesion for graphene which can hinder its adhesion on the overall wafer, TiWN was used before to improve it. However, it was not enough and a top layer of Au will be tested. Still, Au and AlSiCu cannot be in contact since it would

create an alloy difficult to remove. As such, a thin layer of TiW is kept to provide physical separation between AlSiCu and Au. The layer is kept thin, 15 nm, to make sure the exposure to H2O2 upon removal is minimal.

Lift-Off process

Lift-off is performed with acetone 2h and 10 min of ultrasounds in the final which can remove the sacrificial layer on top of the channels, source and drain sites (for graphene transfer). Procedure is repeat more 4 times. After lift-off, a cleaning in IPA 30 min and water 10 min is recommended.

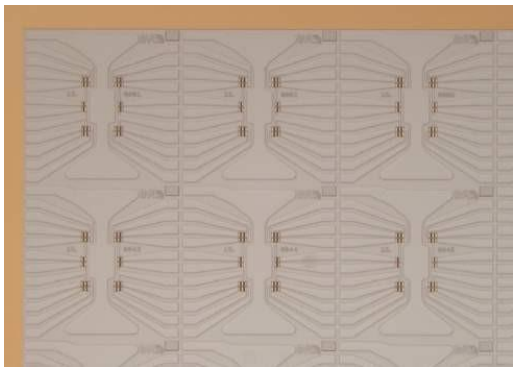


Figure 20- Optical image after lift-off. No sacrificial layer on source, drain and channel.

1.2.5 Graphene Growth and Transfer

During graphene transfer we may have some contaminations from graphene growth or even from the copper dissolution process such as polymeric residues and metallic residues coming from the copper sheet before graphene growth or iron precipitates from the iron chloride solution which are attached to the underside of the graphene film and adhere to the surface to which the graphene is transferred. In addition, one must pay extra attention to air bubbles that can be created under the graphene at the time of copper dissolution and that can originate copper agglomerates, these bubbles can be removed with the aid of tweezers. Iron precipitates can be reduced with the aid of a metal-free attacking agent, such as ammonium persulfate, or by dissolving the iron using an HCl solution. Using fresh solutions of FeCl3 is also an excellent solution previously filtered with a 0.22 µm filter as it can improve the removal of copper agglomerates. Despite all this there are always some small atomic clusters of Cu and ions being observed on the surfaces after graphene transfer. As stated earlier, these particles appear on the copper dissolution side as residues that are trapped at the interface between the substrate and graphene and do not interfere with graphene surface processes, however, are transferred to other exposed wafer surfaces. In our EGFETs, where the upper gate electrode is coplanar with the transistor channel, the exposure of this electrode during graphene transfer leads to

adsorption of residues on the gold surface, contaminating our electrode (strong source of parasitic signal), and as a consequence, the exposure of biological samples can lead to the adsorption of non-specific proteins and DNA at the particle sites. Furthermore, it can lead to voltage drop changes in the electrolyte-holder interface, changing the random behavior, making the interpretation, optimization and use of the device difficult.

Graphene Growth:

For graphene growth the Cu foils were cut in 10x10 pieces, followed by a treatment with an acidic solution (280mL DiWater + 10 mL HCl 37% + 10 mL FeCl3 0.5M) for 1 min.

Figure 21- Pictures showing the process for Cu treatment.

After that graphene was growth in the CVD machine. Growth conditions: 0.5 sccm CH4; 250 sccm Ar; 60 sccm H2; Pressure 6 Torr; Growth time 25 min; Annealing time 30 min; Growth temperature 1040 °C; Annealing time 1040 °C.

a. b. c.

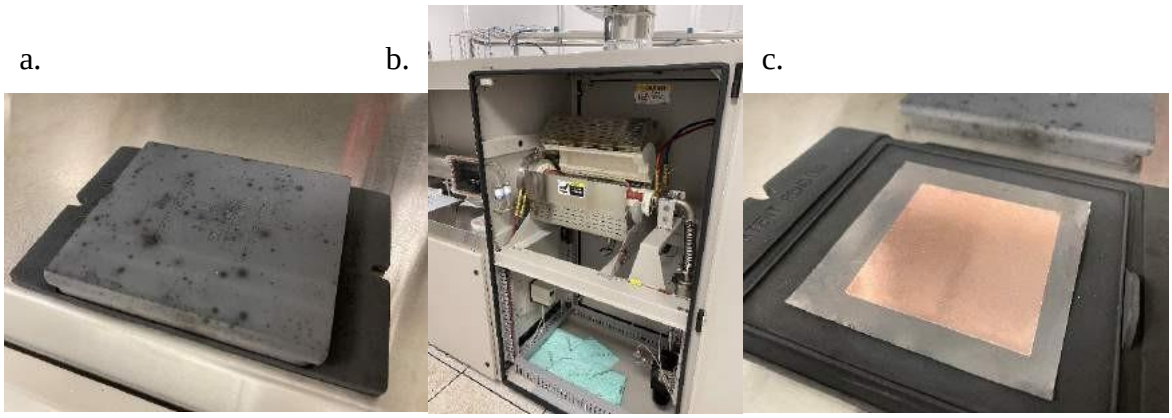


Figure 22- Pictures showing the process for graphene growth.

a. graphite box. b. CVD machine c. graphite box with Cu foil treated.

PMMA 15k powder from Sigma Aldrich ref 200336-100G (273 EUR) dissolved in anisole were coated on top of the graphene (spin-coating with PMMA 15K mix; recipe on the E-beam track recipe 5039, 1k rpm).

a. b. c.

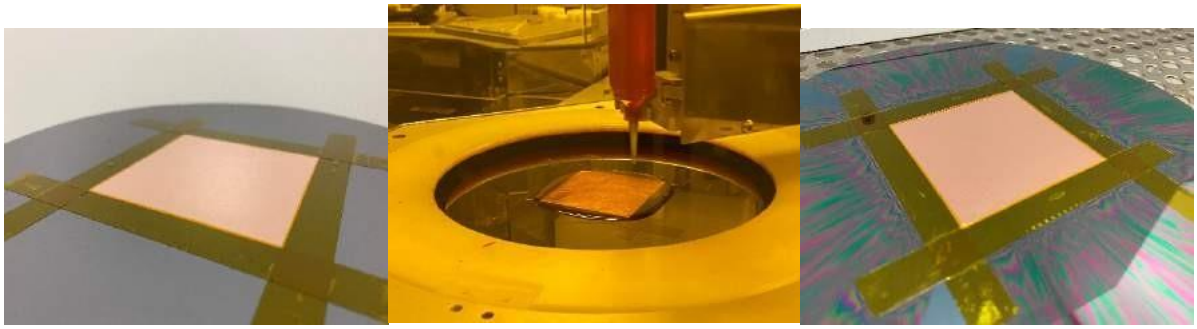


Figure 23 – Pictures showing the process for PMMA coating.

a. graphene without PMMA. b. graphene during PMMA coating. c. graphene after PMMA coating.

Back side was been cleaned by Roth & Rau (recipe: GrapheneCu Foils_O2 Plasma Treatment), 8 cycles of 30s plasma.

a. b. c.

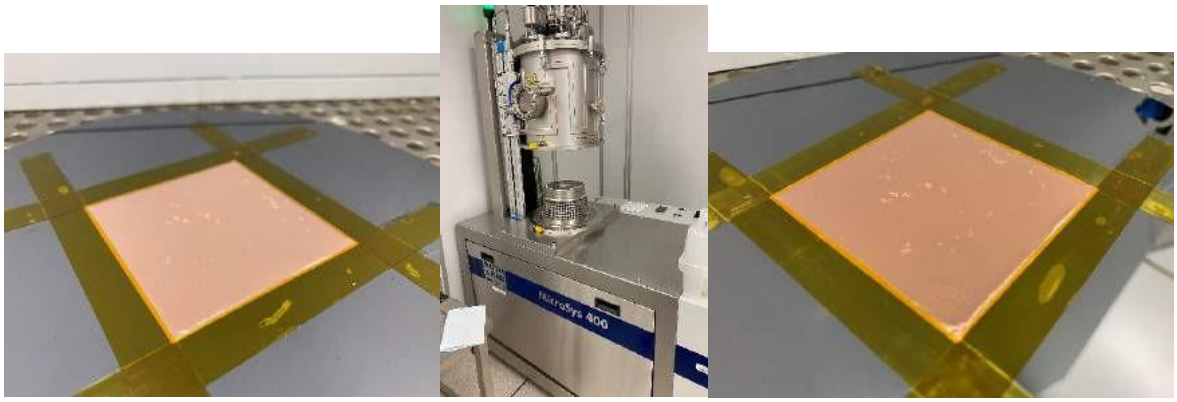


Figure 24- Pictures showing the process for graphene removal from backside.

a. back-side graphene. b. Roth and Rau machine for O2 plasma. c. back-side without after plasma (without graphene).

<u>Graphene Transfer Procedure:</u>

FeCl3 0.5M preparation:

- 163 g of FeCl3 powder to 2 L of diH2O

Add the water slowly due to exothermal reaction

In the end stir the solution with a magnet for at least 3h (1000 rpm)

Cu dissolution:

Fill a glass container with FeCl3 0.5M.

Placed the coated copper piece (~6cm by 6 cm, cut borders) in the glass container for ~2h.

a. b. c.

Figure 25- Pictures showing the process of graphene transfer.

a. Cu/Graphene/PMMA. b. Cu/Graphene/PMMA in FeCl3 for 2h. c. graphene/PMMA in acid (HCl).

- Graphene+PMMA was transferred to clean H2O and then for another container with clean H2O for 10 minutes.
- It was then changed to clean diH2O for 1h.

- The PMMA+graphene piece was transferred to freshly prepared HCl 2% for 3h (108 mL HCl 37% to 2L of DiWater).
- The sample was then transferred to DiWater for 30 min.

- After the final DiWater step, the pieces were transferred to the final substrate.

- After that the wafer was left drying overnight at RT.

When possible, the transfer is done vertically. We should just avoid that the fluids go around from all directions. Therefore, it can be done at an angle. Transfer to the final substrate is performed with the final substrate treated in vapour HMDS to increase hydrophobicity. The transfer tool should be a Si/SiO2 wafer treated in plasma asher to increase hydrophilicity. After transfer, graphene is dried overnight at room temperature. This replaces the bakes that were previously done, with the argument that remaining water molecules blow graphene, when heated, could damage the film. If multiple transfers are performed, PMMA from previous transfer is first removed, then sample is processed again in vapour HMDS.

For PMMA removal the wafer is placed under low vacuum (desiccator) for 1h to improve surface adhesion of the graphene film and then immersed in acetone face up for 3 hours follow by 1hour isopropanol and 30 min Di Water.

1.2.6 Graphene Patterning

E5D lithography – graphene pattering

This layer 4 contains the graphene area. It is larger than then via, so that any misalignment does not change the active width. It is also larger than the gold area because we noticed the plasma asher reduces the size of graphene. If this layer is too large, the excess width will not count for biosensing, but reduce the electrical signal. Therefore, excess should be avoided. This lithography is 1.5 um bigger than VIA, which is the nominal size it should have.

We use lithography to define the area of the graphene transistor. This exposure is Dark. We expose all around graphene, just letting graphene for exposure. It uses a thicker resist (2200 nm) in a way to protect better graphene during the etch.

a. b.

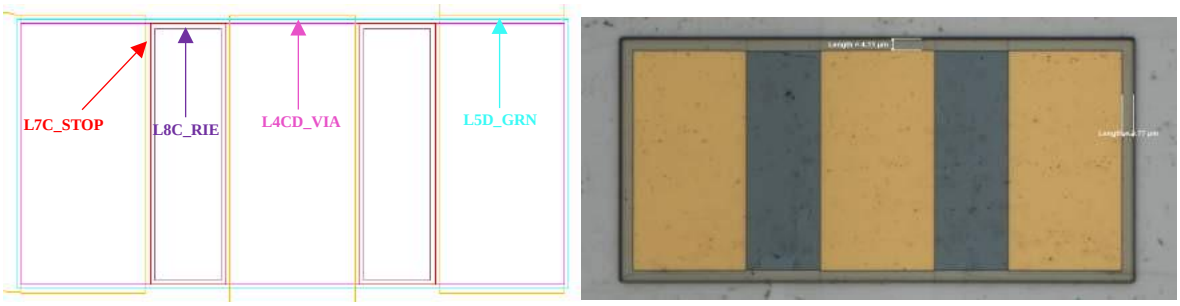


Figure 26- Resume of E5D lithography for graphene pattering

a. L4CD_via (via opening and sacrificial layer definition), L5D (graphene patterning definition), L7C_STOP (stop layer definition), L8C_RIE (ion milling definition). b. Optical images after lithography.

Graphene etch

In the past we have used oxygen plasma steps of 2 minutes at 250 W, monitored by profilometer. The process removes about 100 nm of resist in each step and is monitored by profilometer, in a way to remove about 500 nm of photoresist. This process was able to removed graphene, but was never able to remove completely the residues that came from the graphene transfer. However, because this time we have a superficial layer that protect the wafer from the residues a simple oxygen plasma can be performed ICP machine that controls better the temperature.

a. b.

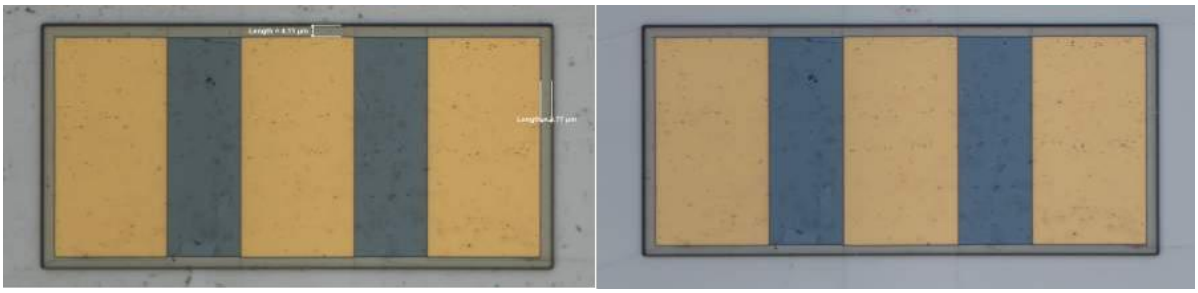


Figure 27- Resume of graphene patterning.

a. Optical image after lithography for graphene patterning. b. optical image after graphene pattering.

Looking for optical images (Figure 27) we can concluded that graphene etch by plasma O2 was successful. The area around source, drain and channel its very clean compare with before graphene etch.

Sacrificial Layer removal

To remove the sacrificial layer:

- TiW etch: Immerse wafer in H2O2 30% for 3min30sec; Rinse with diH2O and dry softly.
- AlSiCu etch: Optical track, recipe 0014, AZ400k 1:4, 120s, 3 times.
- TiW etch: Immerse wafer in H2O2 30% for 150s; Rinse with diH2O and dry softly.

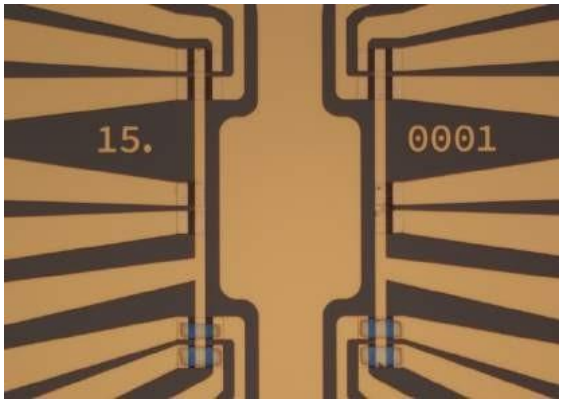


Figure 28- Optical image after sacrificial layer removal.

Photoresist Removal

Acetone is used to remove the remaining photoresist. Because of the plasma process, the photoresist is probably hardened. Removal by acetone has worked. Sample then passes from acetone to IPA, and from IPA to water. As above for the step of transfer, it should be noted that passing from IPA to water should be done with a lot of care due to the difference in

viscosities, which cause perturbations in liquid flow and possibly leads to mechanical damage to the transferred graphene.

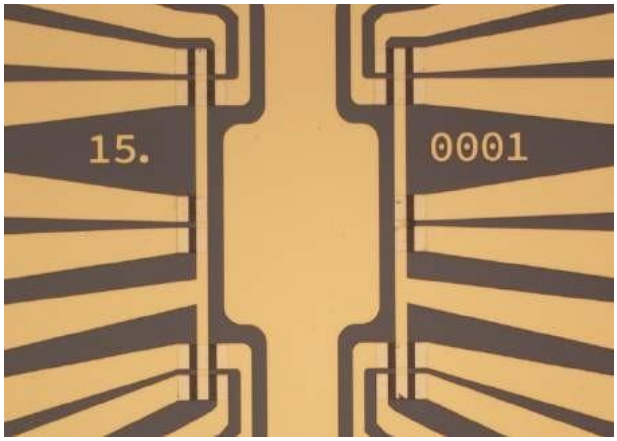


Figure 29- Optical image after photoresist removal.

1.2.7 Al2O3 cleaning from lines

L6D lithography – Al2O3 cleaning (lines only)

The layer contains pads and gate. It is exposed dark so that the photoresist is removed from mostly everywhere, the areas where the passivation is due to stay, and where the aluminum oxide should be eliminated. The aluminum oxide was not deposited with the gold. It was deposited when needed, which is before graphene transfer, with the purpose to protect the gold for graphene etching. It was then removed.

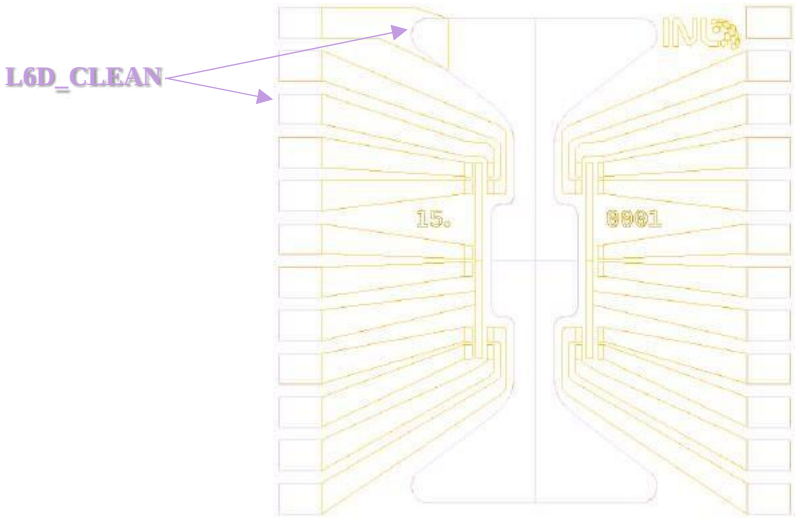


Figure 30- Lithography mask for Al2O3 cleaning (light purple lines).

Actually, a layer of aluminium oxide is included as part of the stopping layer, which is deposited and removed before graphene transfer. In a previous process, we already used the aluminium oxide on top

of the gold immediately after deposition, and opened by wet etch only to open at the source and drain for the transfer. The passivation is done by polymer, after graphene transfer, without stopping layer (and aluminium oxide is removed at that moment). In this process, there is a need for a stopping layer, but contrary to previous processes, it is deposited after graphene. The stopping layer is composed of niquel in the bottom, which is the materials that lasts damage graphene. There is a need for aluminium oxide to be present on exposed gold to prevent intermixing with niquel. But there is also a need to not have aluminium oxide on current lines to avoid that it stays below the passivation layer (aluminium oxide is much worse as passivation, it is easily dissolved in buffers, which might cause delamination of the passivation starting from the channel or from pores in the passivation). The chosen solution is: using the aluminium oxide that stayed on the gold to protect the gate; selectively remove the aluminium oxide from the current lines by lithography. The level lithography is performed clear. As it is an aluminium oxide cleaning, it uses AZ1505 1 µm resist.

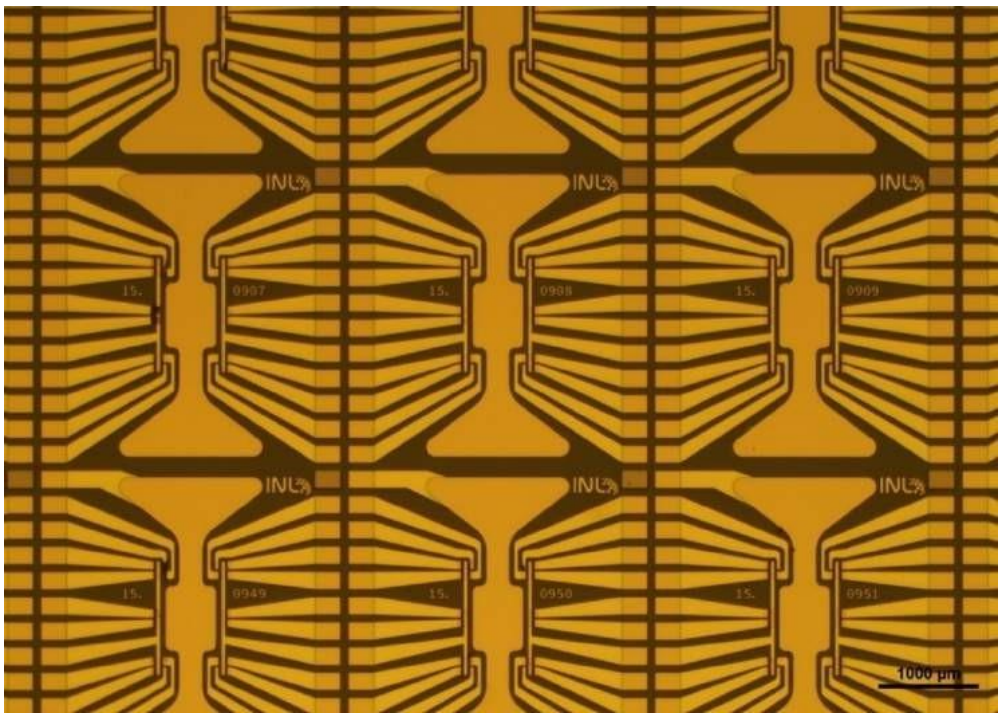


Figure 31- Optical images of the lithography after development + overdelopment.

Passivation etch

Aluminum oxide is removed, as above, using 4 minutes of over-development.

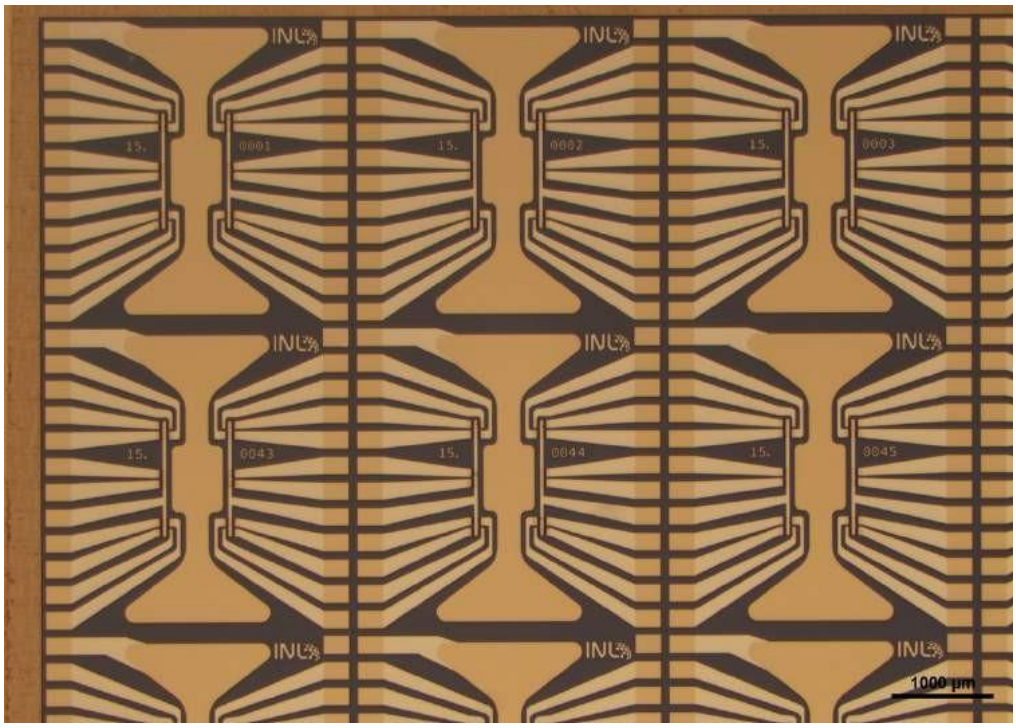


Figure 32- Optical images after photoresist removal. No Al_2O_3 in current lines.

1.2.8 Stooping Layer Definition

L7C lithography – stopping layer

The stopping layer defines the region of the channel, where we want to de-passivate graphene. It is slightly inside the area graphene, because misalignments to the outside would cause a big problem to the function of the device. If overlapping the silicon substrate, it would cause short circuit to bottom gate. If overlapping with the gold contacts it will cut them.

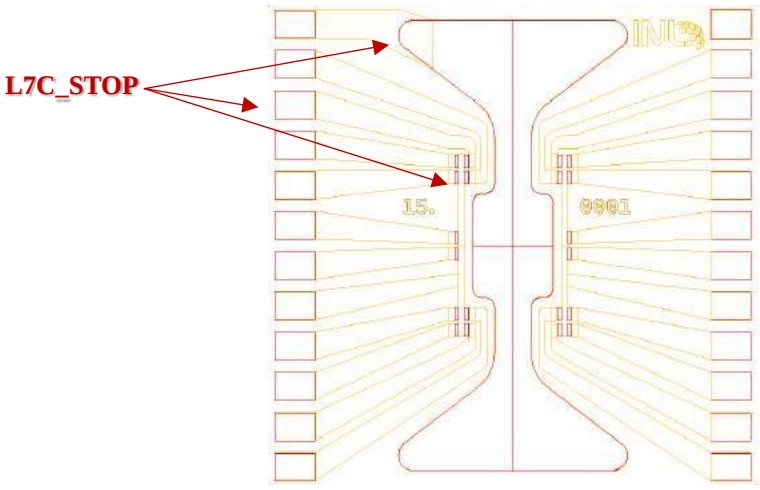


Figure 33- Lithography mask for stopping layer definition (red lines).

As the stopping layer is deposited by lift-off, the lithography is performed first. The stopping layer needs to be present on the places where we want exposed gold in the end: channel, gate and pads. Contrary to previous process, where we passivate 2 µm around the lines, here we will passivate all the silicon area except where needed not to be passivated. This can only lead to better passivation. The lithography is performed clear, because we only open lift-off at the places where we want the stopping layer to be present. Because of the lift-off process, we can consider a thick resist so that the lift-off becomes easier. Soak process was considered for lift- off.

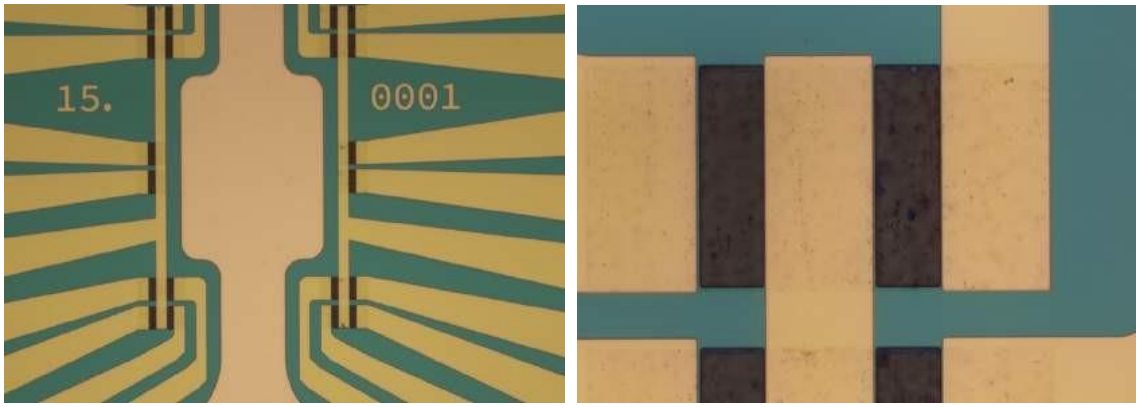


Figure 34- Optical images of the lithography after development (chip 15.001).

Deposition of stopping layer

Stopping layer is chosen as: Ni 10 nm / Al(SiCu) 30 nm Optionally, a thin TiWN layer like 5 nm TiW:

- Niquel 100 nm: niquel at INL is deposited in Kenosistec, which is a low-power sputtering system with larger target-sample distance, which limits damage caused by sputtering. The purpose of Ni is to be a first layer that protects graphene from further treatments. What matters to graphene is the first nanometer that is deposited on top, that should be of a very soft process.

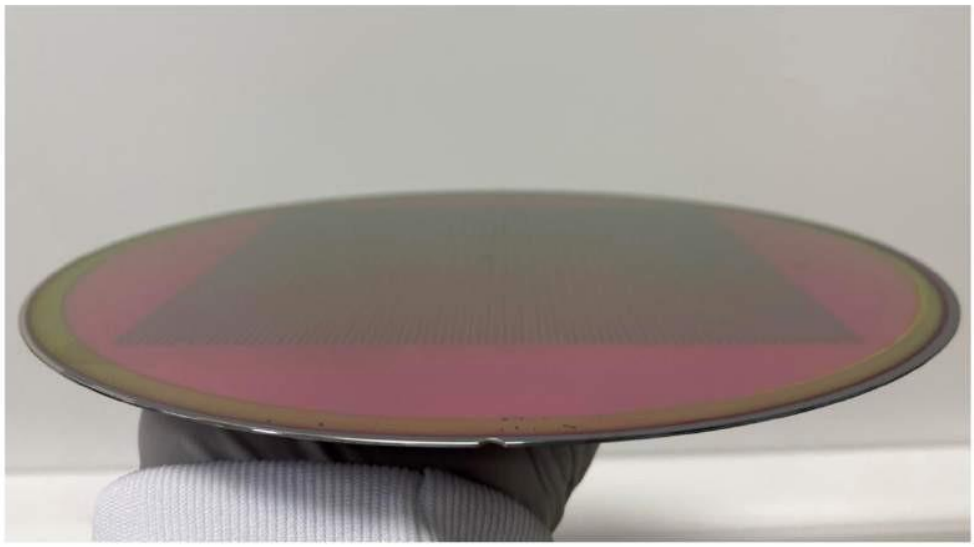


Figure 35- Picture of the wafer after stopping layer deposition (100nm Ni).

Lift-Off processes

Lift-off of the stopping layer must be performed in a way to minimize risk of damaging graphene. • Use of ultrasounds is not possible • Use of Microstrip 3001 is not possible due to presence of copper in the stack • Hot solvents damage graphene.

At first, acetone at room temperature is used, and let for sufficient time (at least 2 h). A flow of acetone, for example using a plastic Pasteur pipette, is used to provoke the lift-off of the metal. Cleaning in IPA and water must be done with care to avoid damaging graphene when changing to liquids of different viscosity.

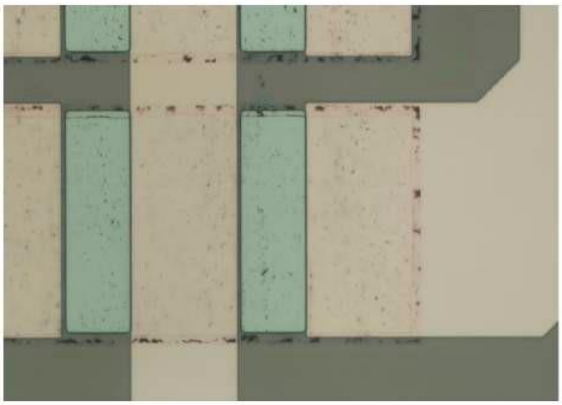
Figure 36- Optical images after lift-off (chip 15.001).

1.2.9 Passivation layer Deposition

Passivation Layer

The passivation layer is a multistack SiNx/SiO2. It is composed of 5 layers that alternate SiNx and SiO2, the first and the last one are SiNx. This provided in the past good insulation, also we never observed stress on the layers. The last layer should be a nitride as this is the best passivation. For the first layer we do not have evidence if nitride or oxide is better, but nitride has worked well so we can keep it. The composition is: (Si/SiO2/Cr/Au/) Si3N4 50 nm / SiO2 50 nm / Si3N4 50 nm / SiO2 50 nm / Si3N4 50 nm.

a.



b.

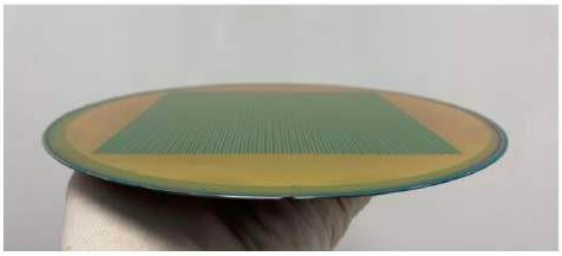


Figure 37- Pictures of passivation process.

a. Optical images after passivation (chip 15.001). b. picture of wafer after passivation.

L8C lithography – passivation layer definition and ion milling

The areas to un-protect by plasma (ion milling) are those inside the stopping layer. This ion milling layer must be strictly enclosed within STOP layer to avoid similar effects as STOP misalignment, which is device short-circuiting to silicon, or gold destruction. One pad on top left is right open, it just etches to silicon, leaving access to back gate.

a. b.

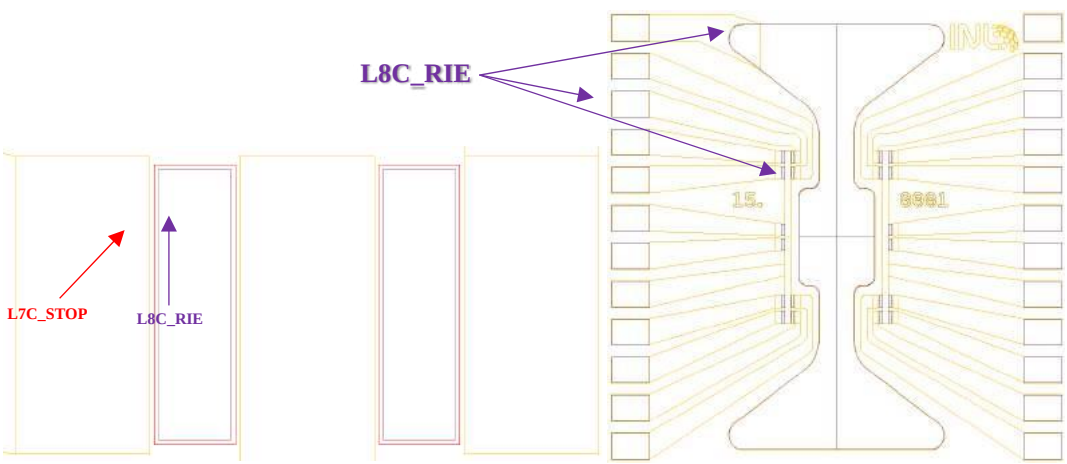


Figure 38- Resume of L8C lithography for passivation layer definition and ion milling.

a. L4CD_via (via opening and sacrificial layer definition), L5D (graphene patterning definition), L7C_STOP (stop layer definition), L8C_RIE (ion milling definition). b. Lithography mask for stopping layer definition (dark purple lines).

The etched slightly inside the stopping layer. Therefore, the exposure will be clear like for the stopping layer. Because of the long etch process that follows, a 1 µm resist is advisable, and has been used in the past.

Figure 39- Optical images of the lithography after development (chip 15.001).

Ion Milling of the passivation layer

The etch of 250 nm of SiN/SiO2 layer was performed by ion milling where we stop plasma after we see the Ni appear.

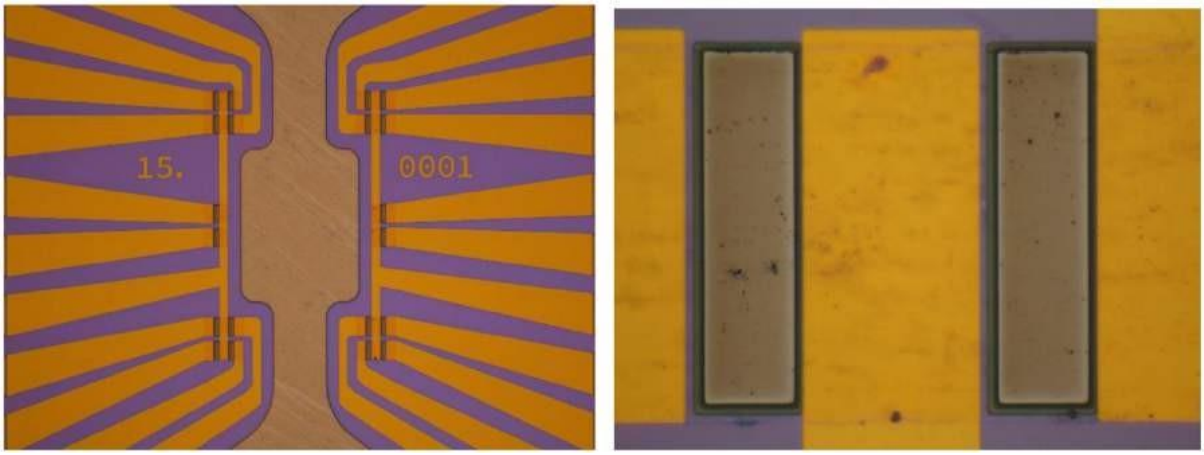


Figure 40- Optical images after ion milling (chip 15.001).

Resist strip

It is necessary to remove the photoresist at this step. Indeed, the next step will be the removal of the stopping layer, and after that graphene is exposed. This step is therefore the last where we can freely use oxygen plasma for a strong cleaning of the resist. The standard recipe low Temperature 13 min can be used, and as usual after exposure to strong processes such as RIE, it can be needed to repeat the plasma asher recipe due to resist becoming stronger.

1.2.10 Stopping layer removal and Al2O3 removal

Remaining niquel is removed by FeCl3 for 1min using agitation.

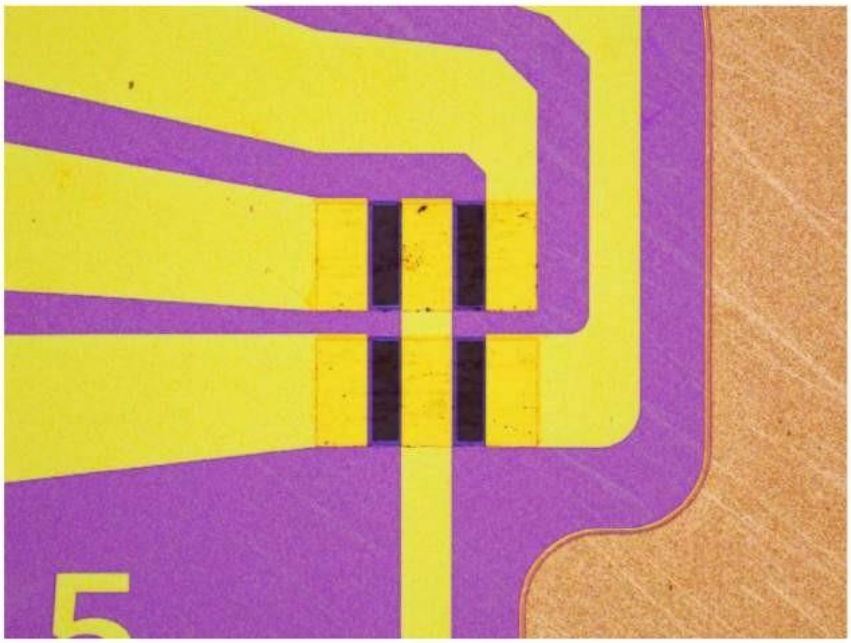


Figure 41- Optical images after stopping layer removal and passivation material removal (chip 15.001).

1.3. FUTURE STEPS FOR FINISHING

1.3.1 SEM Inspection

SEM with EDX enables to check that Ni and Al at are residual levels on graphene. This should be performed here because this is the first time we perform this process on real samples. Because SEM/EDX will contaminate the observed channels with a thick carbon layer. Scanning Electron Microscopy (SEM), FEI NovaNanoSEM 650, Hillsboro, OR, USA, is used to study surface features and energy-dispersive X-ray spectroscopy (EDX) analysis. SEM images are collected in the secondary electron imaging mode at a 5 mm working distance and an operating voltage of 5.0 or 10.0 kV, depending on the materials to be analyzed and the probing depth desired. EDX acquisition using Oxford Instruments INCA software, Oxfordshire, UK, is performed on selected regions from SEM images to confirm surface chemical composition and detect surface contaminants after completing the fabrication process.

1.3.2 Raman Characterization

Raman spectroscopy is performed to check the final status of the chips before individual cutting complicates this task. After microfabrication processes. Raman data analysis is done using WITec Project FOUR+ software, Ulm, Germany. All samples are analyzed using a 532 nm Nd:YAG laser for excitation. The laser beam with power in the range 2 to 3 mW is focused on the sample by a ×50 lens (Carl Zeiss, Jena, Germany), and the spectra are collected with a 600 groove/mm grating using 5 acquisitions each with 2 s acquisition time. Within each experiment, the laser power is fixed to allow comparison of the acquired data.

1.3.4 Electrical testing

For acquisition on the transfer curves of the fabricated EG-GFET samples, the source and drain contacts of each transistor are connected to a Keithley 4687 Picoammeter, Cleveland, OH, USA, which applied a constant (1 mV) source–drain voltage (VSD), and the source–drain current (ISD) is measured. The high-impedance gate circuit is formed between gate and source contacts. It is biased by applying a voltage (VGS) by a Keithley 2400 source meter, Cleveland, OH, USA, which is programmed to apply voltage ramps from 0.2 to 1.2 V in steps of 0.01 V. All the measurements were performed using 10 mM phosphate buffer as gate electrolyte to close the circuit. For full-wafer characterization, an automated wafer probe station is used. The graphene channels' resistance is analyzed by applying a constant voltage between source and drain (1 mV) and measuring the channel's current, using a Keithley 2400 source meter. No liquid electrolyte is added to the devices, and no gate voltage is applied (the gate

contact is left floating). Channel resistance values by the device are obtained by processing the current measurements using MATLAB scripts.

1.3.5 Dicing

Pre-coating necessary to protect graphene. In all cases we dice graphene samples at 8 mm/s with water flow half of the usual. Dicing plan includes three steps First step: separating the two areas. Only the central line is absolutely necessary, but it is better to already reduce the wafer to rectangular areas, this will facilitate the other dicing steps.

1.3.6 Wire Bonding

The chips are kept with photoresist on top. When in need for use for wire-bonding, the cleaning procedure uses quick cleaning with acetone, IPA, water to remove photoresist. A strong cleaning with ethyl acetate or DMF is used to remove all residues. This strong cleaning is repeated after wire bonding, before bio-functionalization.