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A Methodology for the Timing Performance Optimization of the Pre-amplifier Design in High Energy Physics

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The Large Hadron Collider (LHC) is going to enter a High Luminosity –LHC(HL-LHC) phase with a 6-time higher instantaneously luminosity. The increased number of interactions per bunch crossing (pile-up) is one of the experimental challenges in the front-end readout design because a much faster recovery time to the baseline (< 25ns) is required. Depleted Monolithic Active Pixel Sensors (DMAPS) draw a lot of interests to be used as a sensor for timing in High Energy Physics experiments for its advantage of integrating the sensor and the electronics on the same substrate that saves effort on labor-costly wire-bonding process.

Under this background, the design of following amplify circuit faces more constrains: First the input signal cannot be considered as a Dirac-delta pulse due to a sensor collection time of few nanoseconds, in fact it is seen as a triangular pulse in this case. Second the fall time of the output signal is not much larger than the rise time. The first one leads to no analytical solution when the convolution of the system output is Laplace reversed to the time domain. And the second one makes some simplies of the system not possible.

Thus, in this contribution, a new methodology for the front-end design is presented and the validity is tested. Here, we first simplify the pre-amplifier into a small signal model with the freedom of some parameters such as the open loop gain (A0), the feedback resistor(RF), the feedback capacitor(CF), the load capacitor(CL), the total input capacitor(CT) and so on. The transfer function of the system can be written from the small signal model, from which the time constant of the rise and fall time of the signal can be calculated. The calculation for the jitter and the noise of the circuit can be seen in [1] and [2] and is written as:

\begin{equation}
\sigma_j = \frac{e_nC_d}{Q_{in}}\cdot \sqrt{\frac{t_{rpreamp}^2 +
t_{rsensor}^2}{2t_{rpreamp}^2}}
\label{eq:jitter21}
\end{equation}

where en is the noise from the input transistor and is inversely proportional to the power consumption, Q_{in} is the total input charge and t{r_sensor} and tr_preamp are the rise time for sensor signal and pre-amplifier signal. The minimum value shows when tr_sensor is equal to tr_preamp:

\begin{equation} \sigma_j = \frac{e_nC_d}{Q_{in}}\cdot \sqrt{t_{rpreamp}^2} \label{eq:jitter22} \end{equation}

The noise of the circuit is integrated using the time constant of the rise time and the fall time because it is also shaped by the system transfer function and can be written as (only taking the thermal noise of the input transistor into account because it is the main contribution):

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\label{eq:noise_in_circuit} \equation \\ <v_{out}^2 >= v_n 2R_f 2C_T 2 \\int_0 \{+ \\infty\} \\mid\{ \\frac\{s\} \{(1 + s \\tau_r)(1 + s \\tau_f)\} \\mid2df\} \\label\{eq:noise_in\_circuit\} \\end\{equation\} \\
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from where we can see that the time constant of the rise time and the fall time need to be chosen very carefully because the noise is decided by them directly but it is not straight forward with a large phase space for the parameters. So, an optimization process has been run to find the optimal parameters with some given constrains (such as jitter, output amplitude, power consumption and etc) and in this way we fetch the suitable parameters for the requirements.

The ideal model is compared with a more realistic model in which the core amplifier is implemented with transistors and ideal biasing circuits. Simulations showed only a discrepancy of few ps between the two models (41 ps from the ideal model and 50 ps from the more realistic model). It is also possible to include the noise from the biasing circuits considering the gm of the biasing transistors. We did not include here for simplifying the calculation. In conclusion, although this simplified model does not include the noise contributions that arise from the biasing circuit, which will impact on the final jitter, it provides a very good starting point as well as the ability to run a global optimization of the desired parameters to get the most favorable possible parameters before heading to the transistor level design.

References⊠

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