

Characterization of silicon Monolithic Stitched Sensors for ALICE ITS3 in view of LHC Run 4

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The ALICE Collaboration at the Large Hadron Collider (LHC) will replace the three innermost layers of the inner tracking system during the Long Shutdown 3 in 2026-2028. The new three-layer inner tracking and vertexing system (ITS3) will consist of truly-cylindrical silicon barrels to improve the pointing resolution by a factor of two over a large momentum range and the tracking efficiency at very low transverse momenta ($p_T < 0.3 \text{ GeV}/c$).

The detector will be equipped with stitched wafer-scale monolithic active pixel sensors built using the 65 nm CMOS imaging process technology. The sensors will be thinned to $50 \mu\text{m}$ to become flexible allowing the formation of truly-cylindrical barrels with an extremely low material budget of $0.07 \% X/X_0$.

The 65 nm CMOS technology was validated with a set of test structures called Multi-Layer Reticle 1 (MLR1). Starting from mid-2023, new prototypes have been produced to

demonstrate the feasibility of the stitching process, the so-called MOnolithic Stitched Sensors (MOSS). A single chip has a dimension of $14 \text{ mm} \times 259 \text{ mm}$ and a total of 6.7 million pixels organized in 10 repeated sensor units with eight pixel matrices each: 256×256 pixels with $22.5 \mu\text{m}$ pitch in each top matrix and 320×320 pixels with $18 \mu\text{m}$ pitch in each bottom matrix. The different layouts are used to compare the yield depending on the densities and spacing margins. A denser design is implemented in the MOnolithic Stitched Sensor with Timing (MOST) containing 0.9 million pixels with $18 \mu\text{m}$ pitch distributed on a smaller area of $2.5 \text{ mm} \times 259 \text{ mm}$.

The primary goal of MOSS and MOST is to learn about the stitching technique implementation, yield and performance of wafer-scale sensors in view of the production of the ITS3 final-size full-functionality prototype sensor chip. A characterization campaign started on the stitched sensors including the verification of power domain impedances, DAC performance, pixel front-end readout response, threshold scans and fake-hit rate scans.

This presentation includes an overview of the status of the ITS3 project and will focus on the results and learnings from the characterisation campaign of the stitched sensors in the laboratory and in the test-beam facilities.

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