

Characterisation of analogue MAPS produced in the 65 nm TPSCo process

Monday 1 July 2024 18:01 (1 minute)

Monolithic Active Pixel Sensors (MAPS) combine the sensing node and readout circuitry into the same substrate, thus offering several advantages with respect to their hybrid counterparts, including reduced material budget, spatial resolution, and decreased power consumption. Nevertheless, MAPS face challenges in high radiation environments due to their relatively lower radiation tolerance and slower readout speed. Thus, MAPS are uniquely suited to environments where high granularity is the limiting factor, such as in heavy-ion collisions, or future lepton colliders such as the FCC-ee.

In the context of the ALICE ITS3 collaboration, a set of MAPS small-scale test structures were developed using a 65 nm TPSCo CMOS process with the upgrade of the ALICE inner tracking system as its primary focus. One such sensor, the Circuit Exploratoire 65nm (CE-65), and its evolution the CE-65v2, were developed to explore charge collection properties for varying configurations including collection layer process (standard, blanket, modified with gap), pixel pitch (15, 18, 22.5 μm), and pixel geometry (square vs hexagonal/staggered).

In this contribution the characterisation of the CE-65v2 chip, based on Fe-55 lab measurements and test beams at CERN and DESY will be presented. Focus will be given to the study of charge collection properties, pixel input capacitance, and pixel-by-pixel gain variations observed in lab tests. Subsequently, the position resolution, detection efficiencies, and the radiation tolerance of the different chip configurations will be detailed, as well as their dependence on process modifications, pixel pitch, and pixel geometry. The results will be considered also through the lens of future e+e- colliders, where it is shown that MAPS are a promising candidate.

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Session Classification: Poster Session