# Characterisation of analogue MAPS produced in the 65 nm TPSCo process


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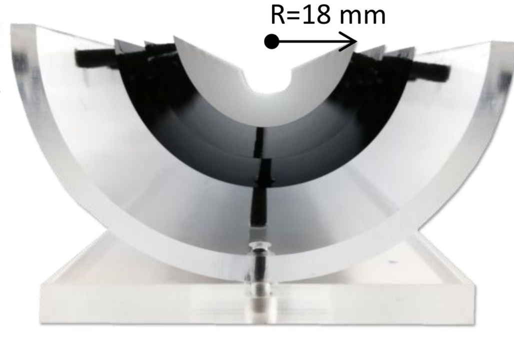
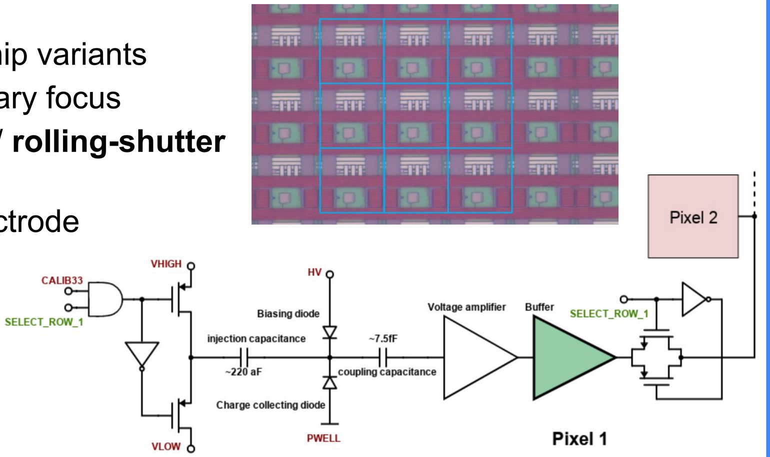
## ALICE ITS3

- **ALICE Inner Tracker System upgrade (ITS3)** will be **installed** during **LHC LS3** from 2026-2028
  - **3 inner layers of ITS2** MAPS will be replaced by **fully cylindrical inner layers**
- Fully cylindrical layers rely on stitching available in TPSCo 65 nm CMOS imaging process
- **20 μm** pointing resolution ($p_T$=1 GeV, η=0) will be reached thanks to
  - Excellent **spatial resolution**
  - **Low material budget** (0.09% $X_0$/layer) relying on **air cooling**, minimal support structures
- First submission for test structures **MLR1** in December 2020
  - Small-scale prototypes: **APTS**, **DPTS**, **CE-65**
- Second submission for MOnolithic Stitched Sensor (MOSS) **ER1** in 2022
  - Learn and study properties of **stitched sensors**
  - Evolution of some MLR1 prototypes, including **CE-65v2**



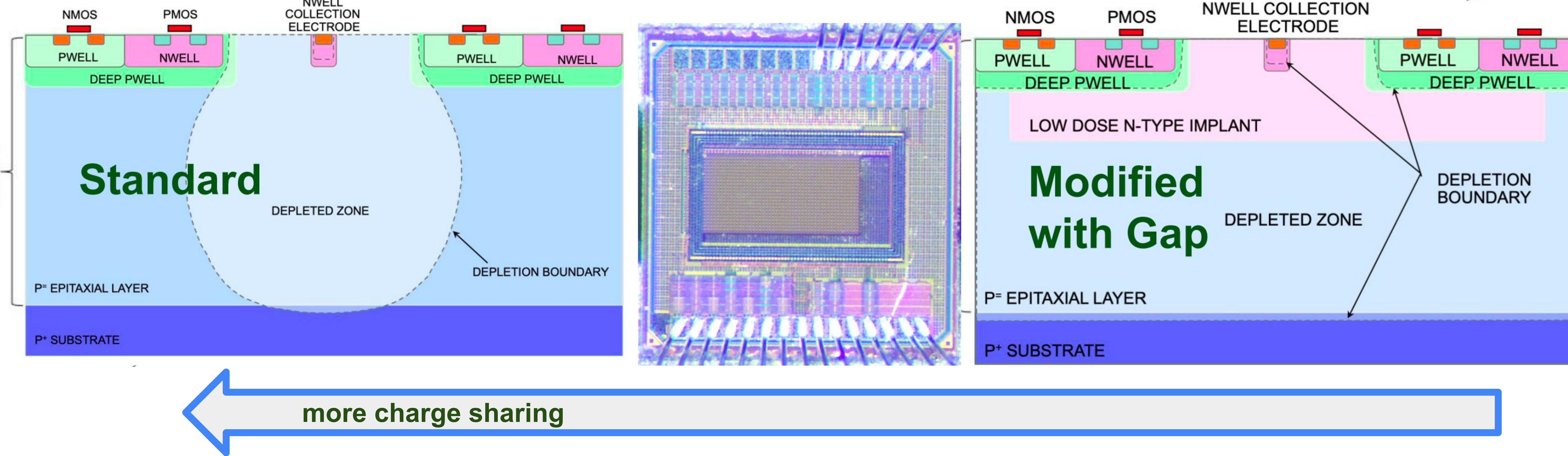

## CE-65v2

- The **Circuit Exploratoire 65nm v2** (CE-65v2) developed by IPHC Strasbourg using a 65 nm commercial CMOS process
  - Explore **charge collection** and **electrical properties** of chip variants
  - **Upgrade of the ALICE inner tracking system** as its primary focus
- **Matrix of 1152 pixels** organized in 48 columns and 24 rows w/ **rolling-shutter readout**
- **AC-coupled amplifier** allows HV bias directly at collection electrode
- 15 variants of CE-65v2 chip
  - **Process variation**: Standard, Modified, Modified w/ Gap
  - **Pitch variation**: 15 μm, 18 μm, 22.5 μm
  - **Matrix geometry**: square vs hexagonal/staggered




## Standard Process

- **Standard process** with n-well collection electrode and in-pixel CMOS circuitry isolated from epitaxial layer by deep p-well
- **Balloon shaped depletion region** centered at collection electrode
- Undepleted lateral region due to limited epitaxial region O(10 μm) results in **diffusion-dominated charge collection**
  - **Slow** and subject to **charge trapping**
  - **High charge sharing**

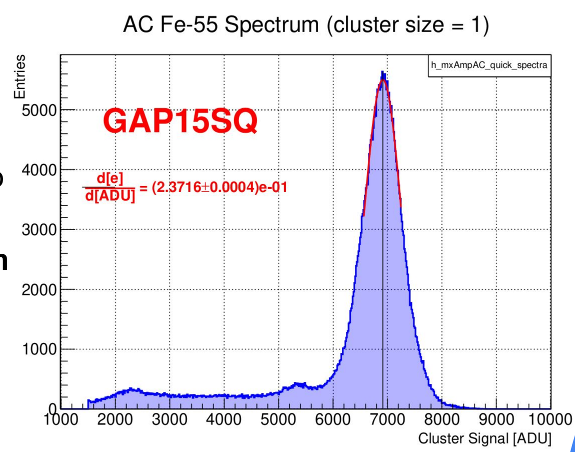



## Modified with Gap Process

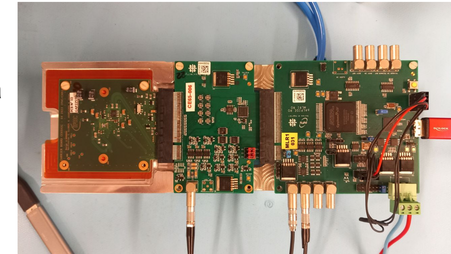
- **Modified with Gap process** in addition has a **deep low-dose n-type implant** between epitaxial layer and CMOS circuitry, w/ **gaps** at the pixel edges
- **Depletion region extends laterally**, with gap enabling development of electric field
- Lateral electric field results in **drift-dominated charge collection** even at edges
  - **Fast**
  - **Low charge sharing**

## Lab Tests

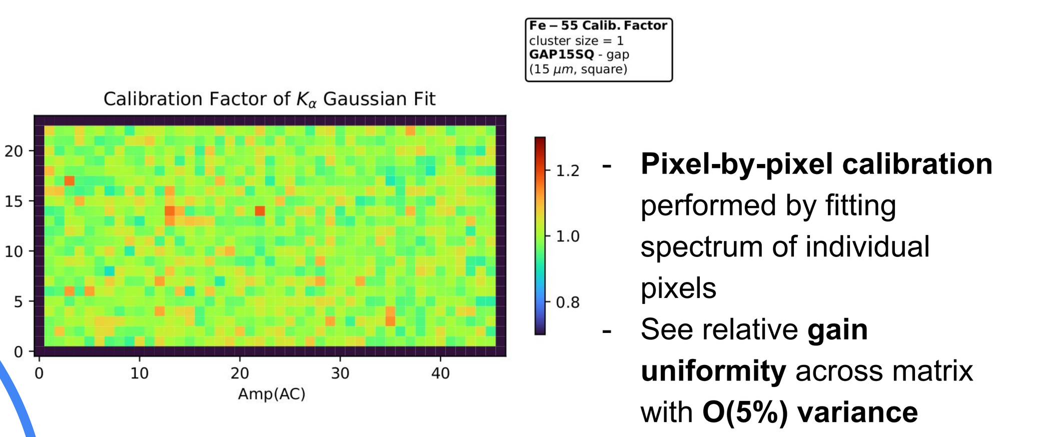
- Fit Fe-$K_\alpha$ emission line with **single Gaussian** to extract peak position
- Allows **conversion from ADU to known energy (5.90 keV)**




Conducted lab tests using setup consisting of
- **DAQ board** based on Altera Cyclone IV FPGA
- **Proximity board** providing all chip biasing
- Carrier board housing **CE65v2**



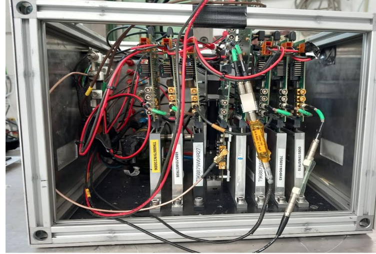
- **O(150 MBq) Fe-55 Source** used to conduct tests
- Standardized w/ chiller at **20ºC**



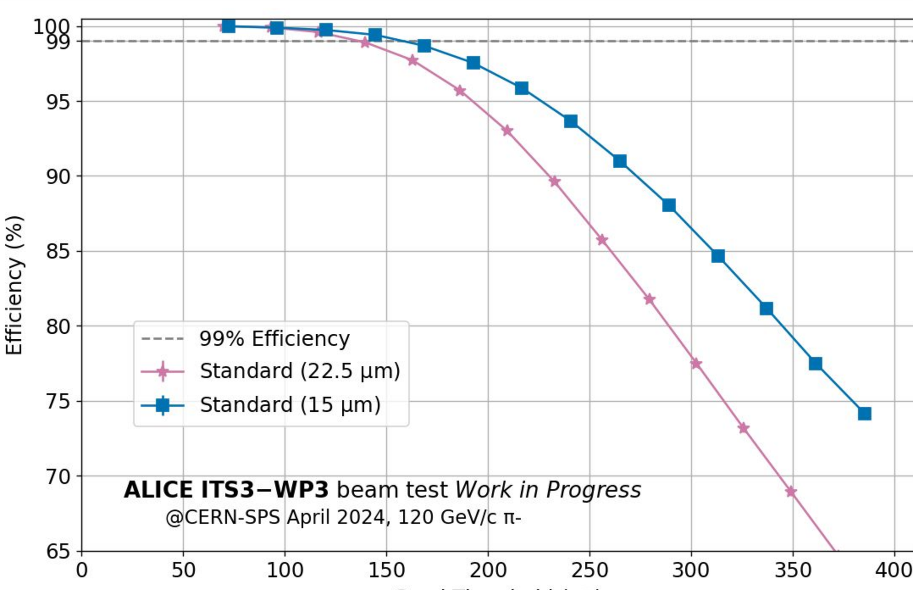

- **Pixel-by-pixel calibration** performed by fitting spectrum of individual pixels
- See relative **gain uniformity** across matrix with **O(5%) variance**

## Testbeam

- Conducted test beam at CERN SPS using **120 GeV/c pion beams**
- Study **charge collection efficiency** and **resolution** of different CE-65v2 variants



- Telescope consisting of **6 ALPIDE planes** and using **DPTS as trigger**
- Achieved a **2.2 μm telescope resolution**

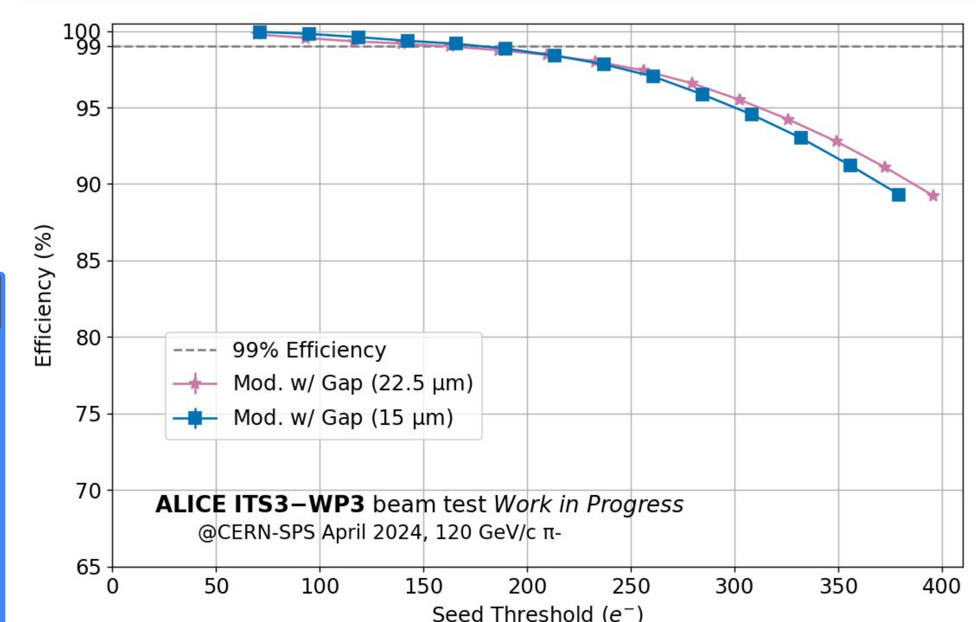



## Efficiency (Standard)

- **Standard process sensors** with **15 μm** and **22.5 μm** pitch
- **Charge collection efficiency** as a function of **threshold in e⁻**
- Efficiency remains over **99%** up to **~130 e⁻** and **~150 e⁻** for 15 μm and 22.5 μm pitch
- Both pitches drop in efficiency wrt threshold, but 22.5 μm does so faster

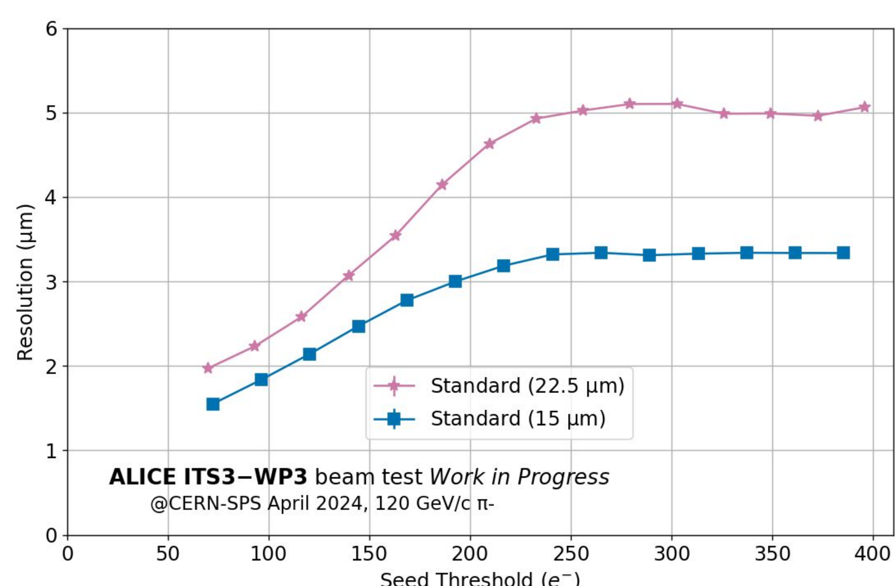
## Efficiency (Mod. w/ Gap)

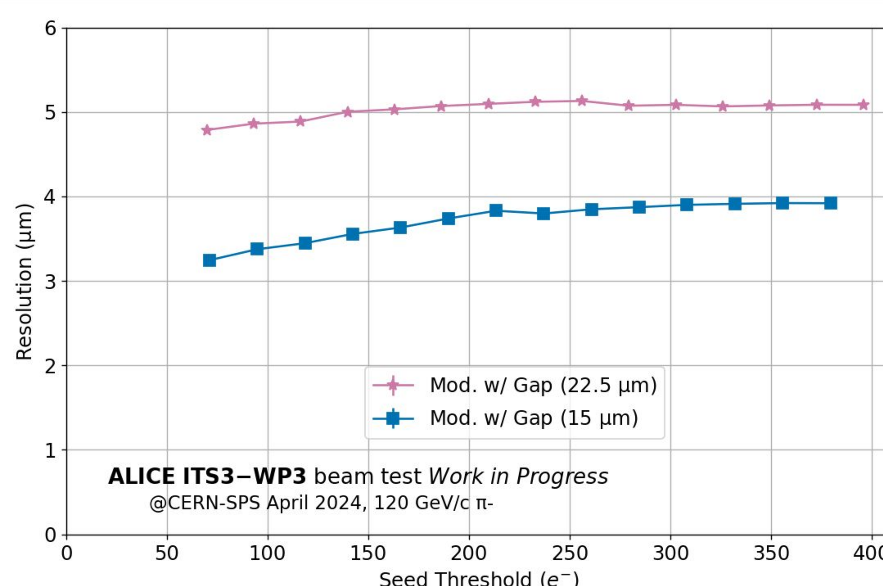
- **Modified with Gap process sensors** with **15 μm** and **22.5 μm** pitch
- **Charge collection efficiency** as a function of **threshold in e⁻**
- Efficiency remains over **99%** up to **~180 e⁻** for both 15 μm and 22.5 μm pitch
- Efficiency drops more slowly for Modified with Gap process
- Little dependence on pitch size




## Resolution (Standard)

- **Standard process sensors** with **15 μm** and **22.5 μm** pitch
- **Position resolution in μm** as a function of **threshold in e⁻**
- Full analogue information used to build **centre-of-mass position**
- **Excellent resolution** at low e⁻ thresholds with **~1.5 μm** and **~2 μm** for 15 μm and 22.5 μm pitch
- **Performance degrades very quickly in ~50-250 e⁻ range** and plateaus at ~3 μm and ~4 μm for 15 μm and 22.5 μm pitch (still considerably **better than binary resolution**)



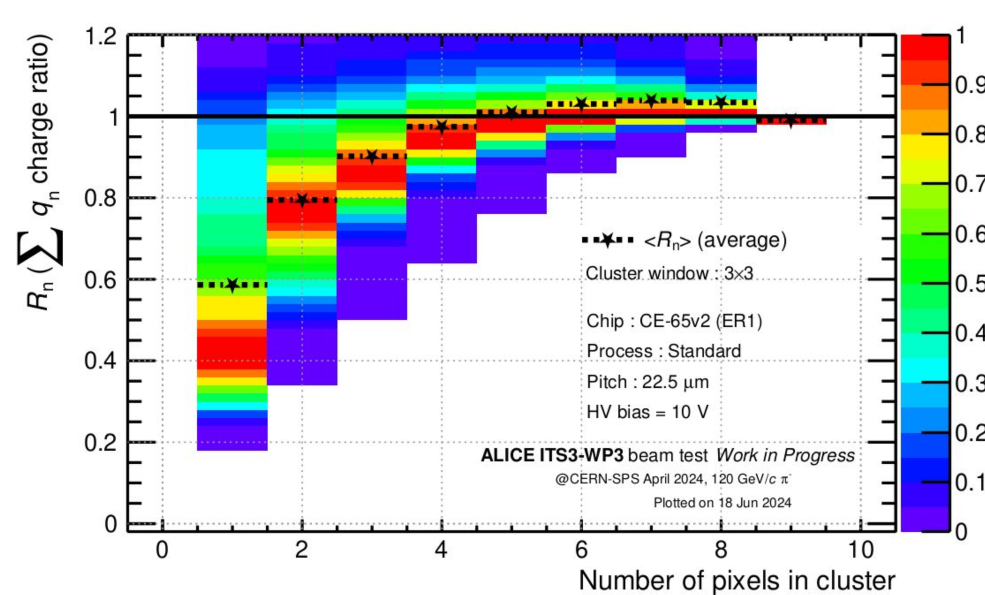



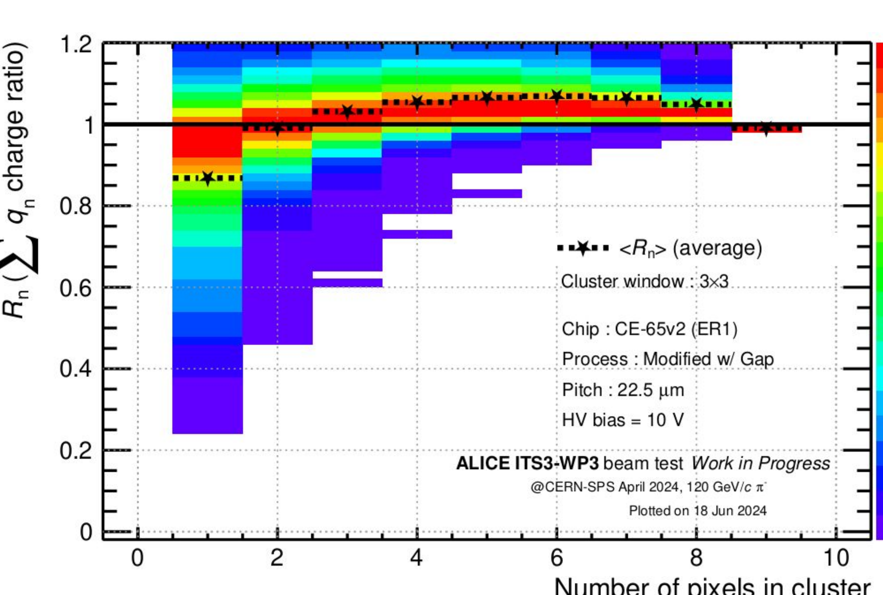

## Resolution (Mod. w/ Gap)

- **Modified with Gap process sensors** with **15 μm** and **22.5 μm** pitch
- **Position resolution in μm** as a function of **threshold in e⁻**
- Full analogue information used to build **centre-of-mass position**
- Achieve **worse resolution for all considered thresholds** especially for 15 μm, but performance **more stable**
- Less variation for 22.5 μm with resolution increasing slightly to just above 5 μm, in parity with Standard process

## Charge Sharing (Standard)

- **Standard process sensor** with **22.5 μm** pitch
- **Accumulated charge ratio** as a function of **number of pixels in cluster**
- **Seed threshold of ~100 e⁻** used
- **Average charge fraction** carried by central pixel **less than 60%**
- **Most extreme charge sharing** for **Standard process in 22.5 μm pitch**
  - Competing effects of **larger pitch** -> more charge collected due to larger area
  - **Electric field does not propagate well at edges** -> more charge diffusion at edges




## Charge Sharing (Mod. w/ Gap)

- **Modified with Gap process sensor** with **22.5 μm** pitch
- **Accumulated charge ratio** as a function of **number of pixels in cluster**
- **Seed threshold of ~100 e⁻** used
- **Average charge fraction** carried by central pixel **over 85%**
- **Lowest charge sharing** for **Modified with Gap process in 22.5 μm pitch**, due to large pitch

## Conclusion

- Achieve **excellent resolution** in large-matrix 65 nm CMOS process test structures
  - **Sub 3 μm spatial resolution** satisfies **FCC-ee requirements** for Standard process at both 15 μm pitch and 22.5 μm pitch
  - Must be operated in **low e⁻ threshold regime**, subject to radiation defects
- Achieve **wide range of operation** for **Modified with Gap process**, 99% efficiency achieved at ~180 e⁻ for both 15μm and 22.5 μm pitch
  - More suited for high-radiation environments

## Outlook

- **Future of CE65 project:** Many on-going testbeam analyses
  - Study effect of hexagonal pixel arrangement in large matrix on cluster size, resolution
  - Study effect of varying HV bias voltage on depletion, resolution, efficiency
  - Radiation tolerance currently under study
- **Future of ALICE ITS3 project:**
  - Ongoing stitched sensor characterisation and testing

## References


- ALICE Collaboration, Technical Design report for the ALICE Inner Tracking System 3 - ITS3 ; A bent wafer-scale monolithic pixel detector, https://cds.cern.ch/record/2890181
- Szymon Bugiel et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, https://doi.org/10.1016/j.nima.2022.167213
- ALICE Collaboration, First measurements with monolithic active pixel test structures produced in a 65 nm CMOS process, https://doi.org/10.1088/1748-0221/19/02/C02017