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A High Accuracy CMOS Peak Detection and Holder ASIC for Neutron Detectors

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With the completion and operation of a series of high-performance neutron sources, such as the China Spallation Neutron Source (CSNS), various neutron scattering spectrometers have continuously increased their performance requirements. One important aspect is to reduce collisions between scattered neutrons and air molecules during neutron scattering experiments, thereby reducing background noise and obtaining highly accurate experimental measurement results. This paper presents an application-specific integrated circuit (ASIC) dedicated to position-sensitive Helium-3 tubes neutron detector, which introduces peak detection and holder (PDH) circuits on the basis of traditional front-end electronics. Through a specific design, the switches and holding capacitor of the PDH module are isolated, ensuring that the holding voltage is not affected by switch noise, and maximizing the measurement accuracy of the PDH module. The 8 channel ASIC, realized in 0.18 um CMOS technology, has a 10fC to 1pC input signal range with a linearity error within -0.1 to +0.09%, measured at 180 ns peaking time. The PDH module is supplied with a single voltage of 1.8 V with a total power consumption of 190 uW with a layout area of 361 um × 68 um. The ASIC further enhances system integration, allowing the analog-to-digital conversion module to employ low-speed ADCs, thereby reducing the overall power consumption of the readout system. This enables the entire detector to operate in a vacuum environment, providing a new electronic readout solution for future neutron scattering and imaging experiments.

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