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A prototype readout integrated circuit for energy-resolved hybrid pixel detector.

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A significant advantage of single-photon counting (SPC) systems, in comparison to integrating ones, is their ability to discriminate photons by their energy. This enables, among others, so called 'color imaging', i.e. radiography with photon energy differentiation. It can provide a notable enhancement in medical diagnostics, facilitating the differentiation of the x-rayed structures. This, however, requires employment of dedicated readout electronics, which can reliably measure the photon energy, fulfilling a set of rigorous requirements, including low power and area consumption, and high uniformity of recording channel main parameters.

Here we present a prototype integrated circuit (IC) of a multichannel readout electronics for energy-resolved hybrid pixel detectors, working in the SPC mode. The IC is equipped with 100 pixels of 50 μm $\times$ 50 μm, each of which incorporates a charge-sensitive amplifier (CSA), a discriminator, an analog-to-digital converter (ADC) and a digital counter. The ADC compensates charges collected at a plate of the CSA's feedback capacitor, injecting a series of short current pulses to it. Since the number of pulses needed to completely discharge the capacitor is directly proportional to the charge, the energy of a detected photon can be measured by simply counting the pulses. Additionally, this process accelerates the CSA baseline restoration, increasing the maximum count rate. The ADC works asynchronously, which has positive impact on the conversion speed and power consumption. The resolution of the ADC can be modified by adjusting the current pulse amplitude. In the presented solution we use the whole 12-bit counter to count the discharging pulses. The advantage of this approach is the ease of increasing the resolution by lowering the amplitude of the current pulse, reducing its width and increasing the number of counter bits. The limitation, however, is noise.

During data readout, all the digital counters are connected together and transformed into one long shift register. To speed up the process, a sparsification method has been implemented in the IC, allowing the bypassing of empty pixels while shifting the data.

The measurements we have made so far revealed power dissipation lower than 17 μW/pixel while working with input pulses of 360 kHz. The channel gain is about 20.7 μV/e$^-$, allowing for the registration of energies up to 140 keV, assuming CdTe sensor. The least significant bit (LSB) of the 12-bit counter corresponds to approximately 33 e$^-$.

The article will proceed to examine the interrelation between conversion resolution and speed, as well as the useful measurement range.

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