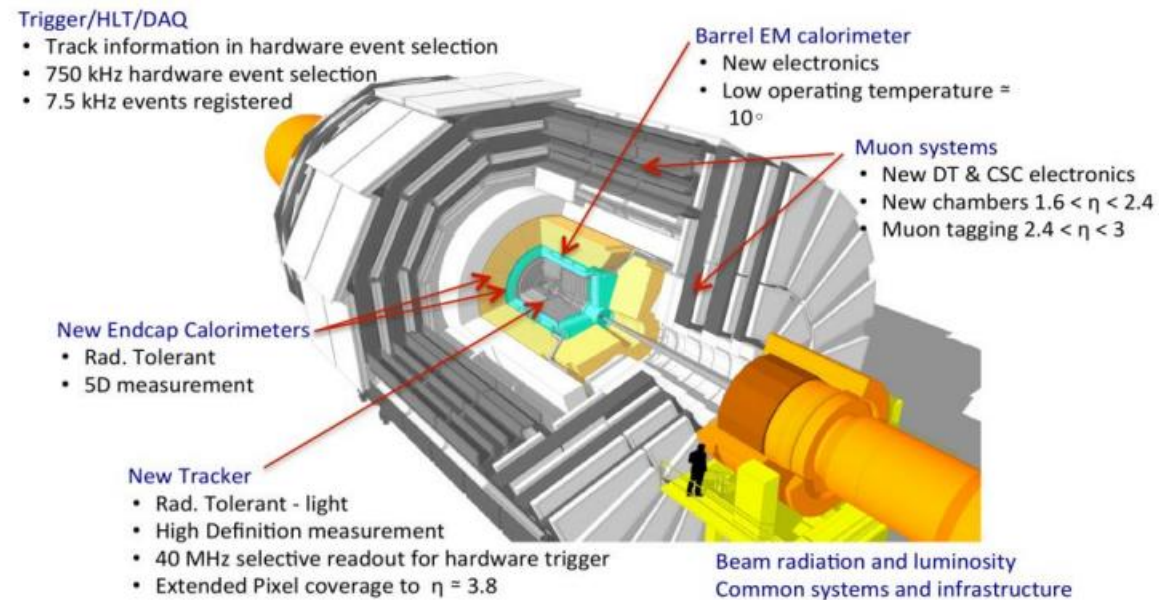


CMS Inner Tracker DAQ and System Tests

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- High Luminosity LHC (HL-LHC):
 - LHC upgrade that will increase the rate of collisions
 - Detector upgrades are needed to support the increased hit rate and radiation
- CMS Phase-II upgrade:
 - Major upgrade of CMS planned for HL-LHC
 - New tracker design:
 - Increased radiation tolerance
 - Higher granularity (more channels, smaller pixels, etc.)
 - Lower mass
 - Contribution to Level-1 Trigger (Outer Tracker only)
 - Extended coverage ($0 < \eta < 4$)

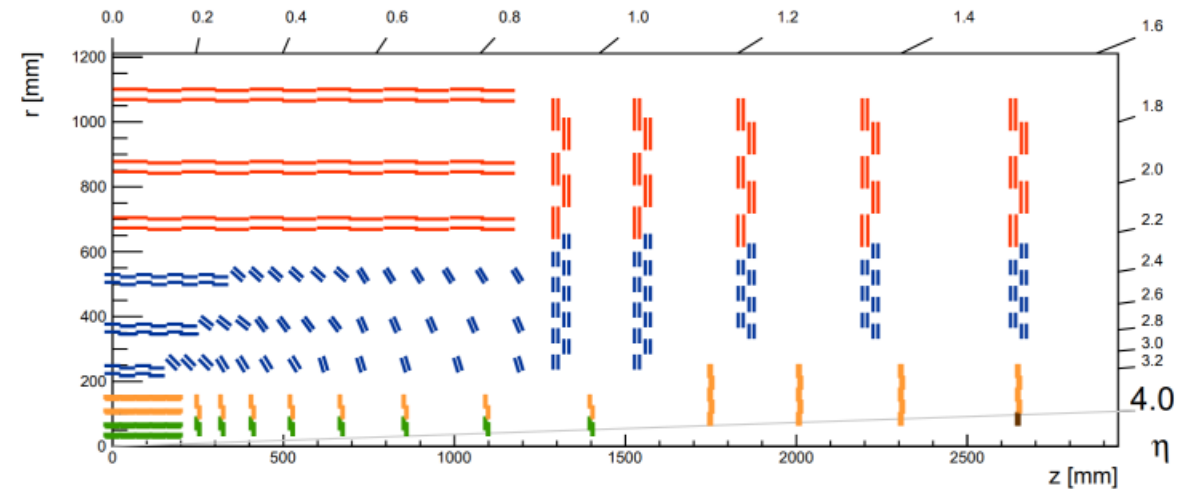
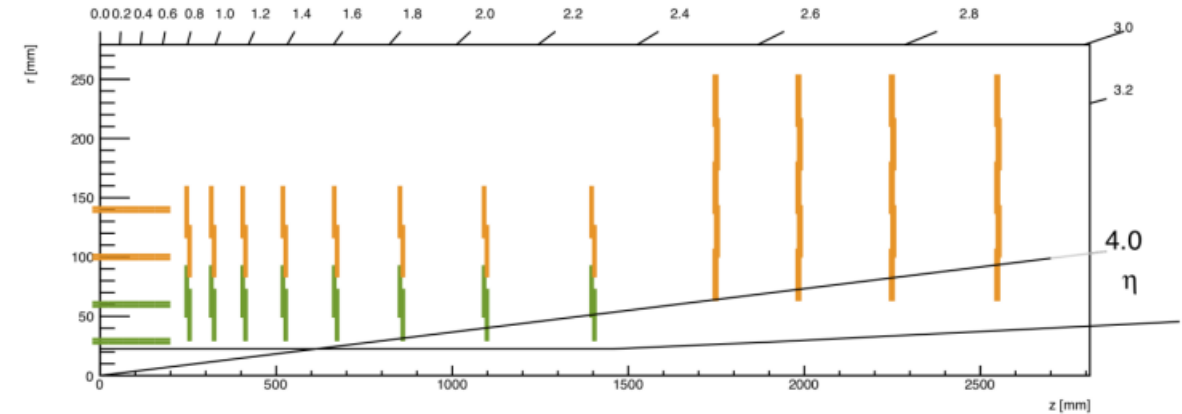


- Inner Tracker:

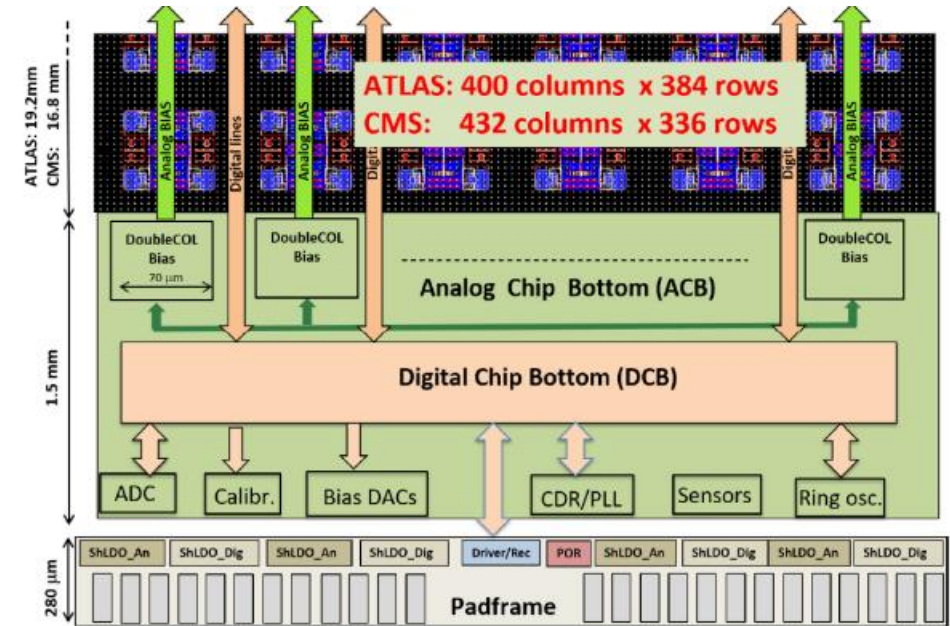
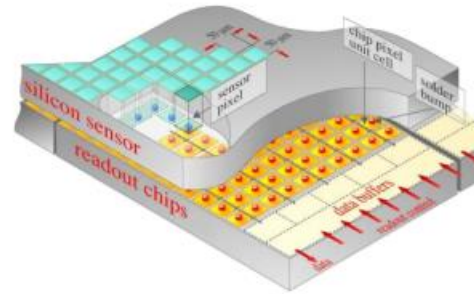
- Innermost layer of CMS, right off the beam pipe
- Silicon pixel detectors, 50 μm pitch
- 10000 readout chips, 3900 hybrid modules
- ~ 2 billion channels, 1342 links @ 10 Gbps
- Modules consist of **1x2** or **2x2** chips

- Outer Tracker:

- Largest part of the tracker
- Double sided hybrid modules:
 - 7608 **Strip-Strip** (2S) and 5592 **Pixel-Strip** (PS) modules
- Each module detects and transmits high p_T track segments (stubs) in real time



- Hybrid module design:
 - Separate sensor and readout chips
 - Flip chip assembly with bump bonding
- Readout chips developed by the RD53 Collaboration (CMS + ATLAS):
 - 65 nm process (TSMC)
 - RD53A**: Half-sized demo version, extensively tested
 - CROCV1**: Full-sized (336 x 432 pixels) pre-production prototype, received Sep `21
 - Final version to be submitted this year



Phase-1		HL-LHC
Rate 400 MHz/cm²	× 8	Rate 3.2 GHz/cm²
L1 rate 100 kHz	× 7.5	L1 rate 750 kHz
Latency 3.2 μs	× 4	Latency 12.8 μs
Radiation ~100 Mrad	× 10	Radiation ~1.2 Grad

→ **×60 Bandwidth**
→ **×32 Buffers**

- The readout and control of the future front-end modules of the CMS Tracker, will be performed by the DAQ, Trigger and Control (DTC) System.
- The μ DTC project was established to perform these tasks in the prototyping and production phases.
- Common framework for Outer Tracker (OT) and Inner Tracker (IT) based on FC7 board and IPBus* - this presentation focuses mostly on Inner Tracker implementation (IT- μ DTC).



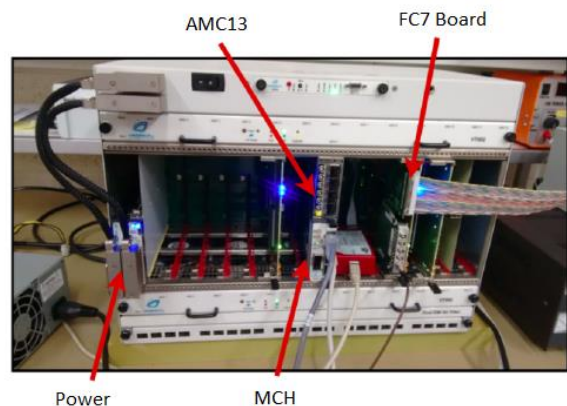
❖ **Demokritos has undertaken the responsibility to develop and maintain the DAQ for the Inner Tracker System Tests**

- *Software in C++ and Python*
- *Firmware in VHDL*

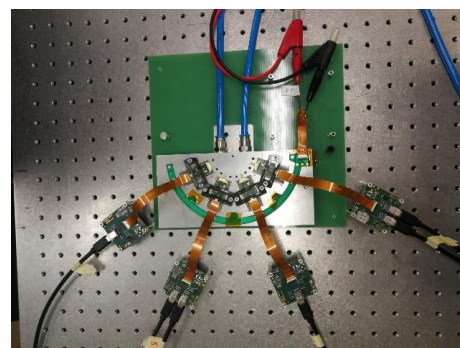
*IPBus: Ethernet-based communication protocol, developed by CERN.

IT- μ DTC will form the basis for the final DAQ System of the Tracker and provides support for various systems:

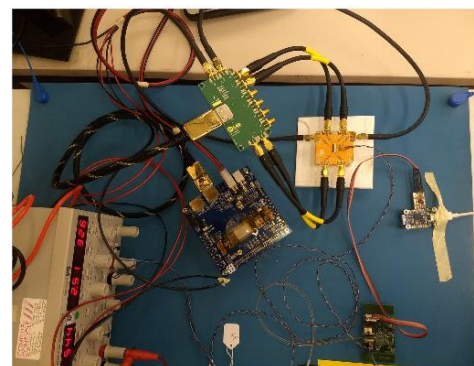
- Chip testing and characterization
- Hardware characterization
- Beam Tests
- Wafer Probing
- Multiple design flavors to support
 - Crate or Desktop operation, Optical or Electrical link, Single Chips or Modules, RD53A or CROCv1 chip



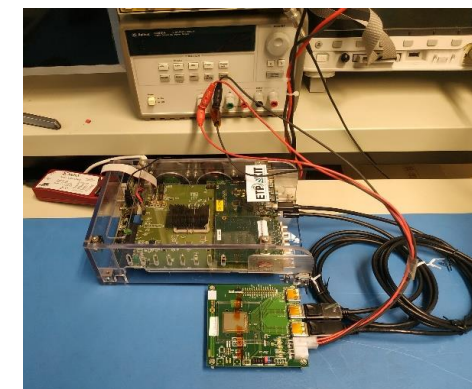
uDTC setup in Crate-mode operation



Setup with Quad-modules



Setup with optical link

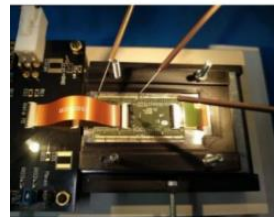


INPP DIL setup with SCC and RD53B on electrical link (Desktop-mode)

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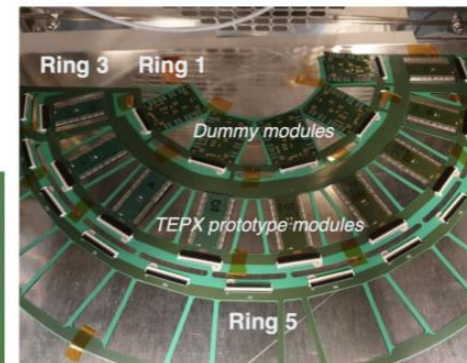
Quad module



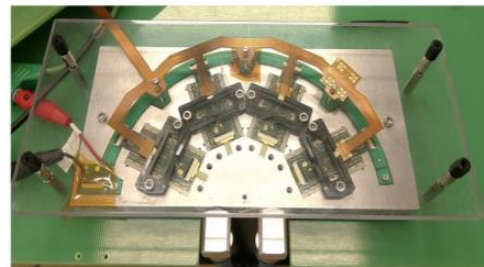
Two TBPX CF ladders readout by TWP



TEPX disk equipped with dummy & RD53A quad modules



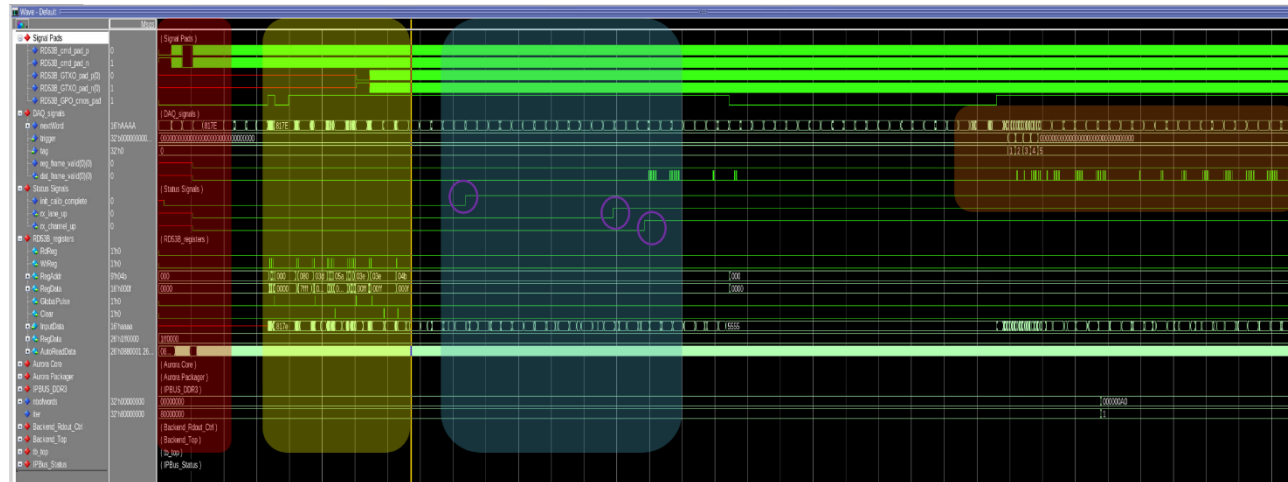
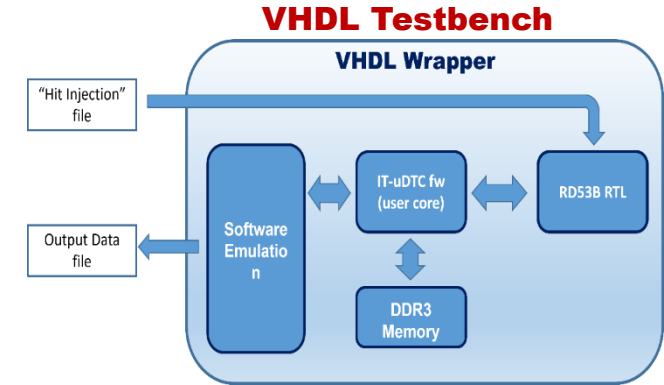
Double module



TFPX ring powered by Alu flex and readout by Cu flex

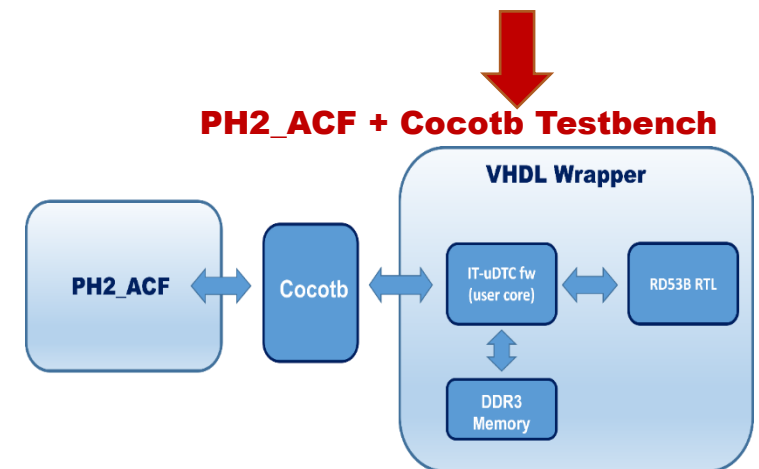
In order to facilitate the development of the DAQ, a framework for co-simulation of DAQ + RTL of the chip in Questa simulator for past and future chips has been established

- Testbench originally implemented in VHDL
- Migrating to Cocotb to allow more advanced verification including the software in the simulation chain
 - Cocotb is a python-based simulation framework



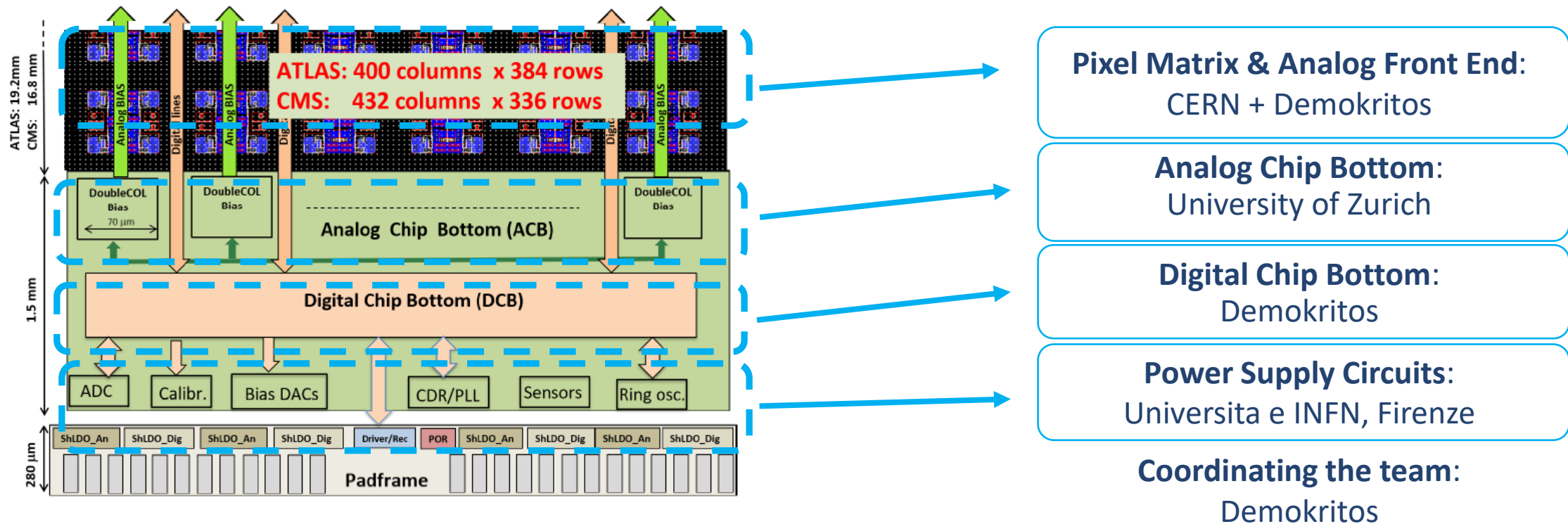
Initialize CDR circuits **Initialize uplink & downlink** **Communication Established**
 - DDR3 Calibration done
 - Aurora Lane/Channel up

Hit-Data



For the new version of the CMS readout chip, Demokritos is leading the team for the characterization of the ASIC.

- CROCv1 is a versatile ASIC:
 - Hundreds of global configuration parameters, various monitoring and calibration features
- Comprehensive suite of tests has been developed to characterize it



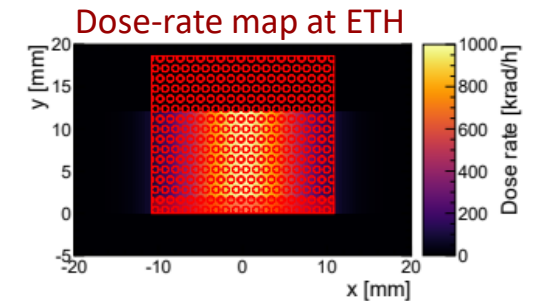
During Lab-tests, the performance of the ASIC is evaluated under different conditions, mostly in bare-chip configurations (i.e., without a sensor).

➤ X-Ray Irradiation Campaigns

- Radiation tolerance is one of the most important aspects of the chip
- CROC needs to survive after a TID of at least 1 Grad
- Various tests performed before, during and after irradiation to verify that the performance is still acceptable



X-Ray setup



➤ Climatic Chamber Campaigns

- Various parameters of the chip are affected by temperature
- Dedicated studies with Climatic Chamber in Demokritos facilities
- Controlled environmental conditions with temperature ranging between -40C to +40C



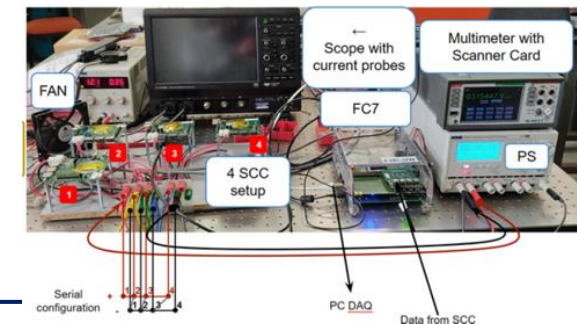
CROC SCC



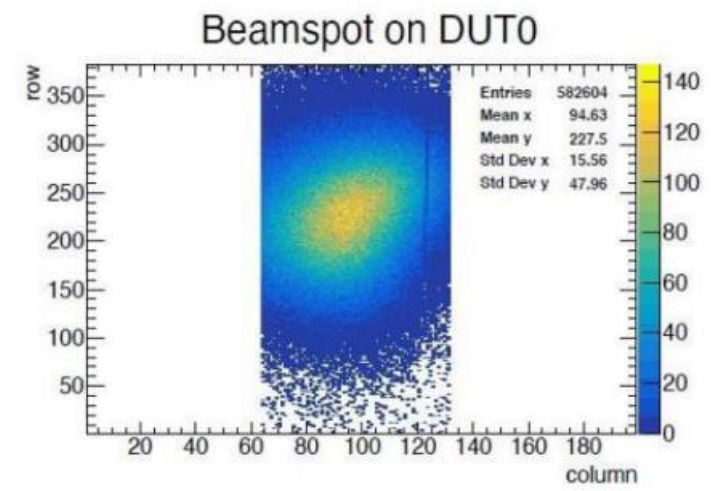
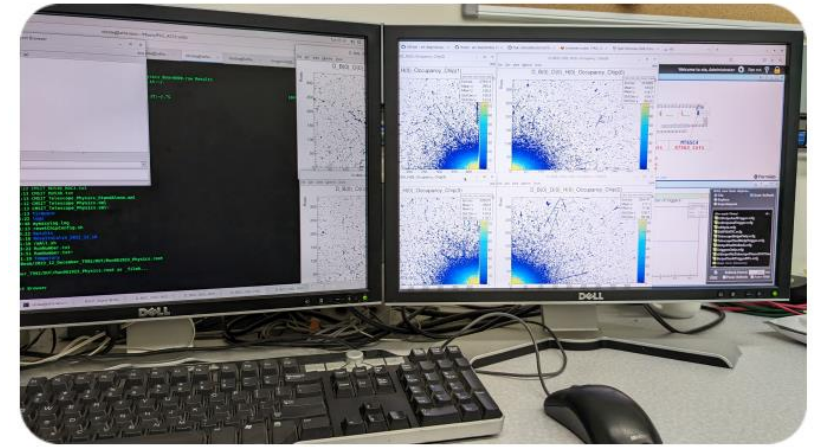
Climatic Chamber

➤ Multi-chip module system tests

- Detector-like configurations with chips assembled in 1x2 or 2x2 modules
- Serial Powering tests



- Test beams provide an opportunity to demonstrate the ability of the modules to detect particles efficiently
- CROC modules have been tested under particle beams at various accelerator facilities:
 - CERN North Area
 - DESY
 - Fermilab
- Various configurations have been tested:
 - Different sensors
 - Different telescope setups
 - Different angles of incidence



“DEMOKRITOS” is involved in the following activities regarding CMS Inner Tracker Upgrade

- **Development of the DAQ for the prototyping and production stages**
 - Hardware validation and extensive tool-set for signal integrity studies
 - Wafer Probing for production testing of ASIC
 - Framework for co-simulation of DAQ + RTL of past and future chips

- **Testing and characterization of CMS Readout chip (CROC)**
 - Lab-tests (X-ray campaigns, temperature studies, performance evaluation)
 - Beam tests

- **Required skills to contribute:**
 - At least one of the following
 - Good knowledge of C++ and/or Python
 - FPGA design using VHDL

Backup