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Reduction of setup time in wafer sort process before integrated circuit packaging

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The purpose of this research aims to reduce of setup time in wafer sorting before integrated circuit packaging. To add hardware respectability detection process without prober setup before correlation wafer check process with modification of test program and making up a tool kid. Then, the experimental data was correlated with the respect range. Finally, this setting up was limited that it will be the reference for detection of respectability functioning test hardware. The results showed that the tool achieves for test hardware respectability detection. By our methodology, it will apply to other wafer test hardware and it could clearly reduce wafer sort setup time.

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