

Type: **Oral**

The Cosmic Muon Veto Detector (CMVD) at TIFR, Mumbai, will be made of extruded plastic scintillators and SiPMs and require an efficiency of 99.99% or better and a false count rate of  $10^{-5}$  or lower. To achieve this goal, a suitable high-speed, low-noise electronic DAQ system is required. The SiPM signal will be used for charge measurement for the detection of muons, whereas the trigger will come from the RPC detectors. However, the original analog signal from the SiPMs will be lost by the time the DAQ system triggers the acquisition process due to trigger generation delay and latency, and charge measurement will not be possible. Hence, a suitable temporary storage system is required to hold the signal long enough for the trigger to be generated and the data acquisition process to start. We have found that the DRS4 chip, developed by PSI, Switzerland, is a good candidate for this analog signal storage application, which can operate up to  $5\text{ GSa/s}$  with  $1\text{ V}_{p-p}$  input span and has 1024 cells to sample and hold the analog signal. Since a typical SiPM pulse has a rise time of  $8 - 10\text{ ns}$ , a pulse width of about  $100 - 150\text{ ns}$ , and an amplitude of  $20 - 200\text{ mV}$ : a sampling time of  $1\text{ ns}$  is good enough for this application, and hence the DRS4 can be operated at a speed of  $1\text{ GSa/s}$ . However, a proper offset correction mechanism is required, where individual offset for every cell has to be determined and must be subtracted from the signal. When paired with a suitable ADC and fast processing electronics, and after proper offset correction, it is possible to achieve the full dynamic range required to cover the full spectrum of muon pulses ( $\sim 30\text{ pC}$ ) at the required least count of  $0.1\text{ pC}$  for the calibration of SiPM.

## Field of contribution

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**Track Classification:** Future experiments and detector developments