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Design of fast settling SFA and ALLF controlled 4th order Phase locked loop using Simulink

Analysis of phase lock loop (PLL) using Simulink is an efficient method. Designing a PLL on a chip is a tedious process as it requires a lot of sums to fabricate it and consume months of time for development. Hence, we need another alternative to know whether the design will work or not and so Simulink is the preferred choice. SIMULINK provides a platform for graphical editing of blocks, managing them, libraries for predefined models and simulation of complex systems and rectification if required. We use such advantages of SIMULINK for deep analysis of PLL. Here, we discuss, analyse, design and discover uses of PLL using SIMULINK. In this work, we focus on designing a 4th order PLL using basic foundation blocks such as phase detector (PD), active loop filters such as: active -Standard Feedback Approach (SFA) and Active Lead-Lag Filter (ALLF) and voltage-controlled oscillator (VCO). Further we simulate and analyse certain criteria's such as settling time (ST), loop bandwidth (BW) and phase margin (PM) for checking performance of the PLL. The fastest ST for SFA controlled PLL and ALLF controlled PLL is observed to be 0.431nS and 1.32nS respectively. As such, the SFA controlled PLL provides faster ST and consequently faster acquisition with an improvement of 67.34% over ALLF controlled PLL. Also, both the systems result in improved stability in terms of PM. We have found out the output of VCO, PD, SFA and ALLF in simulink of the PLL model which provides essential response and hence improves the dynamic characteristics of both the system.

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