Contribution ID: **308** Type: **Poster**

Design of Readout Electronics for the Cosmic Muon Veto Detector

Monday 12 December 2022 14:00 (1 hour)

A Cosmic Muon Veto Detector (CMVD) is being built around the existing RPC-based Mini-Iron Calorimeter (Mini-ICAL) to study the feasibility of a shallow depth neutrino experiment. The CMVD uses 4.5 m long extruded plastic scintillator strips. A Di-Counter made up of two extruded scintillator strips, is the basic building block of the CMVD. Two fibers embedded along the length of the strips are used to carry the scintillation photons to both the sides, where Hamamatsu made SiPMs (S13360-2050VE) sense photons and produce pulse with a charge proportional to the energy deposited by the passing Muon. A total of 380 Di-Counters will be required to cover four sides of the Mini-ICAL. The front-face of Mini-ICAL is not covered by CMVD for operational reasons. Each Di-Counter consists of 8 SiPMs which adds up to 3,040 readout channels. A charge resolution of 10 fC and a dynamic range of 100 pC are required to identify and veto true muon events from the background signals in SiPM.

The proposed readout electronics system will acquire charge and timing information from all the 3040 SiPMs on Mini-ICAL trigger. The extrapolated muon trajectory will be compared with the signal in CMVD to measure the veto efficiency. A Data Acquisition (DAQ) module is being designed to readout 40 SiPM channels. The raw SiPM signals are transmitted to the DAQ module using HDMI cables. DAC generated bias voltage for SiPMs is supplied using the same cable. Each of the SiPM signals is first amplified with a trans-impedance amplifier of gain 1200Ω and its pulse profile is digitised at 1GHz using a DRS4 ASIC. Since a DRS4 channel has 1024 cells, the SiPM pulse profile for the last 1024 ns (˜1 µs) is available at any point of time. Considering a mini-ICAL trigger latency of 300 ns, a digitization window of more than 100 ns is available for muon pulses from CMVD detector. A 12-bit pipelined ADC is used to digitize the pulse profile of the SiPM signals. A zero suppression logic is used to filter data from channels with no hits. An Ethernet controller interfaced with an FPGA is used to handle the data communication between the DAQ module and a backend server.

This paper will briefly introduce the CMVD detector. A detailed description of the readout scheme of the detector along with the expected performance parameters of the scheme will be presented.

Session

Future Experiments and Detector Development

Author: ELANGOVAN, Yuvaraj

Co-authors: Mr DEODHAR, Aditya (Tata Institute of Fundamental Research); MAJUMDER, Gobinda (Tata Inst. of Fundamental Research (IN)); SARAF, Mandar (Tata Institute of Fundamental Research); BHEESETTE, Satyanarayana; Mr SHINDE, Ravindra Raghunath (TATA INSTITUTE OF FUNDAMENTAL RESEARCH, MUMBAI); Mr S. S., Upadhya (Tata Institute of Fundamental Research); Mr PANYAM, Nagaraj (Tata Institute of Fundamental Research)

Presenters: ELANGOVAN, Yuvaraj; SARAF, Mandar (Tata Institute of Fundamental Research)

Session Classification: Poster - 1