ATLAS HL-LHC upgrades from a Swedish perspective

Jonas Steentoft on behalf of the Swedish ATLAS institutes

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Atlas Inner Tracker (ITk) HL-LHC upgrade

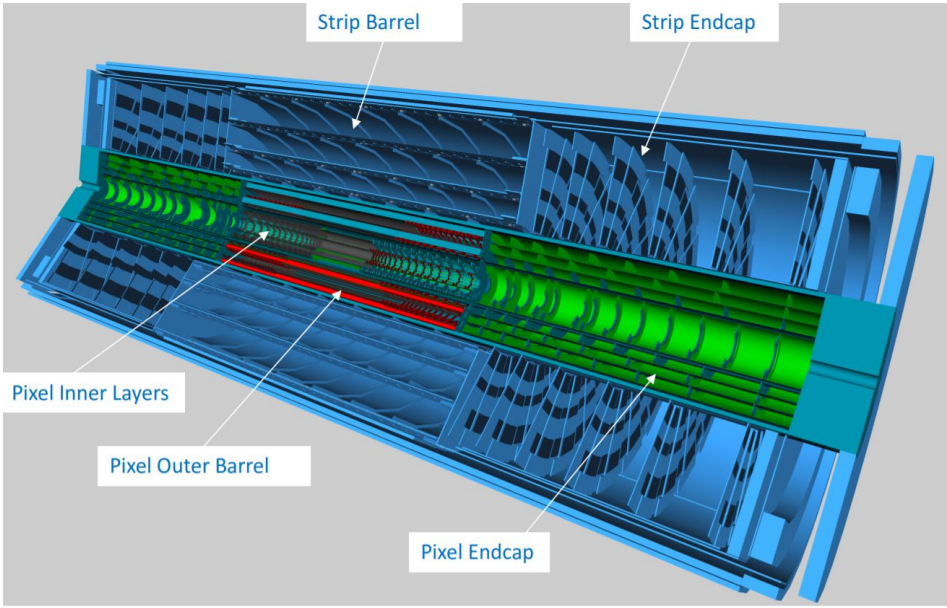
HL-LHC impact on tracking in ATLAS:

- Radiation damage
- Pile-up
  - Detector occupancy
  - Read-out bandwidth saturation
- TDAQ and trigger

All silicon tracker

Strips: 17.888 Modules, 59.89M channels
(current 6.3M channels)

Pixels: 10275 Modules ~800M channels
(current 92M channels)



Parameter	LHC Run-1	LHC Run-2 & 3	HL-LHC
Beam energy [TeV]	0.45–4	6.5–7	7
Peak inst. luminosity [$cm^{-2} s^{-1}$]	$0.8 \cdot 10^{34}$	$(0.7–2) \cdot 10^{34}$	$5 \cdot 10^{34}$ (levelled)
Bunch distance [ns]	50	25	25
Max. number of bunches	1380	2028~2748	2748
β^* [cm]	60	40	15
ε_n [μm]	2.3	2.5–3.5 (2.3 with BCMS)	2.5
Max. num. protons per bunch	$1.7 \cdot 10^{11}$	$1.2 \cdot 10^{11}$	$2.2 \cdot 10^{11}$
Average pileup ⟨μ⟩	21	21~50	140

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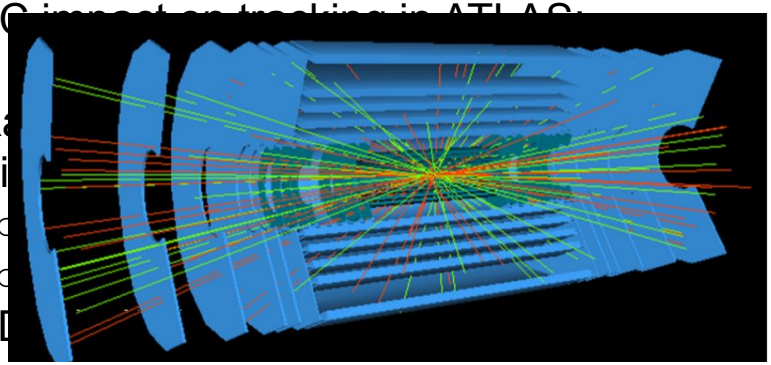
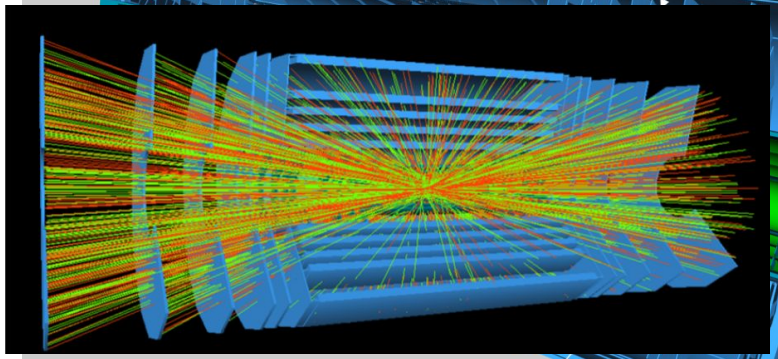
HL-LHC impact on tracking in ATLAS:

- Ra
- Pi
  -
  -
- TD





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Strip Module overview

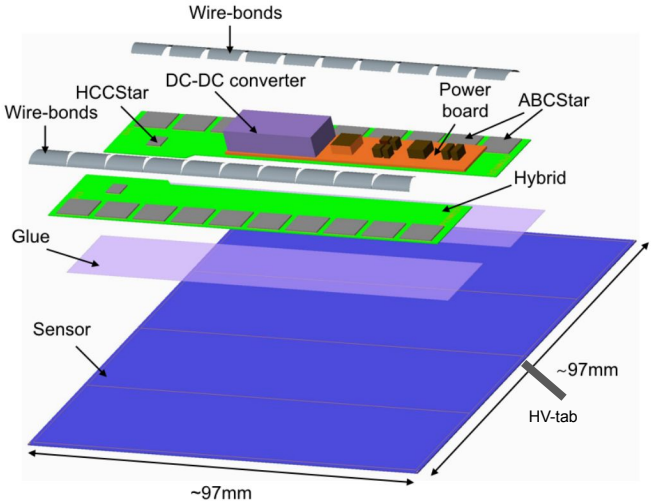
- N-on-p Si technology, 69-86 micron pitch
- Atlas Binary Chip(ABC) read-out asic
- High voltage supplied through al tab welded to sensor backside
  (significantly complicates assembly)

End of life performance requirements:

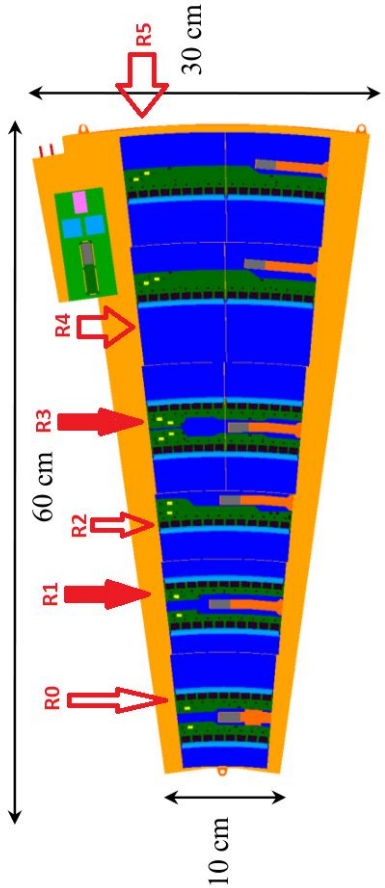
Efficiency > 99 %

Noise-occupancy < 10^-3

signal/noise ratio > 10



Exploded view of barrel type strip module

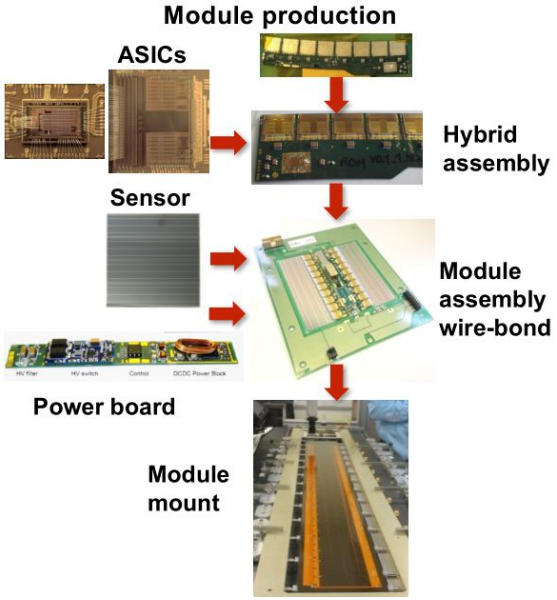


Endcap petal, mechanical sub-structure

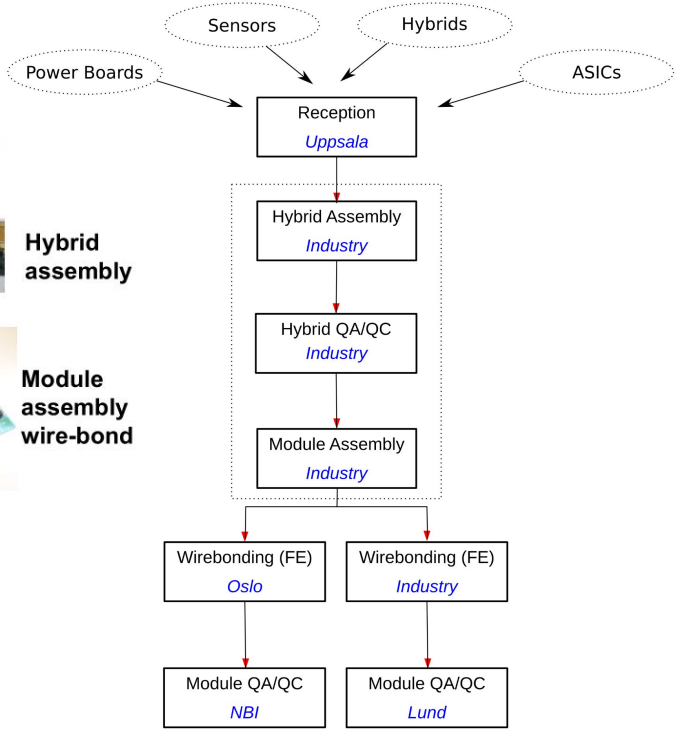
Swedish Contribution overview

- Scandinavian cluster collab on Endcap module production.
- Working with electronics industry, NOTE in Norrtälje.
- Committed to build 10% of Strip Endcap, ~700 modules split 50/50 across two types; R1 and R3.
- Final stages of prototyping, expecting Pre-production start end of Q1 2022

Covid delays:
lab lockdowns, international supply chains, Site qualification done through extensive documentation instead of review visit.



Production flow for barrel type modules, difference lies in sensor geometry.



Parts flow in Scandinavian Cluster

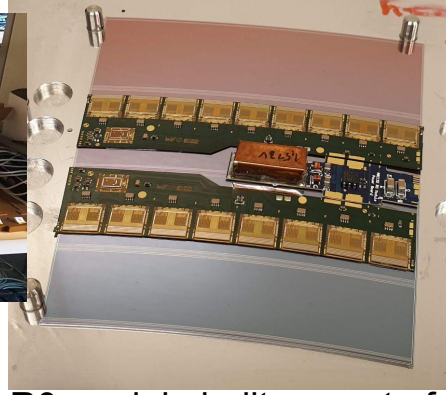
UNIVERSITY OF COPENHAGEN · UPPSALA UNIVERSITET · UiO: University of Oslo · LUND UNIVERSITY

Module assembly

Uppsala workshop committed to produce R1 assembly tools

(10-20 micron planarity across ~100 cm2 not easy to achieve!)

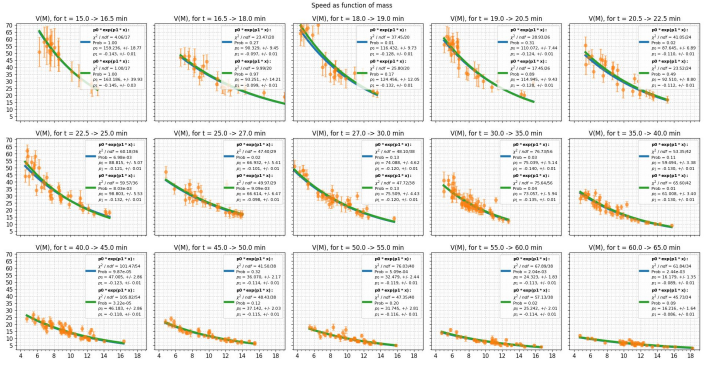
Production of all precision vacuum assembly tools for R1 type modules



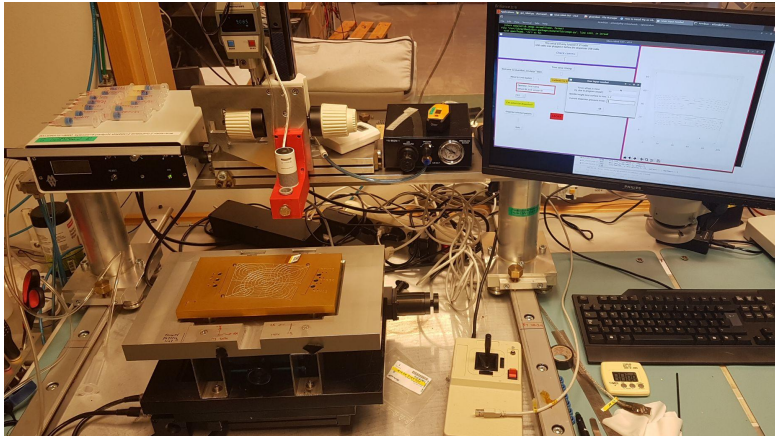
R0 module built as part of early prototyping. (front-en wirebonds missing.)

Hybrid-sensor 2-component epoxy.

Gluerobot developed so not reliant on specific operator for high quality assembly. Tricky to calibrate!



Gluerobot xy-table speed vs target mass, time-sliced in 0.5 - 3 min intervals



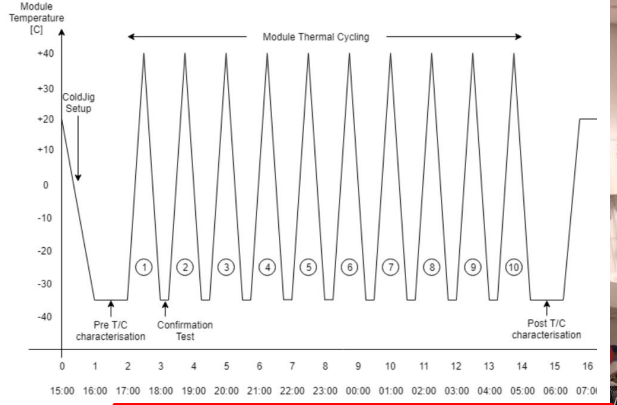
Gluerobot developed for hybrid-sensor assembly

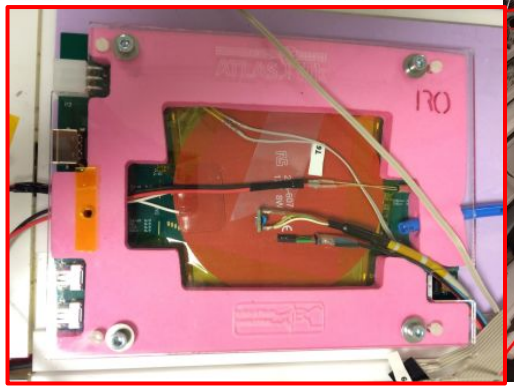
Thermal cycling QC

Modules subjected to 12 hr thermal cycling
(+45 <-> -35 C), and electrical testing (3pt gain, etc).

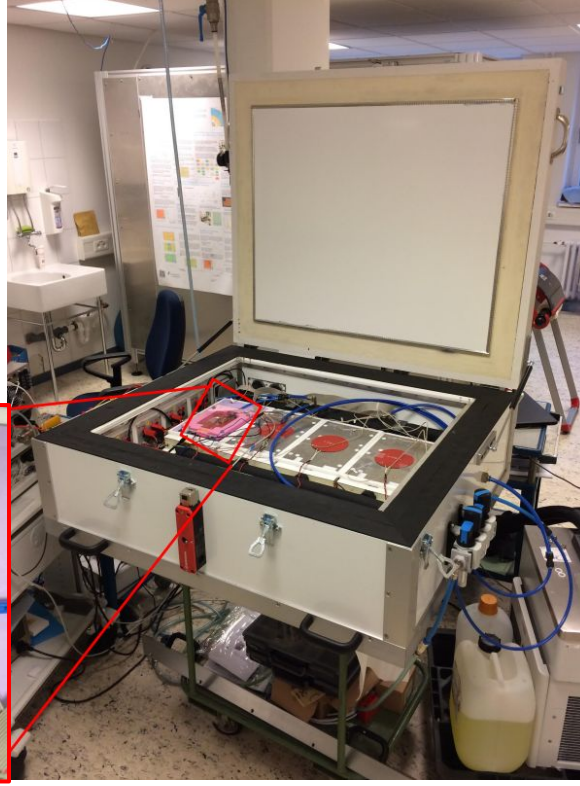
Stress testing to ensure expected lifetime performance.

Lund very involved in the developed of control software and hardware, collaborating directly DESY assembly site





Module mock-up using heating pad



Coldbox to be used at LU and NBI for QA/QC of all modules produced in Scandinavian Cluster

ATLAS HL-LHC trigger strategy

Initial scenario: all subsystems operate at 1 Mhz L0 trigger (10x current)
Limited capabilities for hadronic and exotic triggers (eg LLP) - bandwidth constraints!

Evolved scenario: split trigger L0/L1, regional read-out at 4 Mhz

The Hardware Track Trigger (**HTT**), utilises FPGA's and custom ASIC's.
A scalable event reconstruction co-processor to the Event Filter (**EF**) CPU farm. (Uppsala involved in project management and software dev)

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However:

ATLAS ITk pixel deemed it impossible to install 4 Mhz read-out services - They're too delayed.

Summer 2021, HTT cancelled in favour of purely commercial hardware approach.

ATLAS traded better trigger performance in favour of scheduling and risk management.

Not an easy decision!

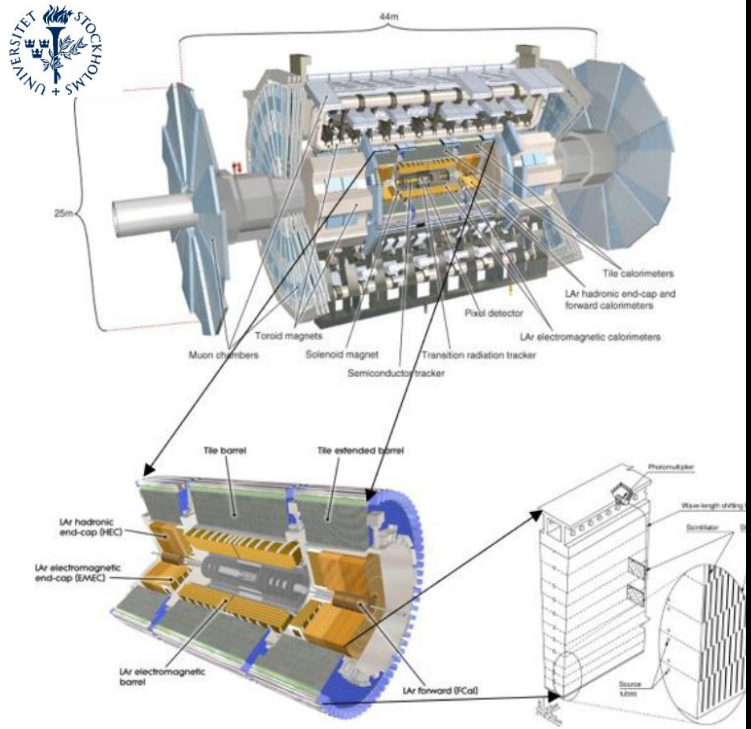
TileCal HL-LHC upgrades

HL-LHC TileCal electronics should handle:

- ~ 20x higher ambient radiation
- Capable of effectively resolving the higher pile-up conditions(~200 collisions per bunch crossing)

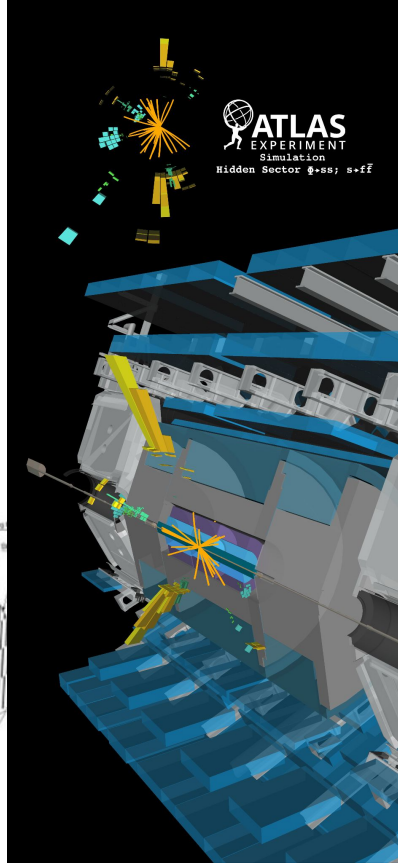
Approach:

- Full electronics re-design - both on and off detector
- Low latency 40 Mhz off-detector read-out rate (current ~100 kHz)
- Each individual read-out will be done at much higher sampling rate - increasing the fidelity
- Replacing heavily degraded PMTs (10%)



TileCal; after LAr cal is a segmented sampling calorimeter, steel plate absorbers and plastic scintillator tiles.

Read-out electronics located in pocket at the end of each tile wedge.

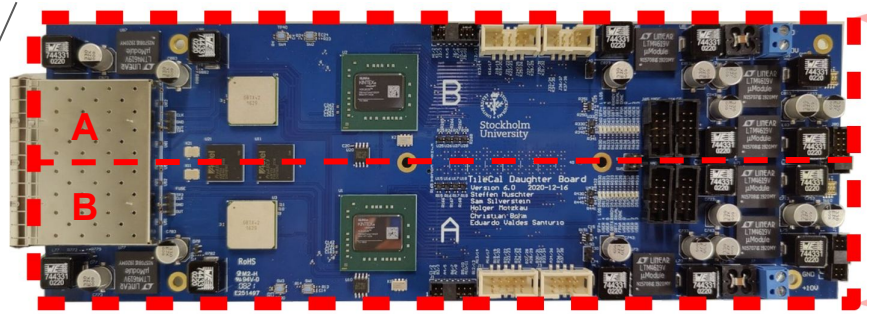


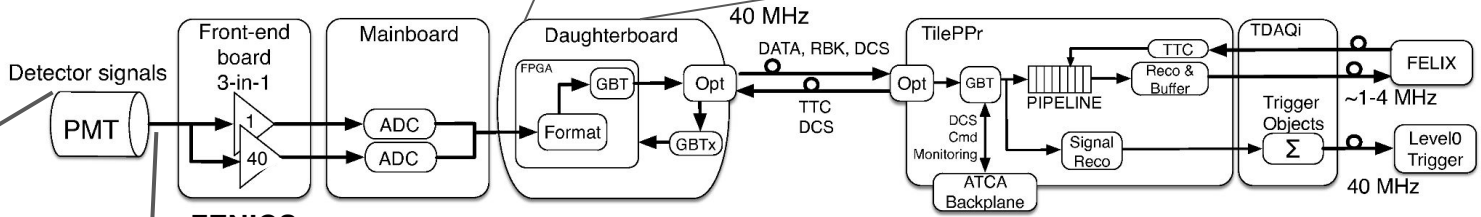
Example of hidden sector search, looking for displaced jets in Tilecal

The Daughterboard(DB) front-end read-out system

DB is the readout link and control interface for the upgrade TileCal front-end systems

- Sends detectors data to the off-detector electronics
- Receives and distributes LHC synchronized clocks, configurations and slow-control commands
- Design focus on radiation tolerance and redundancy.

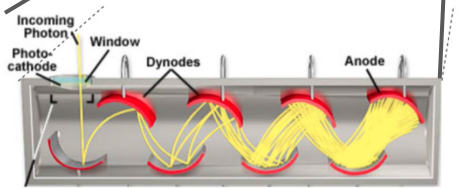




FENICS

~100 m fiber optic cables

L0 trigger, 40 Mhz



Evolution and radiation tests

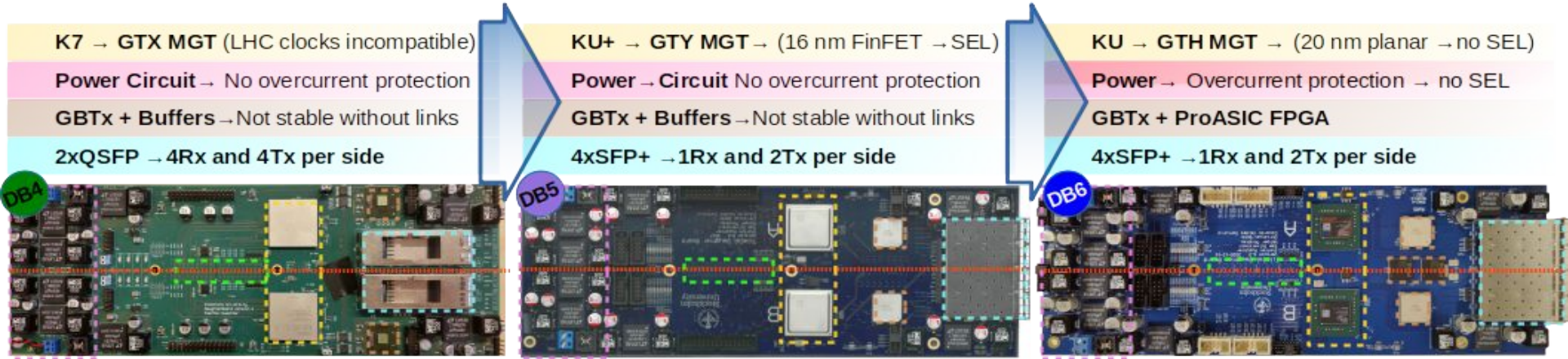
Tremendous efforts spent on design validation, especially wrt. radiation damage.

- Radiation test campaign showed DB5 FPGA prone to Single Event Latch-ups (SEL) (over-current)
  - Triggered ~1.5 years re-design of DB -> DB6

SEE (Feb 2020): No SEL detected up to 1.11E+12 p/cm2
- pre-liminary SEU soft error rate manageable and to be mitigated through logic triplication.

TID (June 2021): 2x DB6 successfully test up to expected end-of-life dose + safety factor

NIEL (Oct+ 2021): 1x DB6 used, waiting for radiation cooldown, to be tested in ~ December.
- Physics data was taken using the DB6 at SPS testbeam!



Project overview

- **Daughterboard production plans:**
  - For full HL-LHC need to produce ~1000
  - On track installation of the tests and and maintenance facility in Stockholm ATLAS lab for QC

- **Milestones achieved 2020-2021:**
  - Migration to a new FPGA, mitigating SEL problem
  - Almost complete radiation test campaign for the DBv6 (dedicated SEU before FDR in July 2022)
  - Successful integration with adjacent Upgrade Hardware components:

- **Main risks taken into consideration:**
  - Component shortages and obsolescence
  - Price fluctuations for electronics components (Xilinx increased FPGA prices 20% → still affordable with the current budget→ less DB prototypes for tests)
  - Strategic purchase of batches to minimize radiation tests (KU FPGA purchase in one batch)

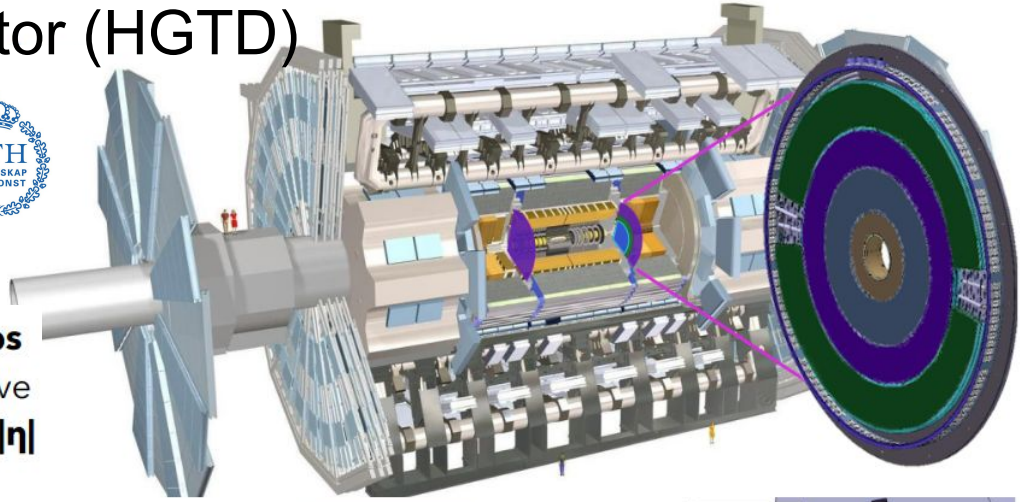
- Current version close to final - only minor changes foreseen.

- New ATLAS radiation policy from 2020 imposes new radiation tests of production batches, initially not foreseen: additional cost and time..

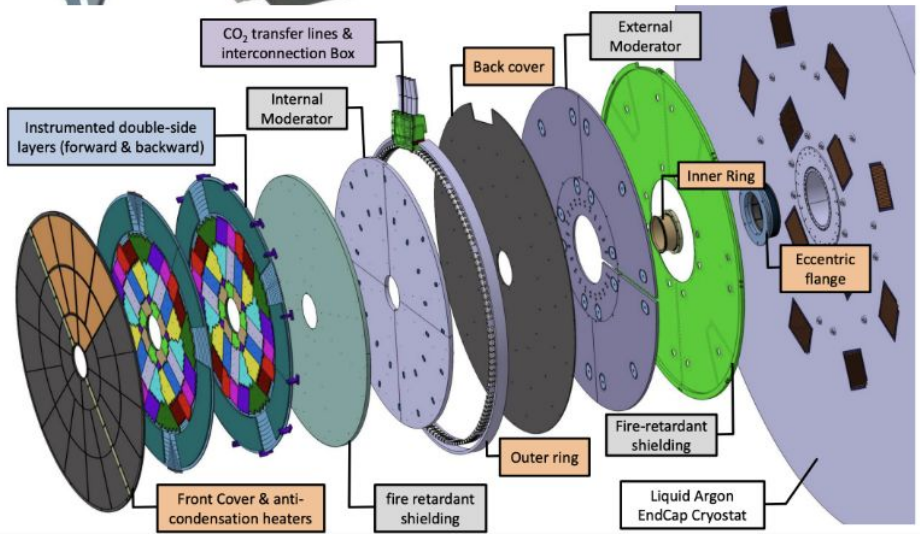
Project is still on track; delivery ~1 year before they are needed!

High Granularity Timing Detector (HGTD)

New detector to be inserted in the ATLAS forward region, between the ITk and fwd calorimeters



High precision timing (per-track resolution of **35-50ps** up to 4000 fb-1) to mitigate pileup effects and improve the ATLAS performance in the forward region (**2.4 ≤ |η| < 4.0**)



Strong design limitations based on the available physical space in the detector volume

➔ total wheel thickness of 12.5 cm

3-ring layout, divided based on expected dose

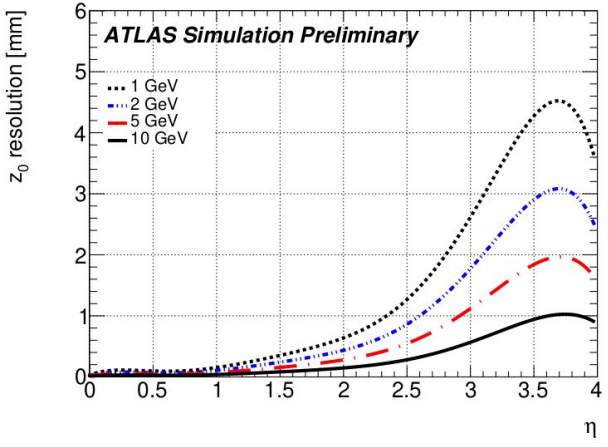
➔ Max expected fluence 2.5E15 neq/cm2

Gain of precision timing

HL-LHC pile-up conditions means primary vertices closer together in Z - timing helps separate events!

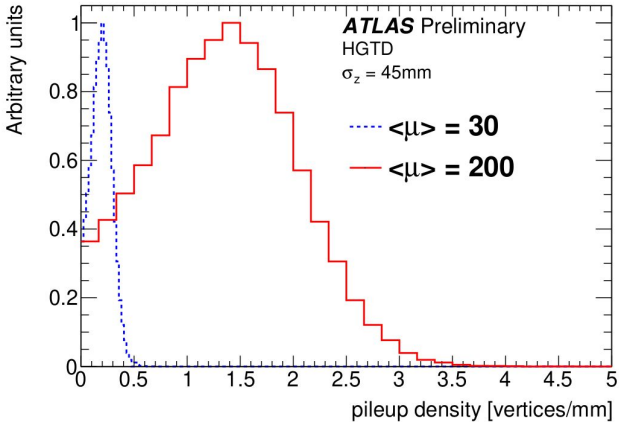
Track-vertex association criteria: (From HGTD TDR)

$$\frac{|z_0 - z_{\text{vertex}}|}{\sigma_{z_0}} < 2, \qquad \frac{|t - t_0|}{\sigma_t} < 2,$$



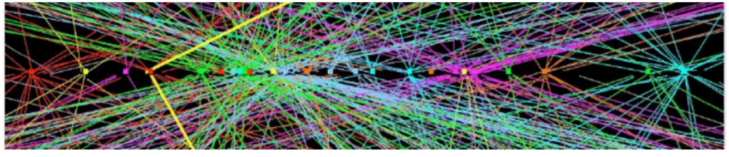
Z resolution estimate for prompt vertices - displaced vertices (B tagging) worse

If achievable Z resolution is worse than ⟨ρ(z)⟩:
We're in trouble!



⟨ρ(z)⟩ avg pile-up density along beam axis, Run2 and nominal HL-LHC conditions

LHC (25 vertices)

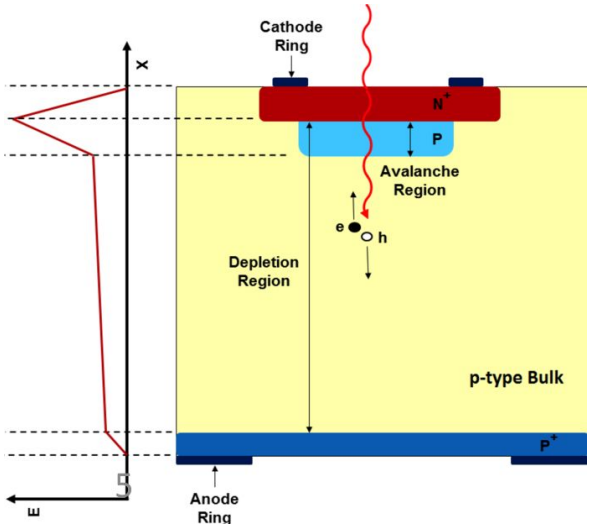


HL-LHC (200 vertices)

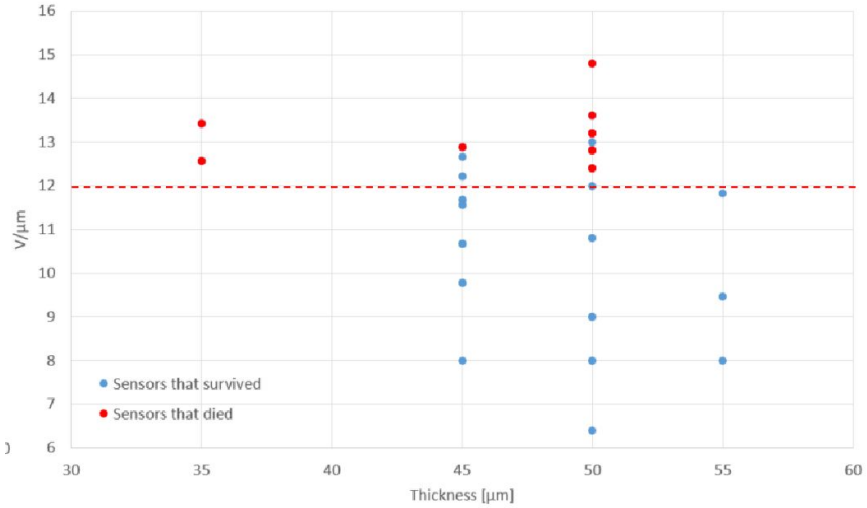
Low Gain Avalanche diode sensors (LGAD)

Si sensor technology with integrated charge amplification

- Sensor internal **gain>20** before irrad (**>8 at EoL)**
- Very thin wafer (50 micron) to ensure sufficiently fast rise time
- However, HV gradients more problematic with thin wafers
- Issues with Single-Event-Burn-out (SEB) seen in testbeams



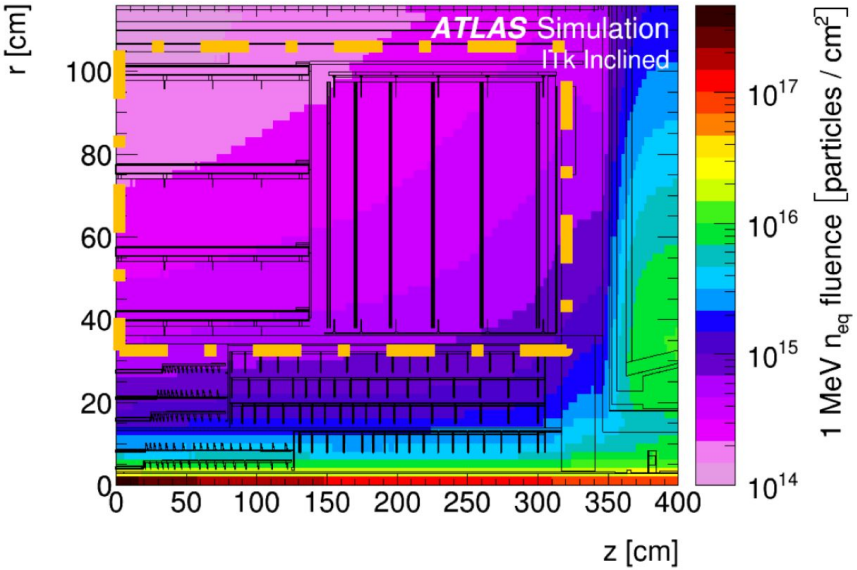
Doping profile of the LGAD. Compared to conventional pn junctions, the added charge gradient causes a high E-field and electron generated impact ionisation (avalanche).
(Only electrons are amplified to avoid total current breakdown.)

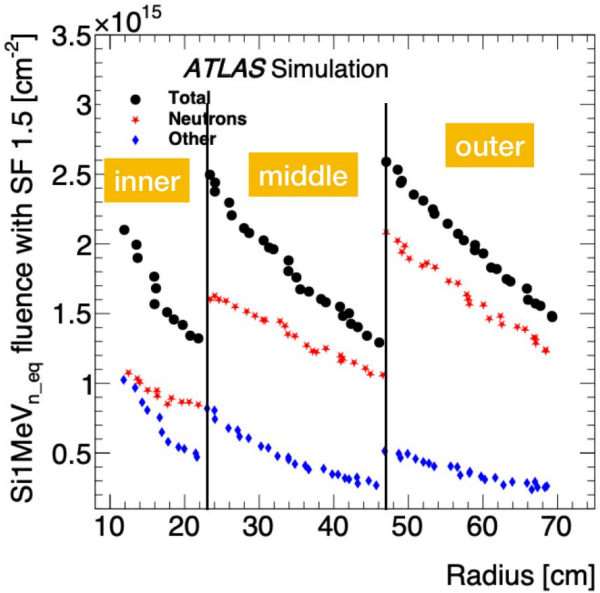


Recent testbeam results showed safe limit of HV biasing at ~ 12 V/micron

Radiation tolerance

Forward (low r) region is where we expect to have the highest radiation fluence.





Mitigation strategy is to divide HGTD into 3 layers, and plan for replacements:

- Inner ring [12-23 cm] -> replaced every 1000/fb
- Middle ring [23-47 cm] -> replaced after 2000/fb
- Outer ring [47-64 cm] -> never replaced

KTH involvement in HGTD

Involvement in several HGTD working groups (also in coordinating roles):

- **Electronics**
  Peripheral electronics, grounding and shielding
- **Luminosity and DAQ**
  HGTD is also suitable for performing luminosity measurements at bunch crossing rate.

  DAQ demonstrator being developed at CERN, connecting front-end emulators to the FELIX readout system

- **Software and Performance**
  Implementation/migration of HGTD offline SW into Athena (ATLAS primary offline analysis and simulation framework)

Summary

ITk strip module production:

Site qualification on-going, prototyping efforts in full effect, pre-production to begin Q1 2022, schedule is extremely tight.

Hardware Track Trigger:

Cancelled as a schedule & risk mitigation maneuver, due to ITk pixels inability to implement 4 Mhz read-out.

Tilecal front-end Daugtherboard:

Progress is good, previous radiation test campaign triggered 1.5 year re-design of the board, but new results look very promising and project is still on schedule!

High Granularity Timing Detector:

New precision timing detector will be inserted to improve primary-vertex-to-track association in HL-LHC environment, R&D efforts ongoing but very promising, project schedule is okay.