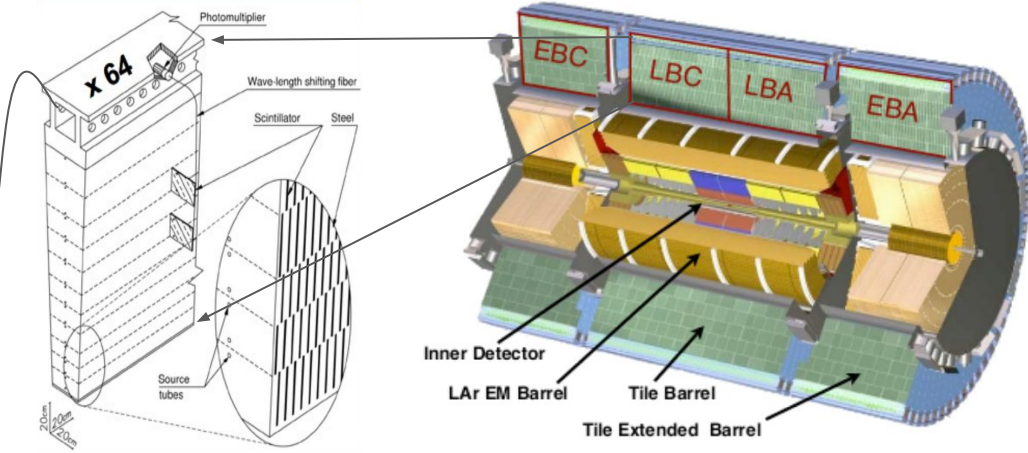


# HL-LHC Upgrades to the ATLAS Hadronic Tile Calorimeter Readout Electronics

[Katherine Dunne](#)

for the Stockholm University TileCal Group  
Swedish Particle Physics Meeting  
November 23–25, 2020

# The ATLAS Hadronic Tile Calorimeter

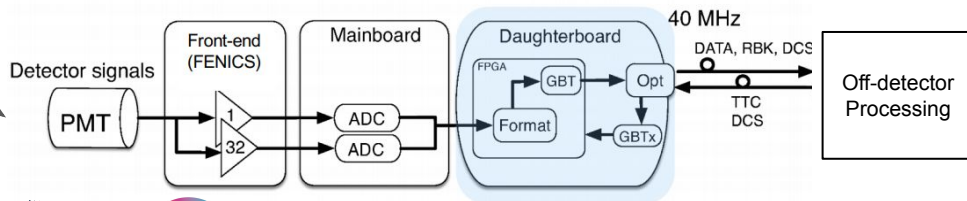


# The High-Luminosity LHC Era

- TileCal essential for measurement of jet/missing energy, jet substructure, electron isolation, and triggering
- Increase in luminosity makes HL-LHC challenging in terms of radiation hardness and triggering
- Phase-II trigger system redesigned with fully digital trigger to improve selectivity
  - access to digital info from each calorimeter cell with low noise and accurate energy calibration
- Electronic components must be replaced to survive higher radiation environment

## Daughterboard: Tile readout-out link

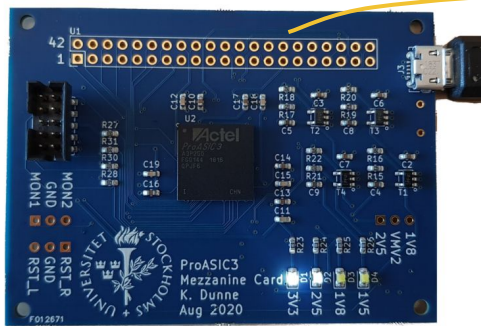
- Control & readout interface for the upgraded TileCal front end systems



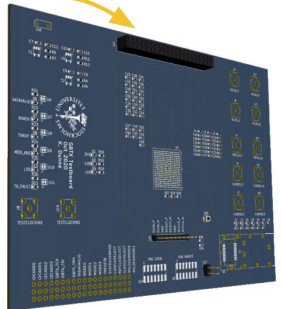
# Daughterboard Upgrades

- Migration to Kintex Ultrascale (KU) FPGAs
  - Single Event Latch-Up (SEL) observed in Ultrascale+
- New remote JTAG interface design using FPGAs (ProASIC3)
  - Improved reliability, buffering, voltage translation
- DC-DC regulation w/ failsafe power-up sequencing, improved monitoring, and over-current protection
- Optimized routing of ADC data & clocks to FPGA banks for better timing performance

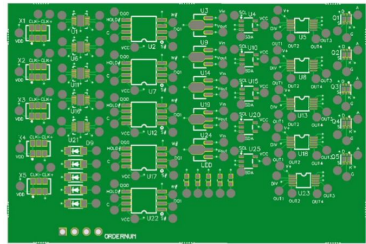
# Upgrade Test Boards



ProASIC3 Mezzanine Board

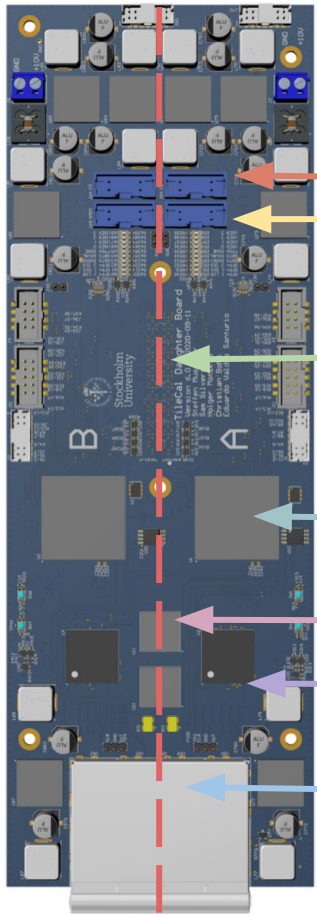


GBTx Test Board



Aux Component Irradiation Board

# Daughterboard v6

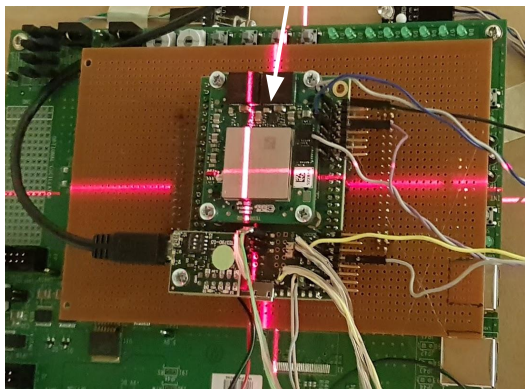
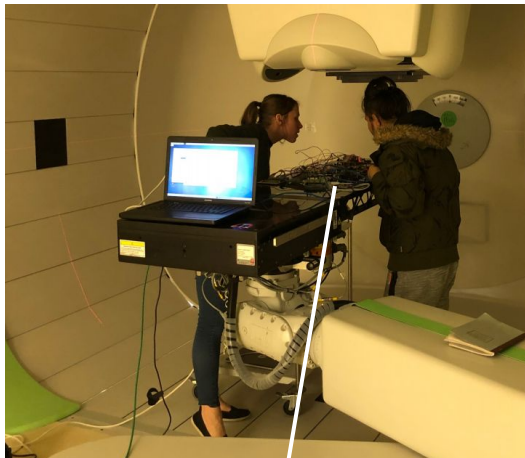


- 2 independent sides
- Power Regulation
- 2x Cs interfaces
- 2x xADC interfaces
- 400 pin FMC interface with MB
- 2x Kintex Ultrascale (KU)
- 2x ProASIC3
- 2x GBTx
- Fiber transceivers  
4x9.6 Gbps uplink  
2x4.8 Gbps downlink
- Power Regulation



## SEU / SEL Tests

- FPGAs tested w/ 226 MeV proton beam at IFJ Krakow
- Fluence:  $1.11\text{E}+12 \text{ p/cm}^2$
- KU SEU rate:  $166 \text{ SEU}/1.4\text{E}+9 \text{ p/cm}^2$ 
  - Negligible disruption to HL data taking
  - Not all FPGA logic used, Triple Mode Redundancy, Xilinx Soft Error Manager
- No latch-up observed (SEL)



## Upcoming Irradiations

- NIEL at Ljubljana TRIG A Mark II
  - $9\text{E}+12 \text{ n/cm}^2$  (1 MeV equivalent)
- TID at Stockholm U. facility
  - 15 kRad + annealing

## Daughterboard Production

- 1085 DBs will be produced
- 896 installed in ATLAS
- Small batch to be produced this year
- Final Design Review completed 2021
- Stockholm U. ATLAS Production Lab:
  - 2 test benches, for production testing and debugging in parallel
  - Burn-in oven capacity up to 40 DBs, with temperatures up to 85C