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Centralized Deployment of EPICS Systems for Zynq-based Devices

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Our society has been benefiting from Zynq/ZynqMP SoCs that integrate ARM processors and programmable logic fabric by utilizing their flexibility from processing system (PS) and high performance from programmable logic (PL). However, the typical approach for utilizing such systems has observed several problems during deployment and maintenance. Firstly, implementation of a typical EPICS software system on such a device involves compilation of EPICS base, supporting modules, and EPICS driver, either through cross-compilation or compilation locally on the SoCs. This process becomes very time consuming when lots of devices need to be built or updated. Secondly, the reliability of the storage on these devices is suspicious. Many of these devices have file systems hosted on non-volatile memory devices, such as SD cards, which are more fragile than hard disk drives or solid state drives. Since EPICS IOCs can create significant amount of data to be written during routine operation, such as writing autosaved files and logs, when the devices are not properly rebooted or powered off, file systems can be corrupted which results in devices malfunctioning. We implemented a centralized framework that reduces the effort for deploying EPICS and supporting software system on such Zynq-based devices, especially when multiple devices are to be deployed. We built Linux images using PetaLinux SDK with the configuration that minimizes the changes needed for each device during deployment. We exported root file systems from a central NFS server, which the devices mount as their own file systems, so that all data are written to the servers which are much more reliable than the SD cards used on the devices. We created root file systems for different devices that include EPICS packages tailored specifically for the corresponding functionality. We automated the procedure that differentiate instances (e.g., at different beamlines), load corresponding parameters and bring up the system. This paper describes the design and configuration of the design.

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