Discussion Session

Timing Workshop EPICS Meeting Spring 2019

Jukka Pietarinen

Micro-Research Finland Oy

Diamond-II Upgrade

- Storage ring harmonic number change from 936 (2*2*2*3*3*13) to 934 (2*467).

- The event clock rate at DLS is RF/4, now one revolution of the SR is 234 event clock cycles

- For Diamond-II 934/4 = 233.5

- Proposal:

    - Distribute "two revolutions" clock 467 event clock cycles

    - Use CML/GTX pattern outputs to generate required SR clock

    - Pattern of 467 event clock cycles with a resolution of 20 (EVR-230) or 40 (EVR-300) bits per event clock

For Discussion

- What are the advantages/disadvantages of timestamping data on the source hardware (DAQ boards) vs. timestamping data with external sources (timing cards).