中国科学院高能物理研究所
INSTITUTE OF HIGH ENERGY PHYSICS, CAS

A Bunch-by-Bunch Beam Position Monitor

Fang Liu

Institute of High Energy Physics,
Chinese Academy of Sciences

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Introduction

Normal BPM

——Turn-by-Turn Measurement
——Fast Acquisition Measurement
——Slow Acquisition Measurement

→ doing **Bunch-by-Bunch** measurement

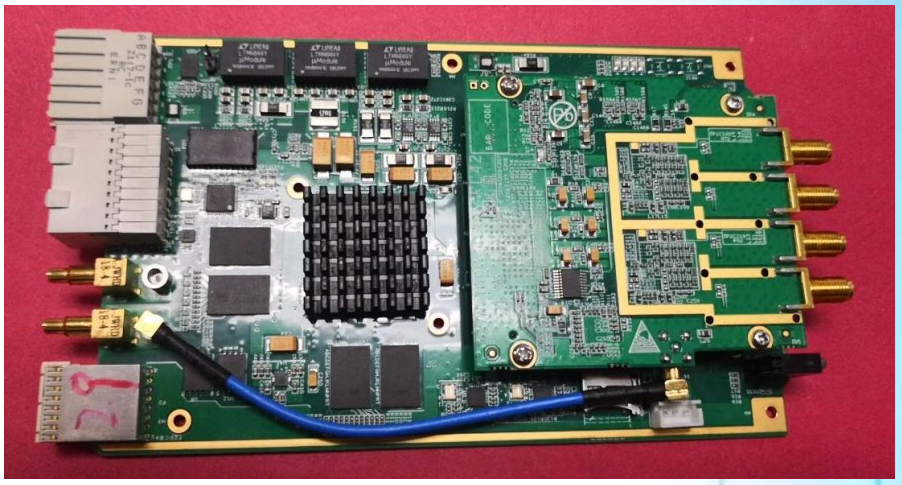
ADC Frequency &Accuracy Improved	Digital Signal Processing Research& Methodology Deeping &Sufficient	High Precision Bunch-by-Bunch Beam Position Monitor Available

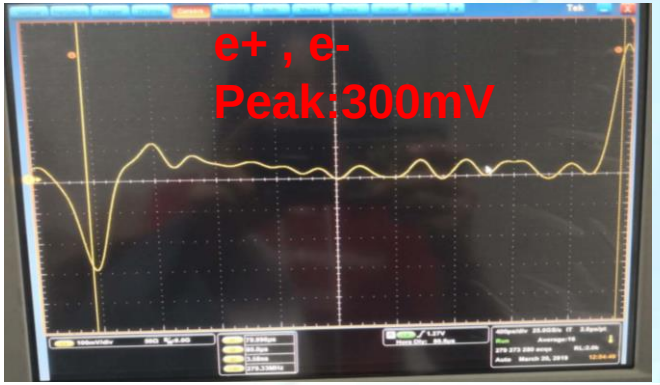
Goal：Resolution of Bunch-by-Bunch : 5um

- Research of Inter-Bunch Beam Dynamics
- Hardware platform of Bunch-by-Bunch Feedback system，Bunch-by-Bunch Beam Current Monitor；Diagnosing Beam Lost and Catching Tune of Beam

A Bunch-by-Bunch BPM

- **Electronic System**
  - **ZYNQ7035**
    - ✓ dual-core ARM Cortex-A9&Kintex®-7 ZYNQ7035
  - **4 Channels 500MSPS 14bit ADC**
    - ✓ AD9684, 2 channels
  - **1GB DDR3**
  - **100/1000Mbps ETHERNET**
  - **PCIE GEN2 X4**
  - **Input Analog Band Width: 10MHz-2GHz**





- **A Four Button Pickup**

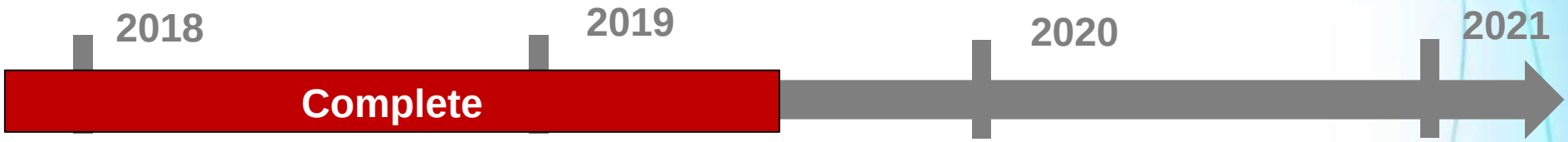
  The signals from the pickups of BEPCII are enough for directly data sampling of ADC

- **Delay Module**

  Adjust to the time to guarantee ADC can get the peak of the Button Signal

Development state

R&D Plan: A ZYNQ Based, Four channels 500Msps ADCs, Bunch-by-Bunch System



Already Down

Hardware : Circuit Design, Soldering and Debugging.

Firmware : ADC control, Clk control, DDR ,Ethernet Bunch-by-Bunch Algorithm

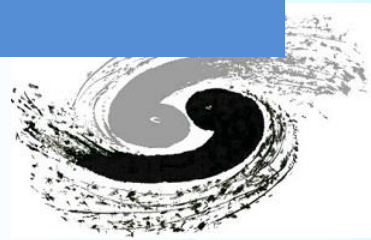
Soft in ZYNQ ARM : Initialization of Ethernet, ADC and Clk. Data Acquisition Control

Need to Do

Develop : Embedded Linux and EPICS on ZYNQ ARM

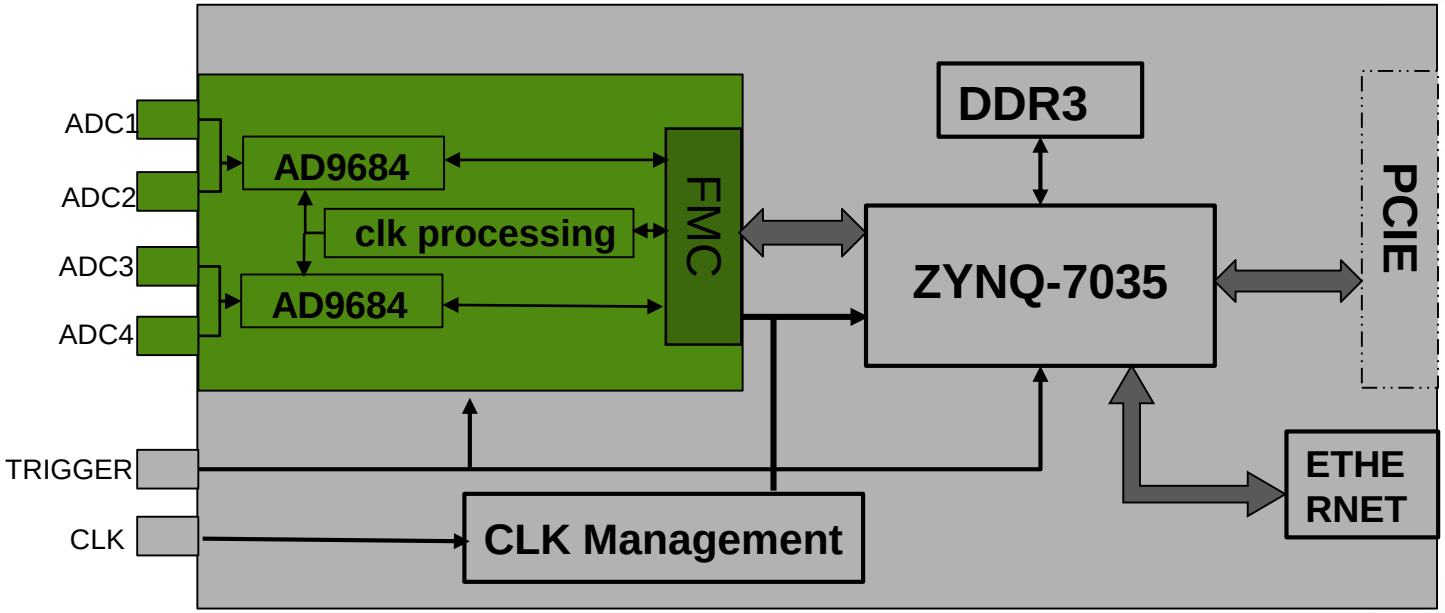
Improvement: Upgrade Hardware and Firmware

Furthermore: Embedded Timing ?....



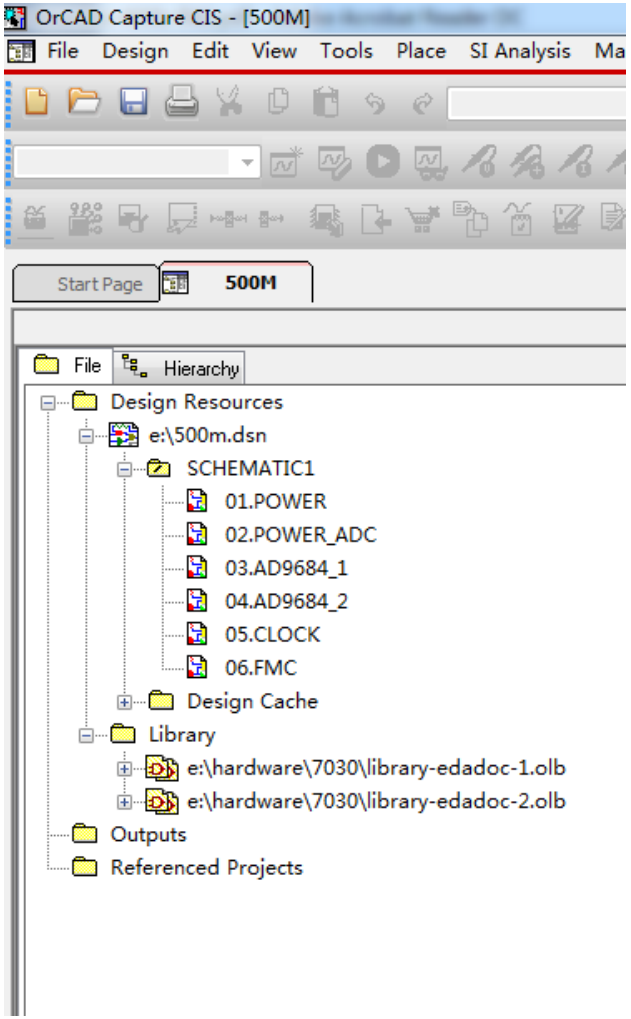
Hardware

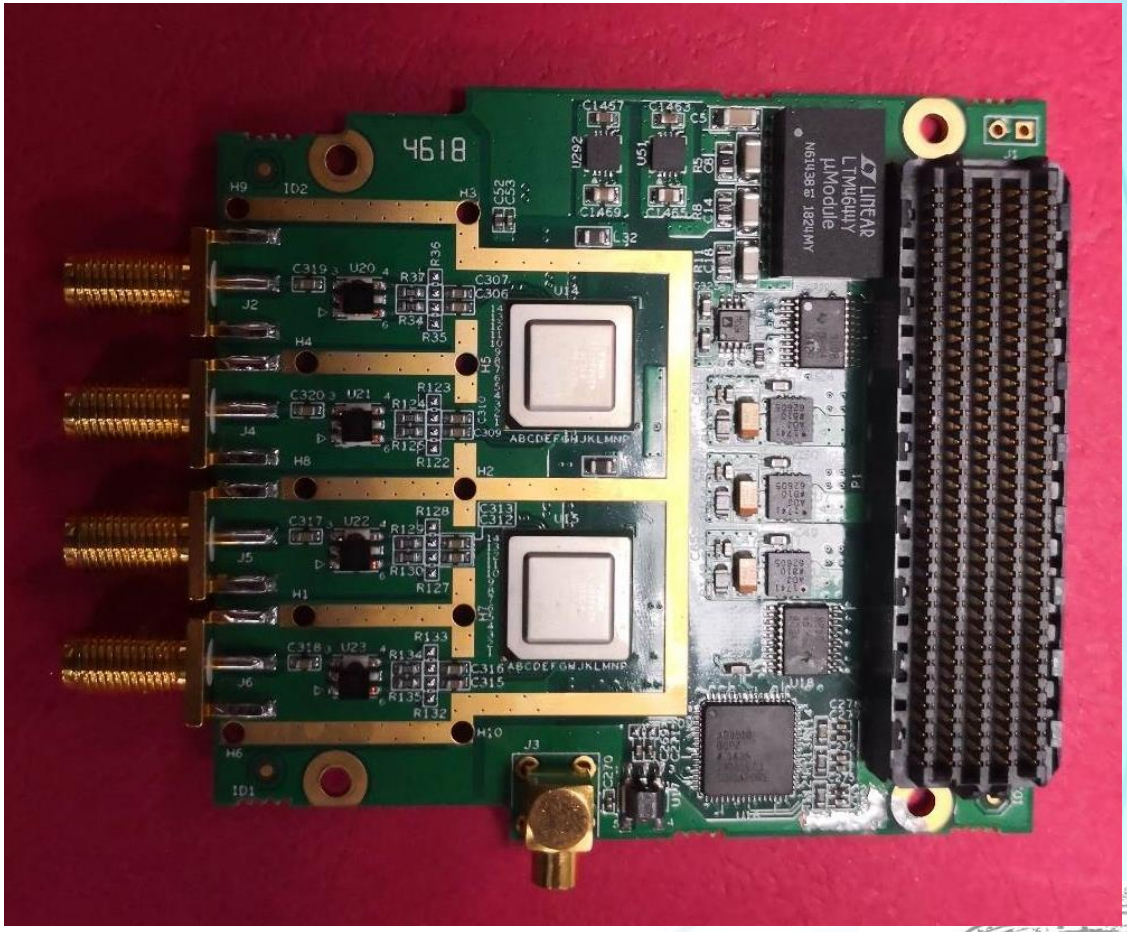
Architecture



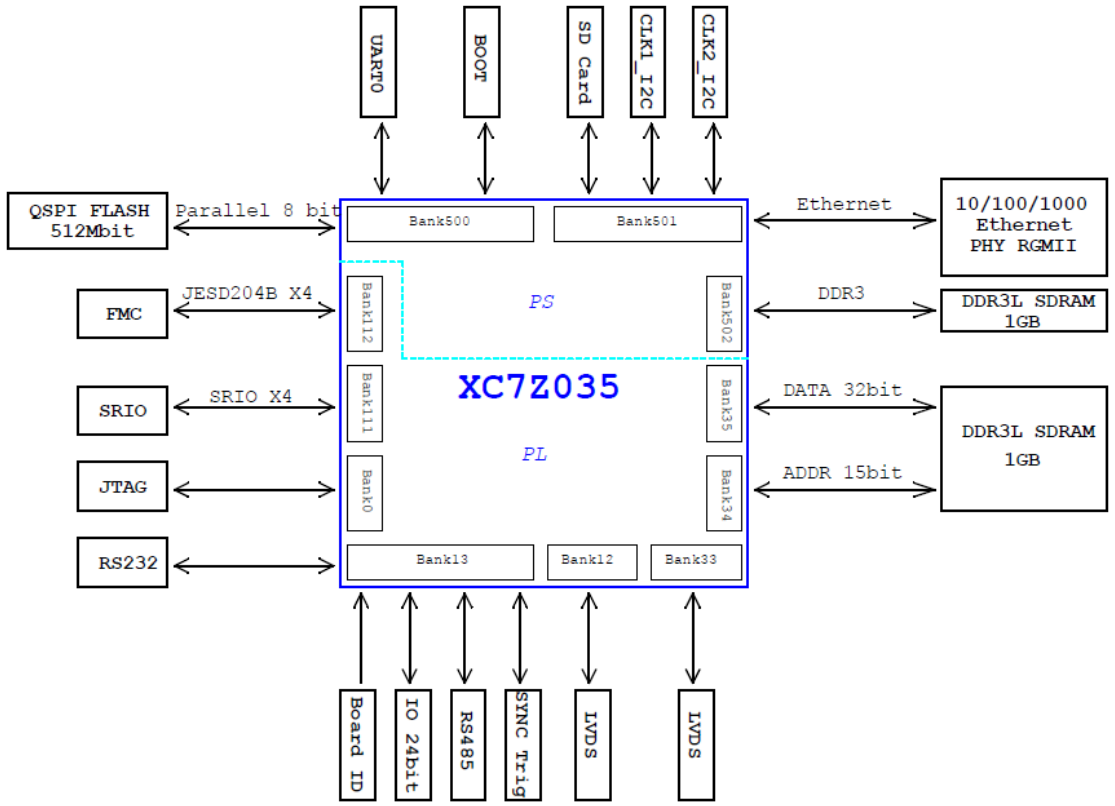
- Base board and FMC Carrier
- ZYNQ7035 FPGA and 4 channels 500MSPS 14bit ADC
- 2 DDR3: one for Data Storage, one for ARM
- 10/100/1000Mbps Ethernet
- PCIE GEN2 X4: backplane

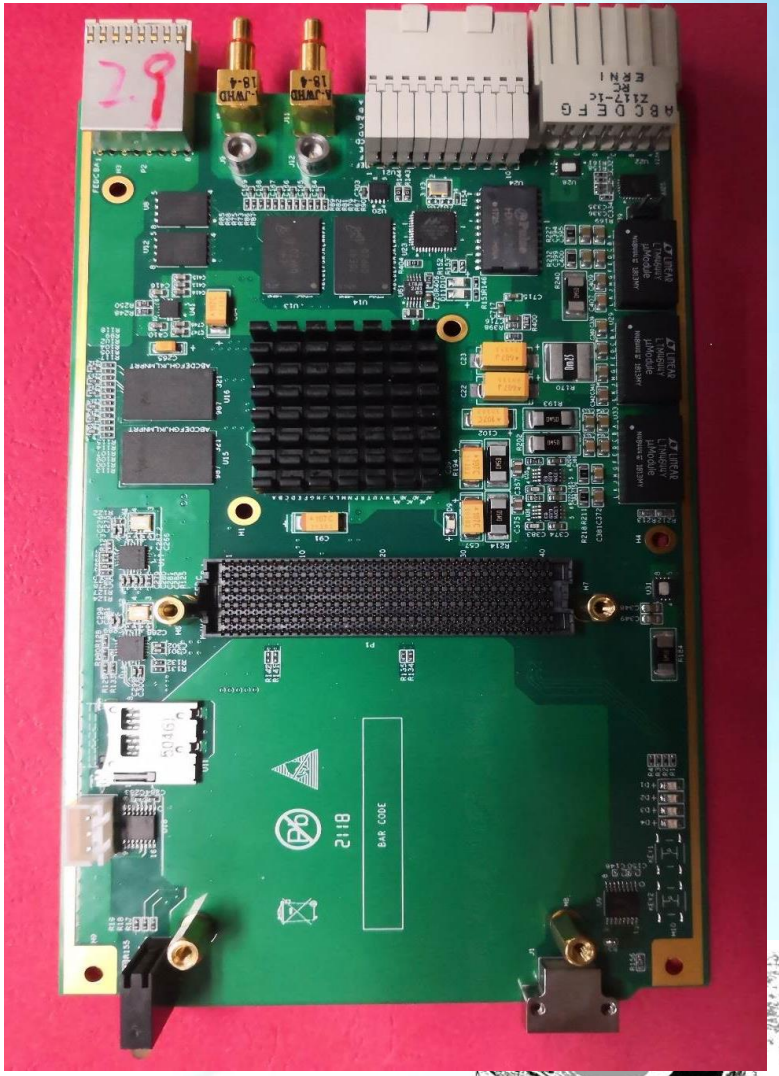
Four Channel 500MSPS ADC FMC Card



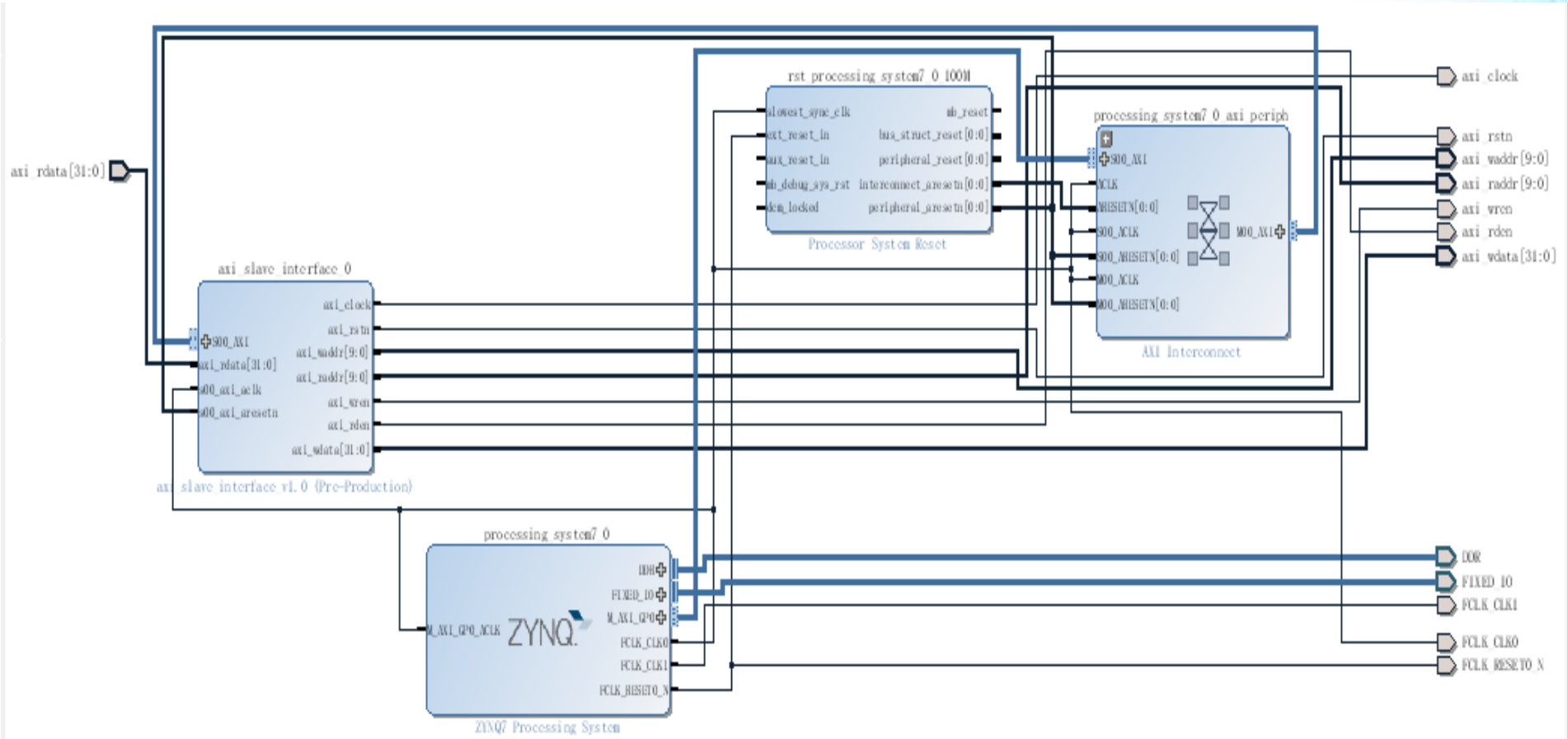


Base Board: ZYNQ7035

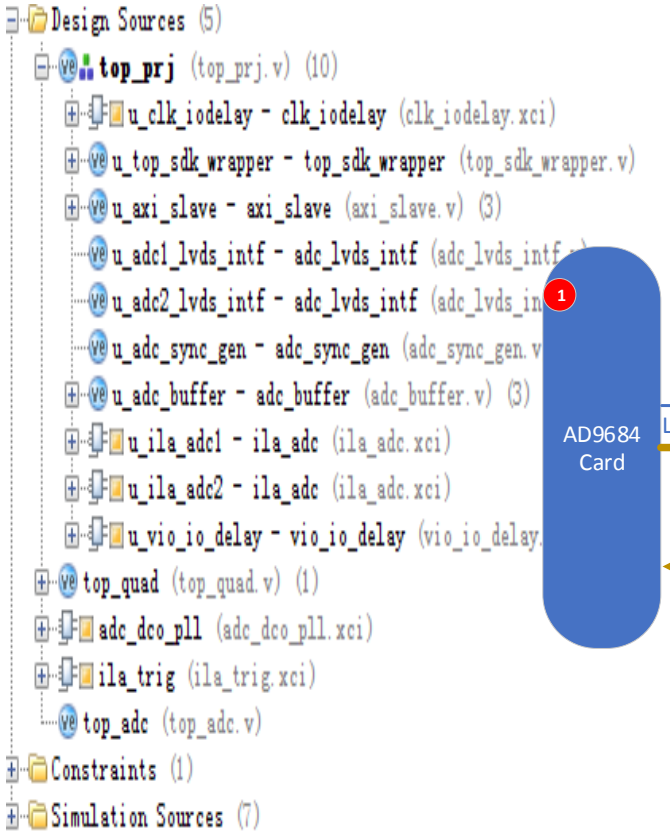


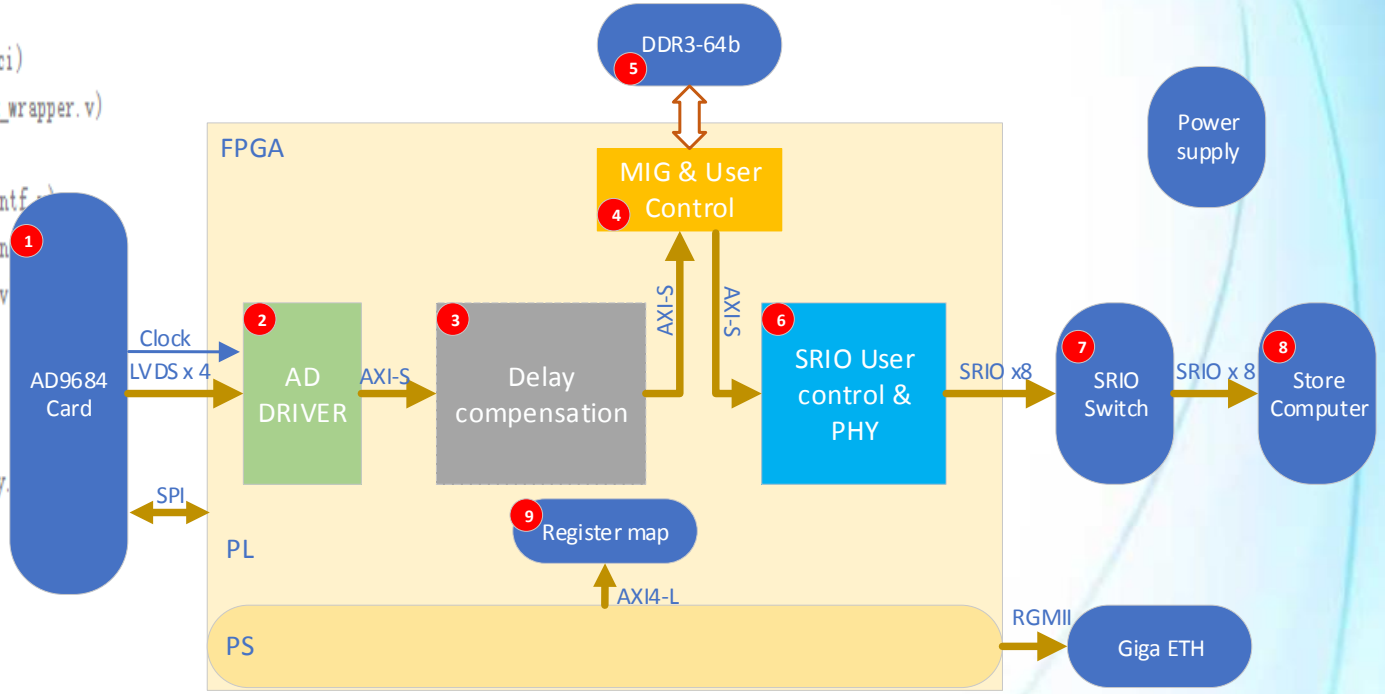


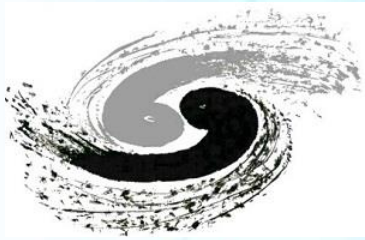
ARM Core Construction



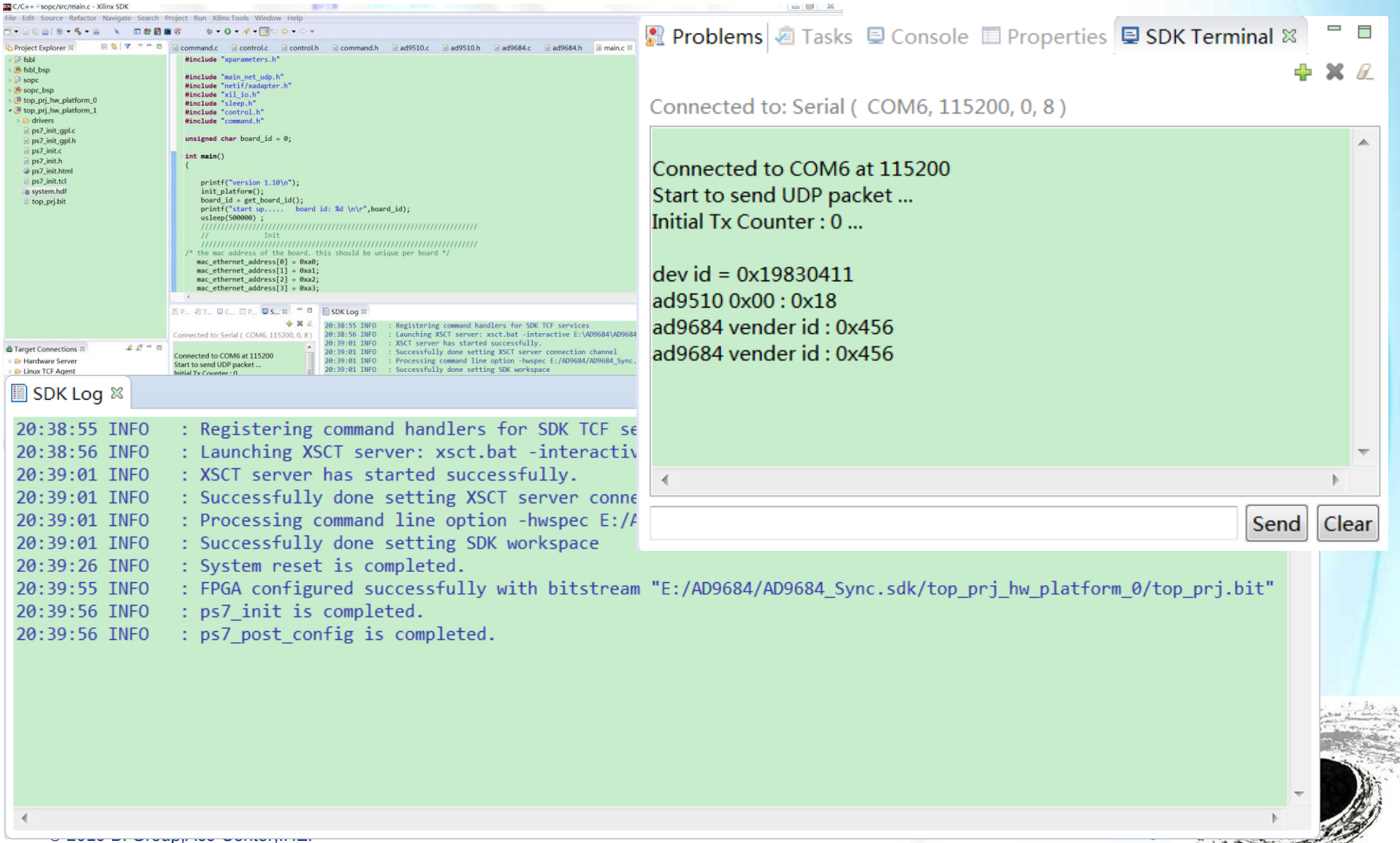
FPGA Logical in ZYNQ PL



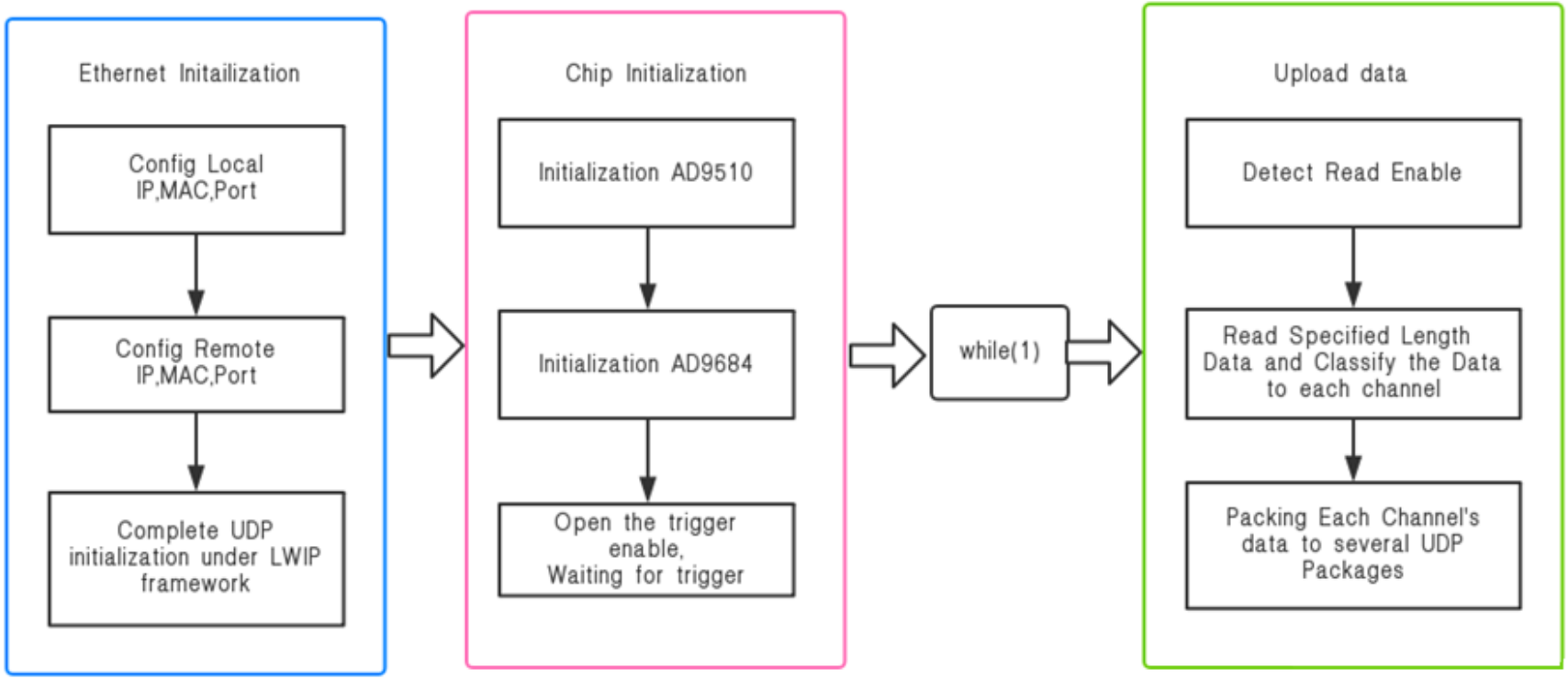




Using PS code configure FPGA



ARM Code in ZYNQ PS

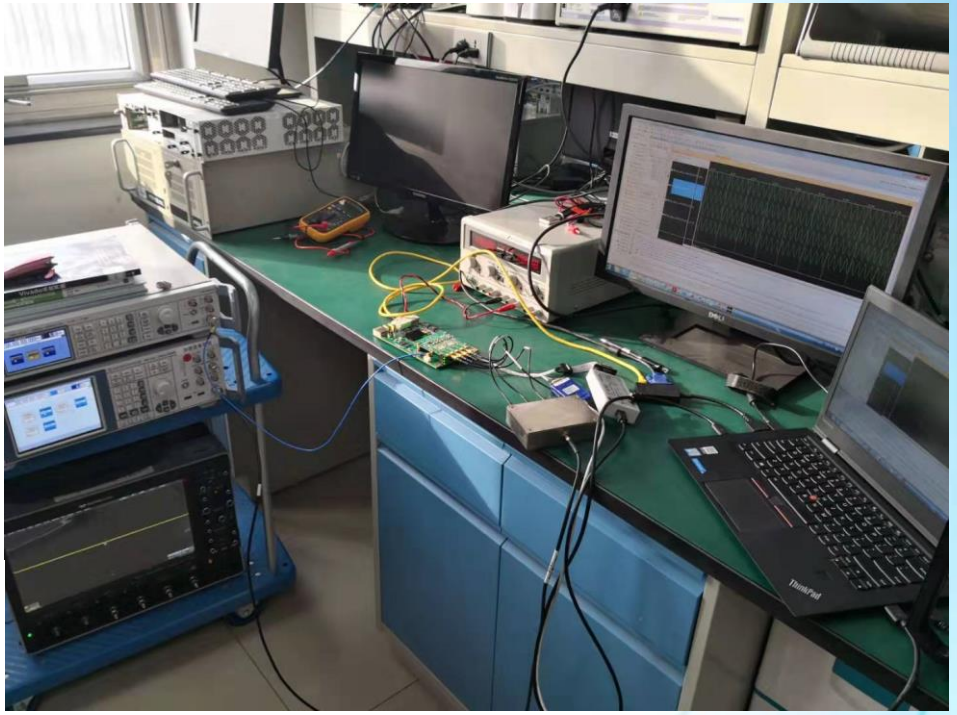


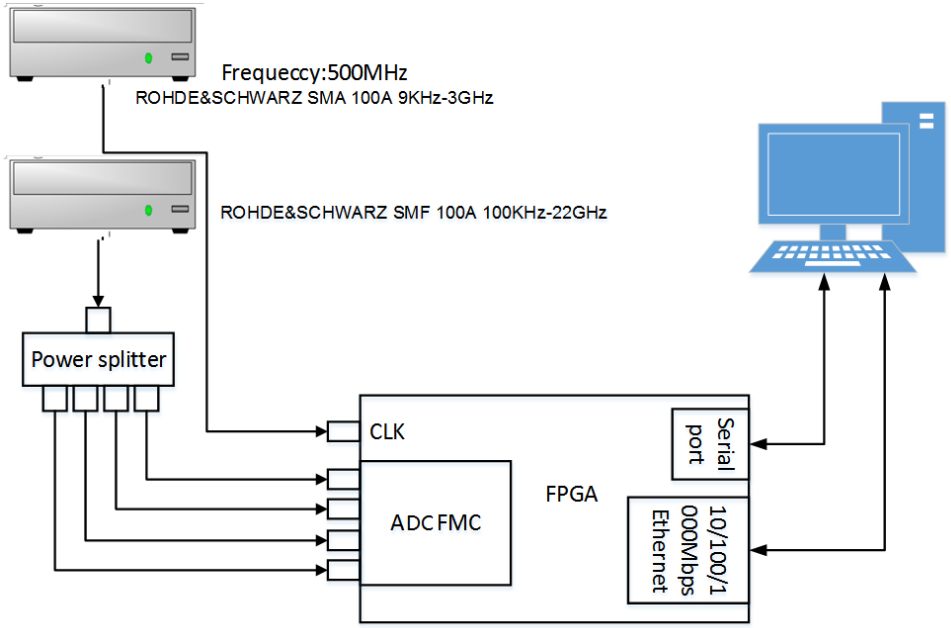
Test in Lab

Test Environment

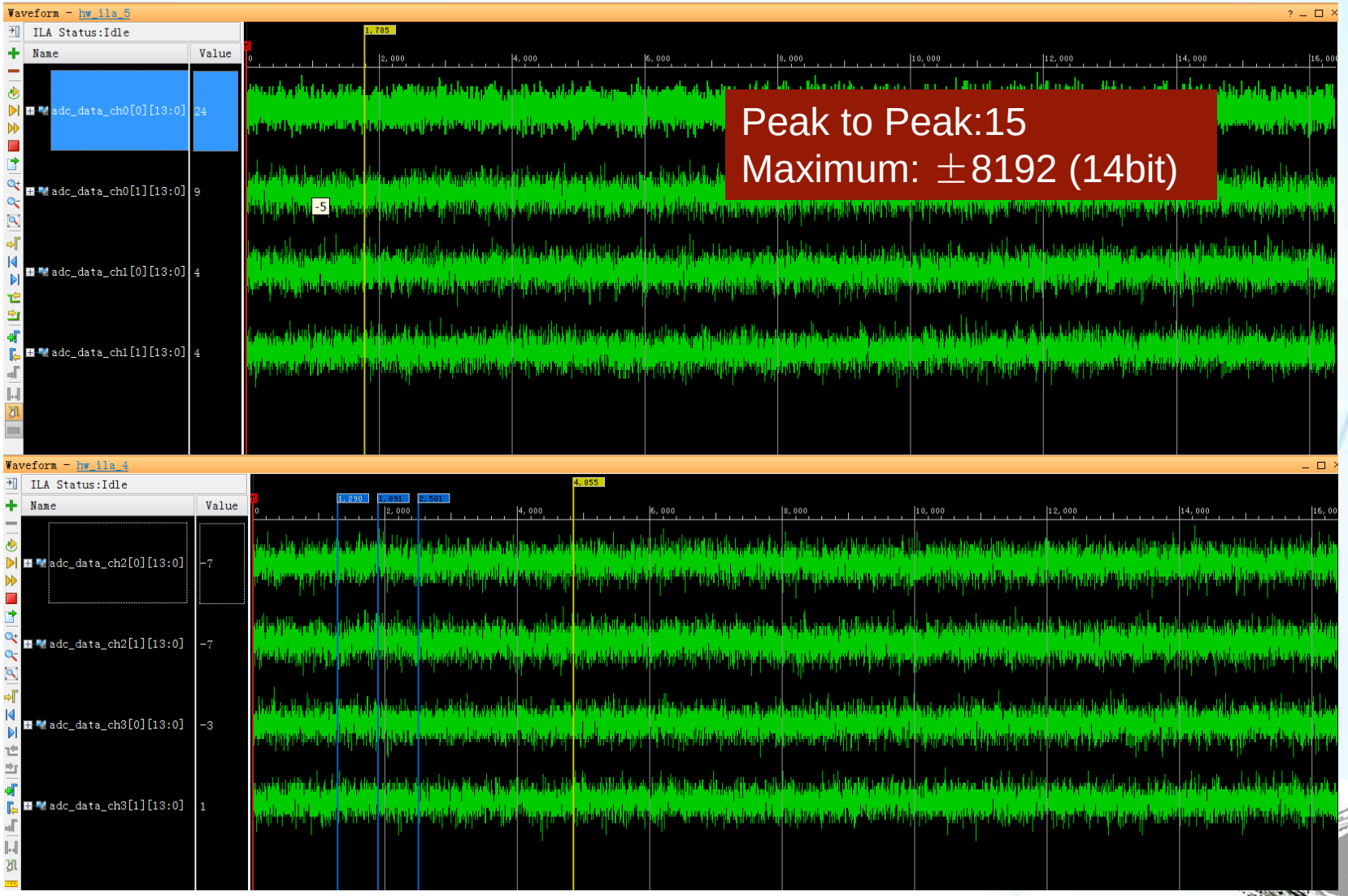
ADC CLK：**500MHz** （Convenient to synchronous two signal generator）（CLK：From ROHDE&SCHWARZ SMA 100A 9KHz-3GHz）

Four Channel ADC **Input**：One to Four Power Splitter, Signal Source：(ROHDE&SCHWARZ SMF 100A 100KHz-22GHz)

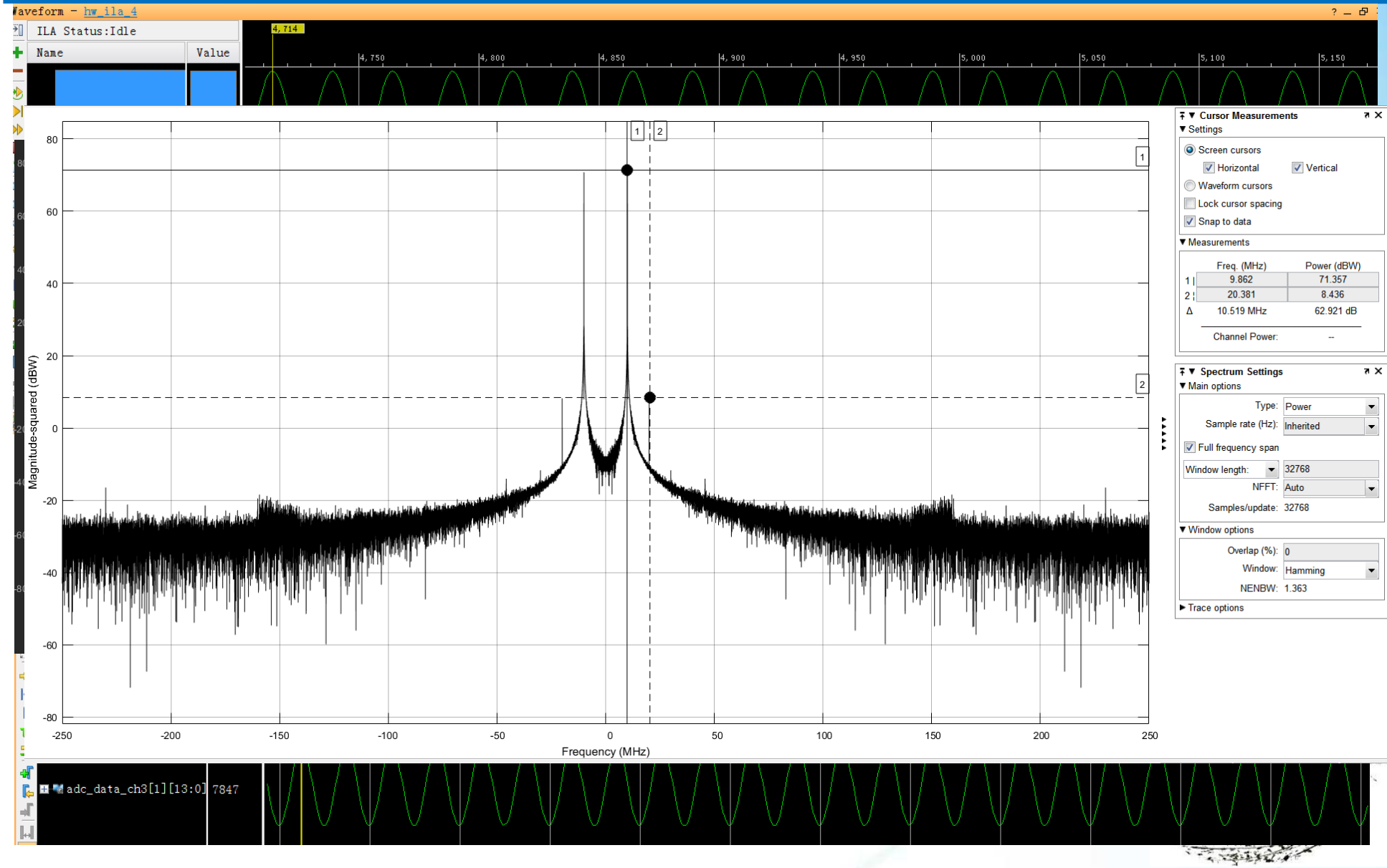




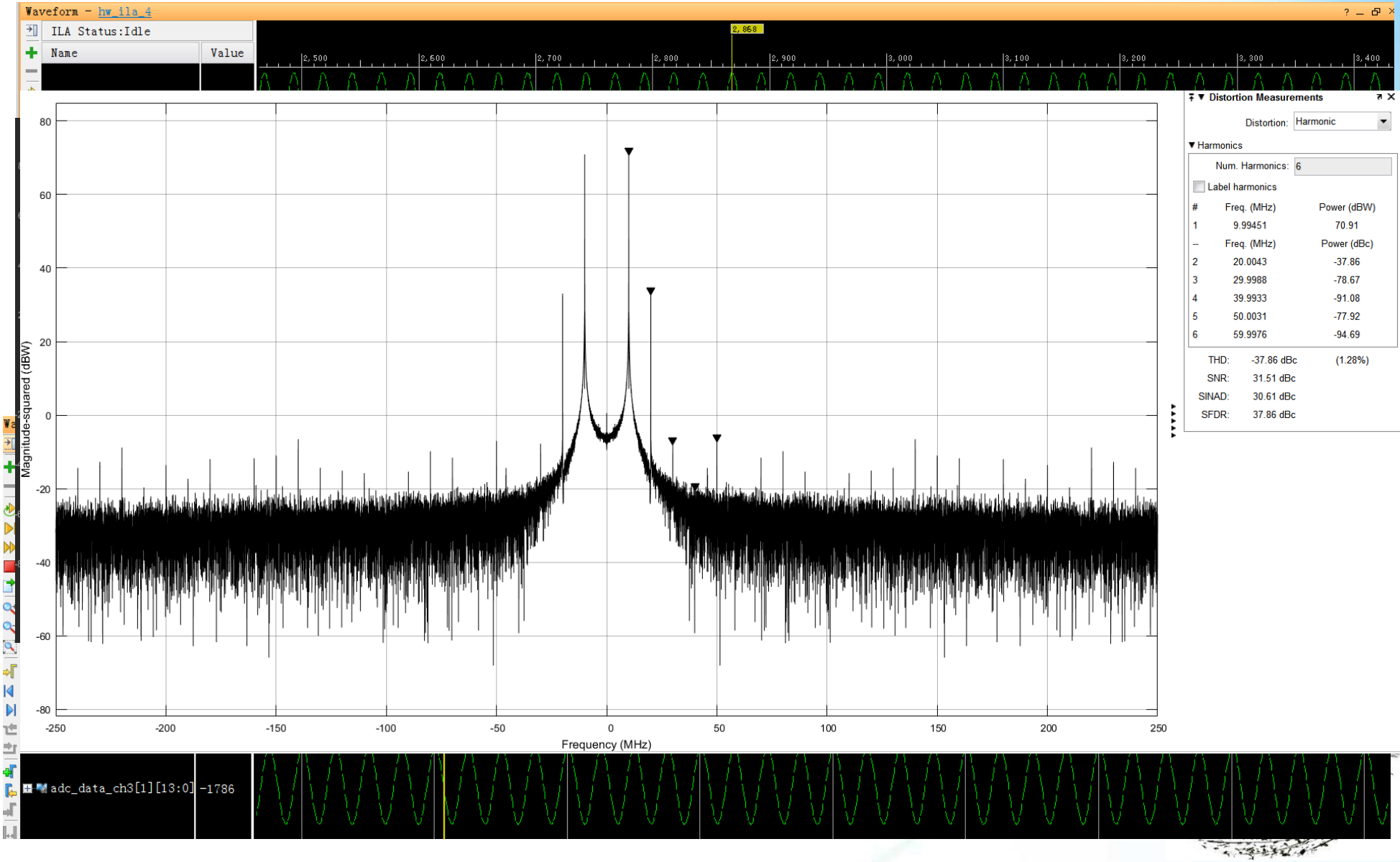
No Input, ADC Raw data



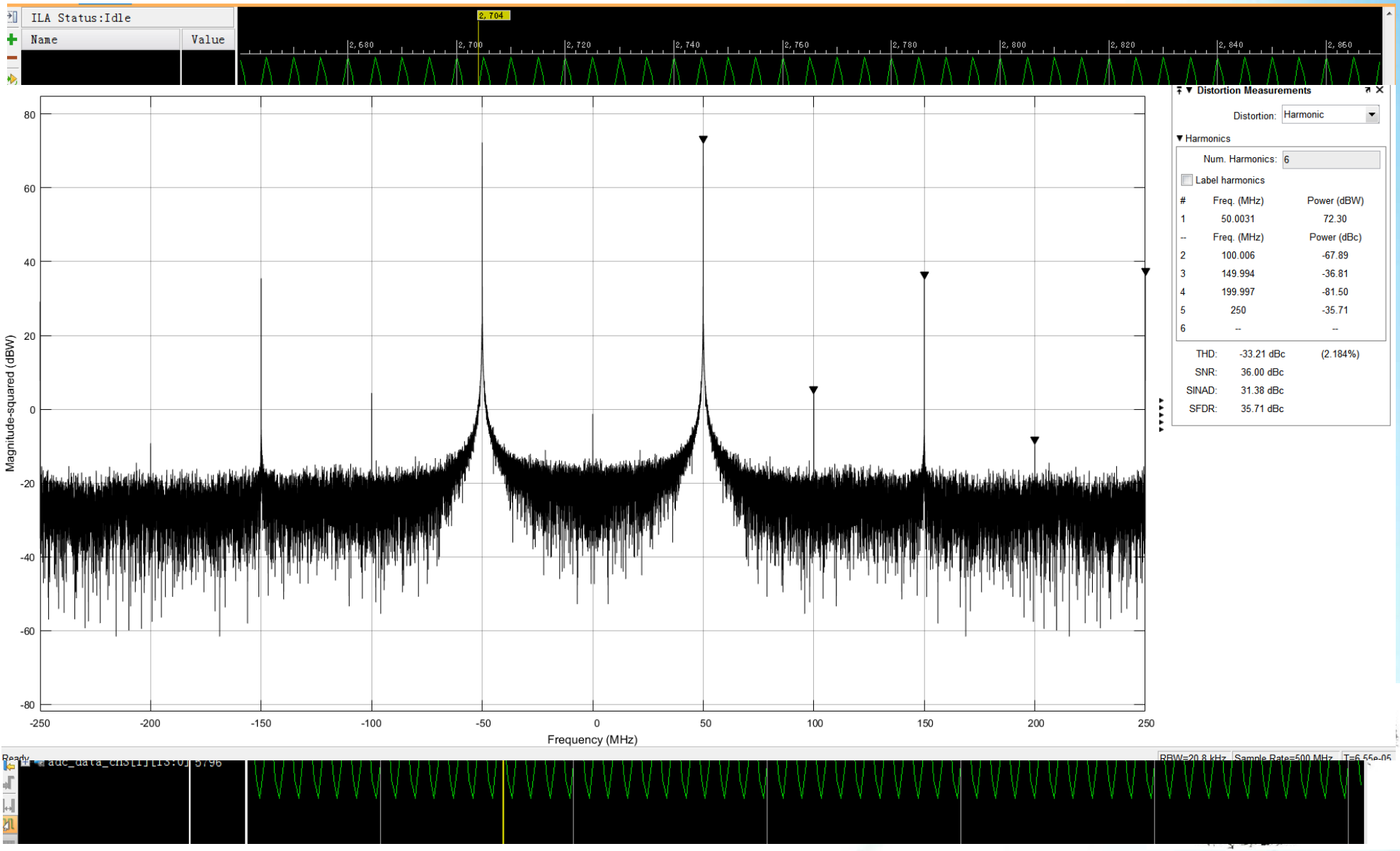
10MHz Input


Waveform - hw_ila_4
ILA Status:Idle
Name
Value
4,714
4,750
4,800
4,850
4,900
4,950
5,000
5,050
5,100
5,150
Cursor Measurements
Settings
Screen cursors
Horizontal
Vertical
Waveform cursors
Lock cursor spacing
Snap to data
Measurements
Freq. (MHz)
Power (dBW)
1 9.862 71.357
2 20.381 8.436
Δ 10.519 MHz 62.921 dB
Channel Power: --
Spectrum Settings
Main options
Type: Power
Sample rate (Hz): Inherited
Full frequency span
Window length: 32768
NFFT: Auto
Samples/update: 32768
Window options
Overlap (%): 0
Window: Hamming
NENBW: 1.363
Trace options
Magnitude-squared (dBW)
80
60
40
20
0
-20
-40
-60
-80
-250
-200
-150
-100
-50
0
50
100
150
200
250
Frequency (MHz)
adc_data_ch3[1][13:0] 7847

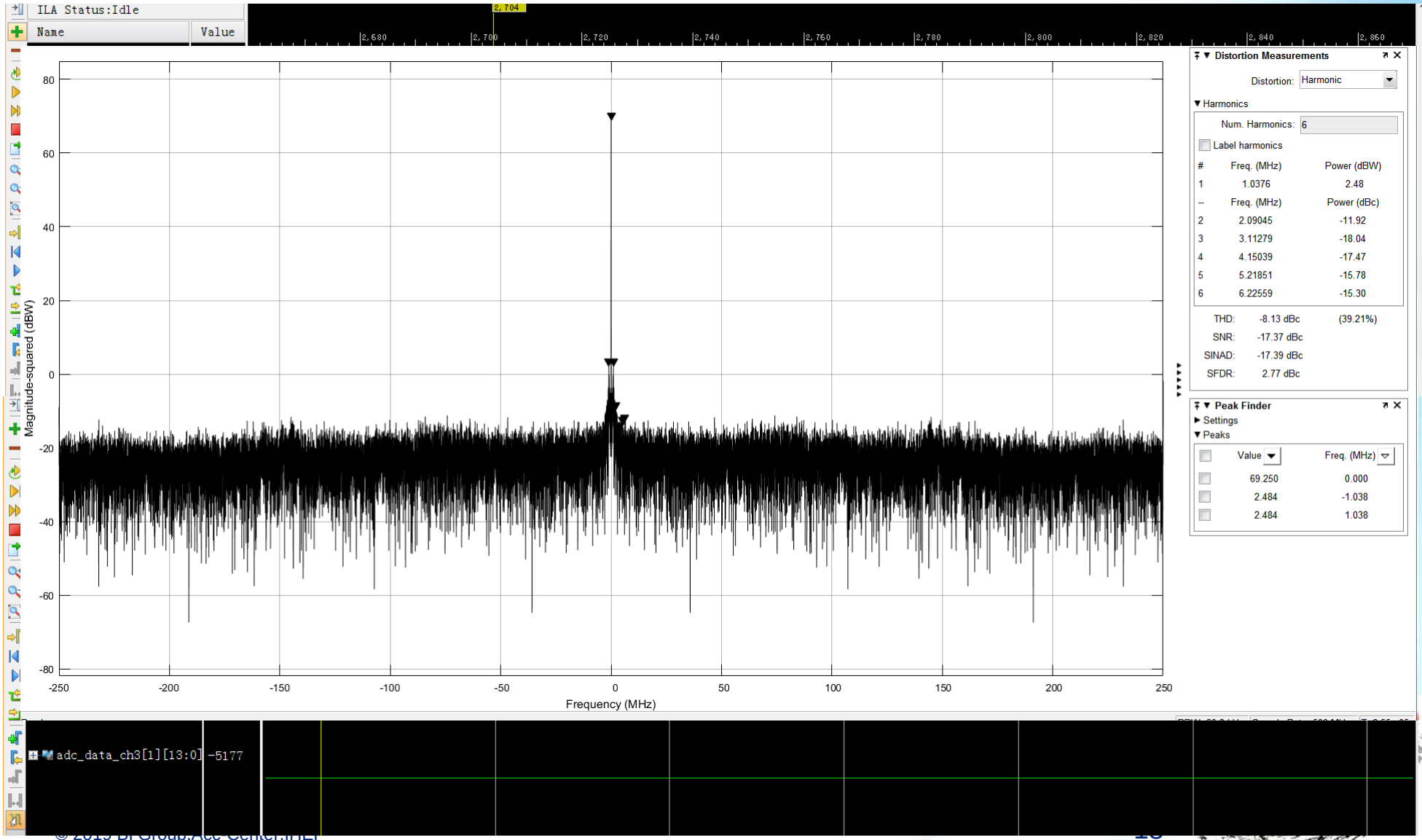
490MHz Input



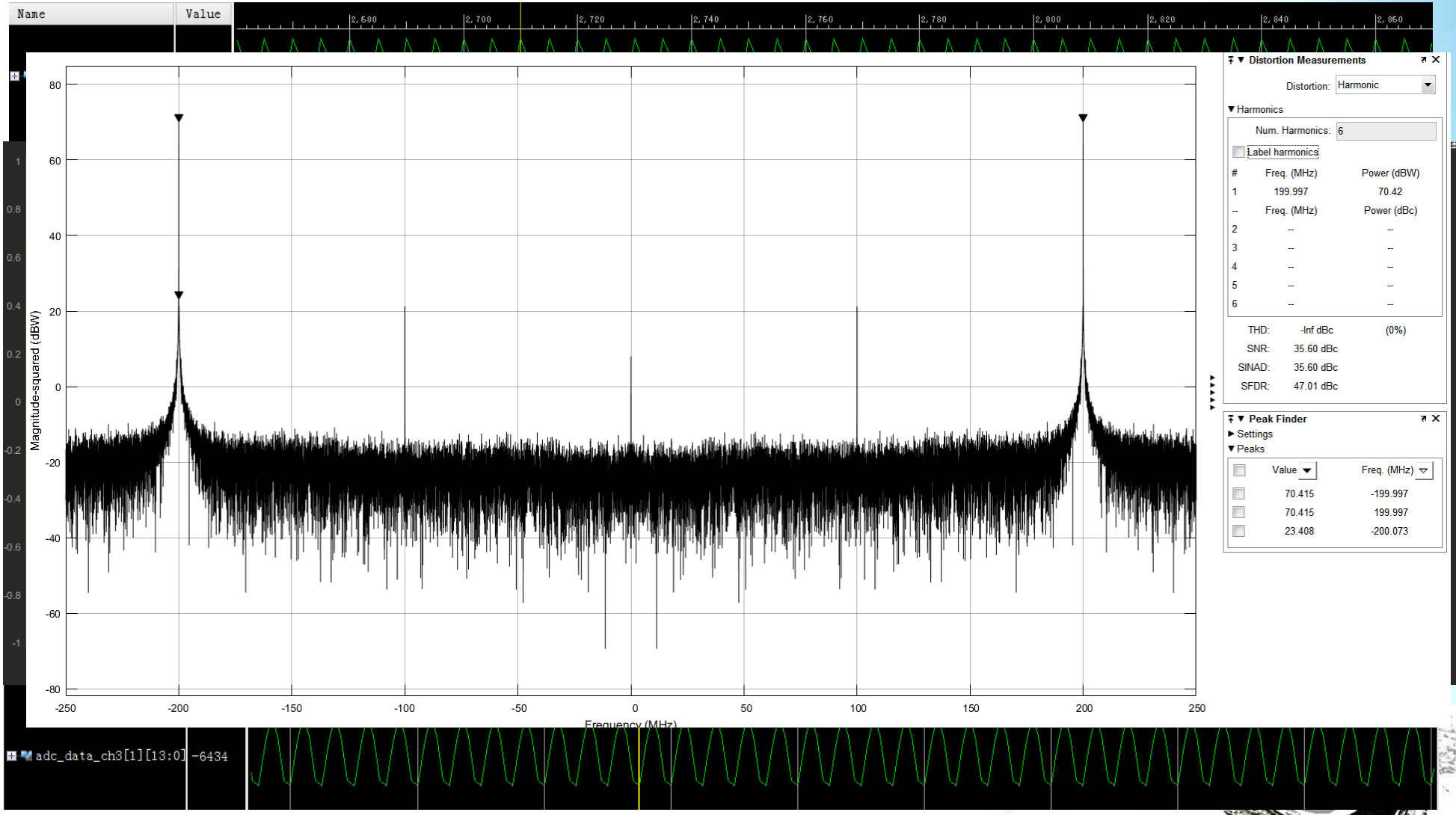
950MHz Input



1.5GHz Input



1.8GHz Input



Summary

- ✓ Bunch-by-Bunch BPM system has been designed.
- ✓ Prototype circuit board has been made.
- ✓ Initial board tests have started.

Next Step:

- ✓ **Develop** : Embedded Linux and EPICS on ZYNQ ARM
- ✓ **Furthermore:** Upgrading Hardware and firmware, adding embedded Timing module…

Thank you !