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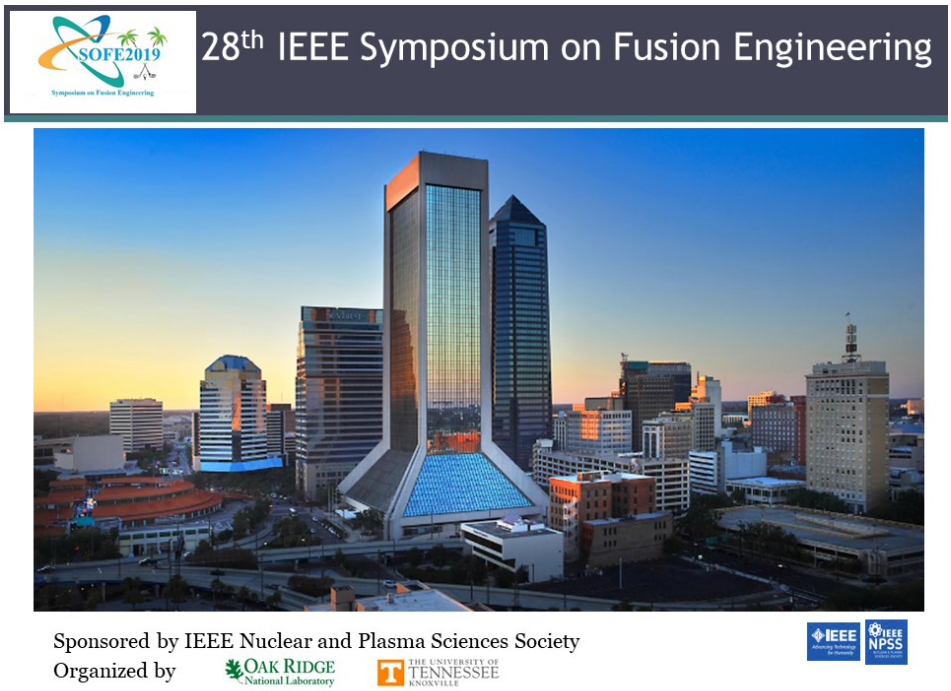

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Book of Abstracts

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Corresponding Author: federico.alessio@cern.ch

427

A true real-time success story: the case of collecting beauty-ful data at the LHCb experiment.

Author: Federico Alessio[1]

Co-author: on behalf of the LHCb Collaboration

[1] *CERN*

Corresponding Author: federico.alessio@cern.ch

The LHCb experiment at CERN is currently completing its first big data taking campaign at the LHC started in 2009. It has been collecting data at more than 2.5 times its nominal design luminosity value and with a global efficiency of ˜92%. Even more striking, the efficiency between online and offline recorded luminosity, obtained by comparing the data quality output, is close to 99%, which highlights how well the detector, its data acquisition system and its control system have been performing despite much harsher and more variable conditions than initially foreseen.

In this paper, the excellent performance of the LHCb experiment will be described, by transversally tying together the timing and data acquisition system, the software trigger, the real-time calibration and the shifters interaction with the control system. Particular attention will be given to their real-time aspects, which allow performing an online reconstruction that is at the same performance level as the offline one through a real-time calibration and alignment of the full detector. In addition, the various solutions that have been chosen to operate the experiment safely and synchronously with the various phases of the LHC operations will also be shown. In fact, the quasi-autonomous control system of the LHCb experiment is the key to explain how such a large detector can be operated successfully around the clock by a pool of ˜300 non-expert shifters. Finally, a critical review of the experiment will be presented in order to justify the reasons for a major upgrade of the detector.

Minioral:

No

Description:

system

Speaker:

Federico Alessio

Institute:

CERN

Country:

Switzerland

426

Timing and clocking scheme in the upgraded LHCb detector

Author: Federico Alessio[1]

Co-authors: Sophie Baron [1]; Julian Maxime Mendez [1]; Jean-Pierre Cachemiche [2]; Pierre-Yves Duval [2]; Frederic Hachon [2]; Frederic Rethore [2]; Guillaume Vouters [2]; Michel Jevaud [3]

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In 2019, the LHCb experiment at CERN will undergo a major upgrade where its detector electronics and the entire readout system will be replaced. The goal is to read-out all events at the full LHC frequency of 40 MHz, reaching a total data rate of ˜40 Tb/s. In this context, a new timing, trigger and fast readout control system has been developed: its main tasks are to distribute centrally the clock, the timing information and to synchronize all elements in the readout system: from the very last Front-End ASIC to the building of events to be stored.

A proper clocking scheme is therefore paramount to make sure that the electronics of the entire readout system is well synchronized with the LHC timing and with the global LHCb upgraded detector. In this paper, the clock scheme as currently used in the upgrade of the LHCb experiment is described in detail, with particular emphasis on the mechanisms, both in FPGA and in hardware design, employed to ensure fixed latency of the clock, deterministic control over the fine phase, low jitter and a narrow frequency spectrum. Measurements for the validation of the scheme are also enclosed.

Minioral:

Yes

Description:

system timing/clock

Speaker:

Federico Alessio

Institute:

CERN

Country:

Switzerland

398

The Readout Supervisor firmware for controlling the upgraded LHCb detector and readout system.

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In 2019, the LHCb experiment at CERN will undergo a major upgrade where its detector electronics and the entire readout system will be replaced. The goal is to read-out all events at the full LHC frequency of 40 MHz, reaching a total data rate of ˜40 Tb/s. In this context, a new timing, trigger and readout control system has been developed: its main tasks are to distribute centrally the clock, the timing information and to synchronize all elements in the readout system: from the very last Front-End ASIC to the building of events to be stored. The heart of the timing and readout control system is a VHDL firmware core that is now finalized and currently in use in test-benches and test-beams by the upgraded sub-detectors, for their initial commissioning phase. Such firmware core is able to generate all necessary processes to keep the synchronization of all readout elements with the LHC bunch crossing as well as it is able to generate asynchronous commands for calibration or test purposes. It is also able to accommodate for specific recipes to handle varying running conditions, by using a generic and fully configurable approach. In this paper, the philosophy and the implementation behind such firmware are described in details, posing particular emphasis to the real-time logical processes that were developed in order to satisfy the requirements of synchronization and readout control of the upgraded LHCb detector.

Minioral:

Yes

Description:

trigger, data throughput

Speaker:

Federico Alessio

Institute:

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Country:

Switzerland

494

The Monitoring System of the EndCap Calorimeter in the Belle2 experiment

Author: Alberto Aloisio[1]

Co-authors: Fabrizio Ameli ; Antonio Anastasio [2]; Paolo Branchini [3]; Francesco Di Capua [4]; Raffaele Giordano [5]; Vincenzo Izzo [2]; Alexandr Kuzmin [6]; Kenkichi Miyabayashi [7]; Isamu Nakamura [8]; Mikihiko Nakao [9]; Gennaro Tortone [2]; Sadaharu Uehara [9]

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The Belle II experiment is presently under construction at the SuperKEKB electron-positron collider in KEK (Tsukuba, J). The detector is a major upgrade of the Belle experiment at the KEKB collider and it is optimized for the study of rare B decays. The new design makes it also sensitive to signals of New Physics beyond the Standard Model, including studies of the dark sector.
The Electromagnetic Calorimeter (ECL) is based on CsI(Tl) scintillation crystals. It splits in a barrel and two annular endcap regions, these latter named Forward and Backward, according to the asymmetric design of the collider.
CsI(Tl) crystals deliver a high light output at an affordable cost, however their yield changes with temperature and can be permanently damaged by humidity, due to the strong chemical affinity for moisture. Each ECL region is then equipped with thermistors and humidity probes to monitor environmental data. While sensors and cabling have been inherited from the original Belle design, the ECL monitoring system has been fully redesigned. In this paper, we present hardware and software architecture deployed for the 2112 CsI(Tl) crystals arranged in the Forward and Backward endcaps. Single-Board Computers (SBCs) have been designed ad-hoc for embedded applications. For sensor read-out, a data-acquisition system based on 24-bit ADCs with local processing capability has been realized and interfaced with the SBCs. EPICS applications send data across the Local Area Network for remote control and display. We discuss sources of error, design strategies and performance achieved, which rivals that of lab-grade equipment.

Minioral:

No

Description:

DAQ board

Speaker:

Alberto Aloisio

Institute:

INFN

Country:

Italy

646

508 Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

645

507 The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters

508

Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Authors: Nicolas Morange[1]; ATLAS LAr Calorimeter Group[None]

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The high-luminosity LHC will provide 5-7 times higher luminosites than the orignal design. An improved readout system of the ATLAS Liquid Argon Calorimeter is needed to readout the 182,500 calorimeter cells at 40 MHz with 16 bit dynamic range in these conditions. Low-noise, low-power, radiation-tolerant and high-bandwidth electronics components are being developed in 65 and 130 nm CMOS technologies. First prototypes of the front-end electronics components show good promise to match the stringent specifications. The off-detector electronics will make use of FPGAs connected through high-speed links to perform energy reconstruction, data reduction and buffering. Results of tests of the first prototypes of front-end components will be presented, along with design studies on the performance of the off-detector readout system.

Minioral:

Yes

Description:

readout scheme

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

507

The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters

Authors: Nicolas Morange[1]; ATLAS LAr Calorimeter group[None]

[1] *Université Paris-Saclay (FR)*

Corresponding Author: nicolas.morange@cern.ch

Electronics developments are ongoing for the trigger readout of the ATLAS Liquid-Argon Calorimeter towards the Phase-I upgrade scheduled in the LHC shut-down period of 2019-2020. The LAr Trigger Digitizer system will digitize 34000 channels at a 40 MHz sampling with 12 bit precision

after the bipolar shaper at the front-end system, and transmit to the LAr Digital Processing system in the back-end to extract the transverse energies. Results of ASIC developments including QA and radiation hardness evaluations, performances of the final prototypes and results of the system integration tests will be presented along with the overall system design.

Minioral:

Yes

Description:

LAr Trigger

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

697

525 Prototype of a multi-host type DAQ front-end system for RI-beam experiments

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525

Prototype of a multi-host type DAQ front-end system for RI-beam experiments

Author: Hidetada Baba[1]

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The multi-host type DAQ front-end system is proposed and a prototype system is developed. In general, CAMAC/VME type ADC modules have a single trigger-input (or gate-input) port. In contrast, a prototype of a new system has multiple trigger-input ports. In addition, the Wilkinson-type and successive approximation ADCs have the dead time, whereas, this prototype system utilizes the combination of Flash-ADC and FPGA that enabling the dead-time free system. Corresponding to the trigger-input ports, data are sent to different back-end systems. So, a legacy ADC module is a 1-to-1 system, but, this proposing system is a 1-to-X system without loss.
This system will be applied for nuclear physics experiments at RIKEN RIBF which produces intense RI-beams. This multi-host type DAQ front-end system enables us to perform different experiments simultaneously at the same beam line. In this contribution, the concept and some performance-test results of the multi-host type DAQ front-end system will be shown.

Minioral:

Yes

Description:

Zynq DAQ

Speaker:

Hidetada Baba

Institute:

RIKEN

Country:

Japan

596

VIVADO High Level Synthesis in CLAS12 Trigger System Design

Authors: Benjamin Raydo[1]; Sergey Boyarinov[1]

[1] *Jefferson Lab*

Corresponding Authors: boiarino@jlab.org, braydo@jlab.org

VIVADO High Level Synthesis was used to design the first stage of the 3-staged CLAS12 Trigger System. It was implemented using Xilinx Virtex7-based VXS trigger processor board specifically designed to be used in the system. Trigger System was successfully complete and used during physics run in Jefferson Lab. Our experience with HLS is described.

Minioral:

Yes

Description:

Trigger

Speaker:

Sergey Boyarinov

Institute:

JLAB

Country:

USA

606

Accelerating HPC codes on Intel(R) Omni-Path Architecture networks: From particle physics to Machine Learning

Author: Peter Boyle[1]

[1] *University of Edinburgh*

We discuss practical methods to ensure near wirespeed performance from clusters with either one or two Intel(R) Omni-Path host fabric interfaces (HFI) per node, and Intel(R) Xeon Phi(TM) 72xx (Knight's Landing) processors, and using the Linux operating system.

Minioral:

Description:

Speaker:

Institute:

Country:

568

An FPGA based high speed network processor - Preprocessing detector images relieving data backend systems

Author: Martin Brückner[1]

Co-authors: Anna Bergamaschi [2]; Roberto Dinapoli [3]; Erik Fröjdh [2]; Dominic Greiffenberg [4]; Dhanya Maliakal [2]; Davide Mezza [2]; aldo mozzanica [2]; Christian Ruder [2]; Bernd Schmitt [3]; Xintian Shi [5]; Gemma Tinti [6]; Jiaguo Zhang [2]; Sabina Chiriotti Alvarez [3]; Carlos Lopez Cuenca [3]; Rebecca Barten [3]; Sophie Eleanor Redfort [3]; Seraphin Vetter [3]; Marie Andrä [7]

[1] *PSI - Paul Scherrer Institut*

[2] *PSI*

[3] *Paul Scherrer Institut*

[4] *PSI - Paul Scherrer Institute*

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At the Paul Scherrer Institut several types of X-ray detectors are being developed. All of them have in common that they use network interfaces to transmit the images to a server for processing and storage.
One, concerning data rate, especially demanding detector is Eiger.
It is module based with 512x1024 pixels and two 10Gbit/s Ethernet connections per module. Since all modules are operated parallel the data rate scales with the size of the detector. So a 1 Megapixel detector with its two modules has four 10 Gbit/s ports and a 9 Megapixel detector with 18 modules 36 10 Gbit/s ports. Since every module can easily saturate the two 10Gb/s Ethernet ports, powerful servers are necessary to receive and sort the arriving network packets.

The current available Xilinx Virtex Ultrascale FPGAs have up to 60 30.5Gb/s GTY transceivers. They are suitable for PCIe and Ethernet connections because of their integrated have a PCIe Gen3 and 100Gb/s Ethernet MAC hard cores.

To unload the host CPU an FPGA design using the MAC and PCIe core in the FPGA has been created. It receives the network packets and reassembles the images in the host memory via PCIe. To do so the network packets are analysed and destination memory address are generated in the FPGA. Finally an interrupt is triggered.
We present the FPGA design as well as first results from a prototype system.

Minioral:

Yes

Description:

image processing

Speaker:

Martin Brückner

Institute:

PSI

Country:

Switzerland

590

Introduction of µTCA DAQ system and parallel reading in CANDLES experiment

Authors: Bui Tuan Khai[1]; Shuhei Ajimura[1]; Kazuki Kanagawa[1]; Tsuyoshi Maeda[1]; MASAHARU NOMACHI[1]; Yorihito Sugaya[1]; Koutaku Suzuki[2]; Masahito Tsuzuki[1]

[1] *Osaka University*

[2] *The Wakasa Wan Energy Research Center*

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Neutrino-less Double Beta Decay ($0\nu\beta\beta$) is an important tool to study absolute neutrino mass and nature of neutrino (Majorana or Dirac particle). Moreover, this phenomenon signals the violation of lepton number conservation, and it has not been observed so far. CANDLES experiment aims to obtain the $0\nu\beta\beta$ from ^{48}Ca. This measurement is a big challenge due to the extremely rare decay rate of ^{48}Ca. To obtain $0\nu\beta\beta$, it is needed to reduce background as much as possible. Series of alpha and beta decays originated from radioactive impurities can remain as background in the energy region of $0\nu\beta\beta$. Because they are sequential decays, we can remove them by tagging preceding and following events. This tagging method requires minimized dead-time of DAQ system. A new µTCA DAQ system was introduced with SpaceWire-to-GigabitEthernet (SpW-GbE) network for data readout and FADCs equipping 8 event buffers. Event buffers, which act as de-randomizer, help reduce dead-time. SpW-GbE has high latency (about 100 µsec) due to long turnaround time, but GbE has high throughput. Thus, for minimization of dead-time, we developed our DAQ system with 4 "module-parallel"reading threads (modules are read in parallel). As a result, the read-time is reduced by 4 times: 40msec down to 10msec. With improved performance, it is expected to achieve higher background suppression for CANDLES experiment. Moreover, for energy calibration, "event-parallel"reading process (events are read in parallel) is also introduced to reduce measurement time. With 2 "event-parallel"reading processes, the data rate is increased 2 times.

Minioral:

Yes

Description:

uTCA

Speaker:

Bui Tuan Khai

Institute:

Osaka University

Country:

Japan

663

594 Back-end Electronics based on an Asymmetric Network for Low Background and Medium Scale Physics Experiments

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594

Back-end Electronics based on an Asymmetric Network for Low Background and Medium Scale Physics Experiments

Author: Denis Calvet[1]

[1] *CEA/IRFU, Centre de Saclay (FR)*

Corresponding Author: calvet@hep.saclay.cea.fr

The readout architecture introduced in this paper is intended for small to medium size physics experiments that have moderate bandwidth needs, and applications that require ultimately low background radioactivity front-end components. I detail a protocol based on time division multiplexing to transport from a back-end unit over a low speed fanout network –which could simply consist of a multi-drop cable –all the information required to synchronize, configure, monitor and control the read out of multiple front-end devices. A set of medium speed unidirectional point-to-point links connect front-end units to a common back-end, and transport simultaneously synchronous traffic, acquired data and slow control. Using links of the minimum required speed gives large freedom to select optimal materials among copper media, glass optical fibers coupled to transceivers based on laser diodes, or visible LEDs transmitters attached to plastic optical fibers. On the front-end link receiver side, I demonstrate the use of a clock and data recovery circuit which overcomes the lower speed bound of serial transceivers embedded in FPGAs. I show the design of a back-end unit capable of controlling 32 front-end units at up to 10 Gbps of aggregate bandwidth using an inexpensive commercial FPGA module where the comparatively large number of regular I/O pins interface to the front-end links, while the few available multi-gigabit per second capable transceivers are affected to the communication with the upper stage of the DAQ system. I describe several deployment scenarios and explain how some other applications could benefit from the described concepts.

Minioral:

Yes

Description:

network

Speaker:

Denis Calvet

Institute:

CEA

Country:

France

526

Readout electronics for a boron-coated multi-wire proportional chamber neutron detector

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Co-author: Ping Cao [4]

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In order to deal with the international problem of shortage of 3He, a new type of boron-coated Multi-wire proportional chamber (MWPC) thermal neutron detector is developed. Readout electronics for it, which can achieve good position resolution, is introduced in this paper. In this readout electronics, hit signal from MWPC detector is fed into the delay line module propagates towards to both directions. After be conditioned by front-end electronics (FEE), hit signal is signaled with differential Low Voltage Differential Signal (LVDS) level and fed to a Nuclear Instrument Module (NIM) time digitizing module. For the purpose of precision, simplicity and flexibility, the time digitizer s implemented in Field Programming Gate Array (FPGA). Each digitizer module can support up to 20 electrical channels. To correctly select the analog signal conditioning parameters, a complete theoretical analysis of the delay line module is put forward in this paper. Lab test shows that the time resolution contributed by readout electronics is better than 700ps with dead time about 550ns. Joint test with MWPC detector shows that the integral position resolution is better than 3mm which can meet the requirement of thermal neutron detection.

Minioral:

No

Description:

FPGA-TDC

Speaker:

Ping Cao

Institute:

USTC

Country:

China

439

FPGA Based Pico-second Time Measurement System for a DIRC-like TOF Detector

Authors: Qiang Cao[1]; Xin Li[2]

Co-authors: Liwei Wang [2]; Jie Kuang [2]; Yonggang Wang [2]; Cheng Li [2]

[1] *Department of Modern Physics,University of Science and Technology of China*

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A prototype of DIRC-like Time-of-Flight detector (DTOF), including a pico-second time measurement electronics, is developed and tested preliminarily. The basic structure of DTOF is composed of a fused silica radiator connected to fast micro-channel plate PMTs (MCP-PMT), and readout by a dedicated FPGA (Field Programmable Gate Array) based front-end electronics. The full electronics chain consists of a programmable differential amplifier, a dual-threshold differential discriminator, and a timestamp Time-to-Digital convertor. By splitting a MCP-PMT output signal into two identical electronics chains, the coincidence time resolution (CTR) of pure electronics was measured as 5.6 ps. By the beam test in H4 (150GeV/c, Muon) at CERN, the intrinsic CTR of the whole detector prototype reaches 15.0 ps without using time-amplitude correction. The test results demonstrate that the FPGA based front-end electronics could achieve an excellent time performance for TOF detectors. It is very compact, cost effective with a high multi-channel capacity and short measurement dead time, which is very suitable for practical applications of large-scale high performance TOF detectors in particle physics spectrometer.

Minioral:

Yes

Description:

Wilkinson ADC_FPGA

Speaker:

Qiang Cao

Institute:

USTC

Country:

China

699

537 Design of a Programmable Gain Waveform Digitization Instrument for Detector Calibration

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537

Design of a Programmable Gain Waveform Digitization Instrument for Detector Calibration

Authors: Zhe Cao[1]; Jiadong Hu[2]; Cheng Li[1]; Shupeng Yu[1]; Shubin Liu[1]; Qi An[1]

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To test and calibrate various detectors in nuclear and high energy physics experiments, a general purposed calibration instrument has been developed. All information including timing, amplitude and charge of signals can be directly obtained to calibrate detector with this instrument by amplifying and digitizing the signal waveform. The system consists of two parts, a large dynamic range pre-amplifier module and a high speed and high-resolution digitization module. The pre-amplifier module based on programmable gain amplifier and attenuator achieves gain from -20 dB to 33 dB, making it suitable to adapt to different detectors. Taking advantage of a 3.6 GSPS and 12-bit resolution analog-to-digit converter (ADC), the waveform digitization module samples the signal after conditioning. To evaluate the feature of this instrument, a BaF2 detector calibration platform was installed and test results showed a bandwidth from DC to 500MHz and a timing precision about 280 ps, which indicated that it had broad application prospect in detector calibration.

Minioral:

Yes

Description:

Design gain control WFD

Speaker:

Zhe Cao

Institute:

USTC

Country:

China

638

478 Clock Distribution and Readout Architecture for the ATLAS Tile Calorimeter at the HL-LHC

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Clock Distribution and Readout Architecture for the ATLAS Tile Calorimeter at the HL-LHC

Authors: ATLAS Tile Calorimeter System[1]; Fernando Carrio Argos[2]

[1] *ATLAS experiment*

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The Tile Calorimeter (TileCal) is one detector of the ATLAS experiment at the Large Hadron Collider (LHC). TileCal is a sampling calorimeter made of steel plates and plastic scintillators which are readout using approximately 10,000 Photo-Multipliers Tubes (PMTs).
In 2024, the LHC will undergo a series of upgrades towards a High Luminosity LHC (HL-LHC) to deliver five times the current nominal instantaneous luminosity. The ATLAS Tile Phase II Upgrade will accommodate detector and data acquisition system to the HL-LHC requirements. The detector electronics will be completely redesigned using a new clock distribution and readout architecture with a full-digital trigger system.
After the Phase II Upgrade in 2026, the on-detector electronics will transfer digitized data for every bunch crossing (˜25 ns) to the Tile Pre-Processors (TilePPr) in the counting rooms with a total data bandwidth of 40 Tbps. The TilePPrs will store the detector data in pipeline memories to cope with the new ATLAS DAQ architecture requirements, and will interface with the Front End Link eXchange (FELIX) system and the first trigger level.
The TilePPr boards will distribute the sampling clock to the on-detector electronics for synchronization with the LHC clock with fixed and deterministic latency.
The upgraded readout strategy has been fully validated in a Demonstrator system using prototypes of the upgraded electronics in several test beam campaigns between 2015 and 2017.
This contribution presents a detailed description of the new clock and readout architecture, and the status of the readout electronics for TileCal at the HL-LHC.

Minioral:

Yes

Description:

clock dist.

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

688

466 Development of a 256-channel Time-of-flight Electronics System For Neutron Beam Profiling

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466

Development of a 256-channel Time-of-flight Electronics System For Neutron Beam Profiling

Authors: Haolei Chen[1]; Jiadong Hu[2]; Li Wang[1]; Zhixin Tan[3]; Shubin Liu[4]

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China Spallation Neutron Source is mainly used for nuclear data measurements. In order to achieve the energy of neutron, one method is to measure the time that the neutron spends to travel along a fixed distance. So we developed a time-of-flight electronics system for the experiment. In order to detect the hit position of the neutron for beam profiling, we use a detector with 256 channels, of which the effective area is 49mm×49mm. Therefore, the system is expected to deal with 256 channels'output from the detector. The article mainly discusses a 256-channel time-of-flight electronics system. Each channel on the front end board (FEB), utilizing the technology of leading edge timing, can output a LVDS signal which contains the information of the time when neutron hits the channel of the detector. Then time-to-digital converter (TDC) boards, which have 64 channels, achieve the signals from FEB as stop signals. The start signal is provided according to the time when neutron begins to fly. TDC boards measure the time between the leading edge of start signal and stop signals by a method called clock phase separation technology. According to the test result, the TDC board has 6.25ns resolution and 3.5ns precision. The time-of-flight measurement system has already been used in the experiment of China Spallation Neutron Source.

Minioral:

Yes

Description:

TOF board

Speaker:

Haolei Chen

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USTC

Country:

China

493

The Design and Test of LAr Trigger Digitizer Board in ATLAS Phase-I Upgrade

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The LHC upgrade is planned to enhance the instantaneous luminosity to 2-3×1034 cm-2s-1 during Run 3 from 2021 through 2023. The Phase-I upgrade of the trigger readout electronics for the ATLAS Liquid Argon (LAr) Calorimeters will be installed during the second long shutdown of LHC in 2019/2020. In this upgrade, so-called Supercells are introduced to provide higher granularity, higher resolution and longitudinal shower shape information from the LAr calorimeters to the Level-1 trigger processors. A new LAr Trigger Digitizer Boards (LTDB) will process and digitize 320 channels of Supercell signals, and transmit it to the back-end processors via 40 fiber optical links where data are further processed and transmitted to the trigger processors. Five pairs of bidirectional GBT links are used for slow control. LTDB also sends 64 summed analog signals to the Tower Builder Board through the baseplane, to maintain the present analog L1 trigger functionality as a possible backup system.
A test system is developed to test all functions of LTDB and perform the performance measurement. A back end PCIe card is designed which has the interface to the ATLAS TTC system. It can control the generation of injection signals to the LTDB for performance test. It can also communicate with the GBTx, and all ASICs on LTDB via GBT-SCA (Slow Control Adapter) through fiber optical links. A front-end test board, test baseplane and a crate will be designed to extend the capability of the test setup, which will be used for the production test of 124 LTDBs.

Minioral:

No

Description:

LAr Trigger

Speaker:

Kai Chen

Institute:

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Country:

USA

674

418 The Detector System Design for the Grating-based Phase Contrast Imaging CT Prototype

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418

The Detector System Design for the Grating-based Phase Contrast Imaging CT Prototype

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In the hard X rays domain, the phase shift of the wave passing through the soft materials like tissues is typically three orders of magnitude larger than the absorption. Therefore the phase-sensitive X-ray imaging methods can obtain substantially increased contrast over conventional absorption-based imaging. The grating-based phase contrast imaging(GBPCI), which can achieve a large field of view with low requirement on time and spatial coherence of the light source, is considered as a potential imaging method for clinical applications. A CT prototype based on GBPCI is developed by National Synchrotron Radiation Laboratory (NSTL), and the detector system for the prototype is designed.
The detector of the prototype consists of 43 Hamamatsu silicon photodiode S12058(X) modules to achieve 200mmx200mm measurement field of view. Each S12058(X) module can provide maximum 384(16x24 pixels) outputs, which the minimum pixel size is 0.75mmx1mm. The detector output low-level current is transmitted to the front-end readout electronics via the high density connector. The Ti DDC1128 are used to complete both current-to-voltage and A/D conversion. After the linear correction and time drift correction in FPGA, the digital signal is converted to the imaging data, and sent to the control system through a data buffer.
The test result shows that the SNR of the detector system is about 14.6 bits which can satisfy the 14.3 bits dynamic range requirement of the prototype experimental platform. The spatial resolution can reach about 0.38mm which close to the theoretical value 0.36mm for the principle experiment.

Minioral:

Yes

Description:

Algo

Speaker:

Lian Chen

Institute:

USTC

Country:

China

495

The Design of Data Acquisition System for EAST Technical Diagnostic System

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EAST (Experimental Advanced Superconducting Tokamak) Technical Diagnostic System (TDS) is used to monitor the outlet temperature of all superconducting coils, in case of temperature anomaly,

it will trigger safety interlock system to meet EAST device safety. The data acquisition system of TDS (TDS_DAQ) is in charge of continue data acquisition of the nitrogen and helium temperature signals, TDS security alarm and long-term data storage. TDS_DAQ has several modules. (a) Data acquisition. TDS uses different thermometers to measure the nitrogen and helium temperature signals, led to different data acquisition methods. The data acquisition of the nitrogen temperature signals is based on the PXI technology while obtaining the helium temperature signals with VISA standard. (b) Data processing. The measured value of nitrogen signals should be converted with linear formulas, while the helium signals don't need any conversion due to the front end has done. After conversion, the data is stored in MySQL and MDSPlus, using for long-term storage. (c) Security alarm. After threshold evaluation of some key temperature signals, it outputs TDS fault signal and the status signal to trigger the safety interlock system to take actions. (d) Data transmission. TDS_DAQ keeps transferring the TDS data to the cryogenic system via TCP/IP and provides an information inquiry service which is convenient for the TDS administrator to get the alarm information and the TDS data. TDS_DAQ has been deployed and will be used in 2018 EAST campaign.

Minioral:

No

Description:

DAQ for diagnostics

Speaker:

Ying Chen

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IPP Hefei

Country:

China

579

High loaded quality factor superconducting cavities accelerating field parameters regulation during continuous wave operation

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Superconducting niobium cavities are main accelerating components in various research facilities. These installed in the European X-ray Free Electron Laser and other free electron lasers are operated in high gradient range (above 20 MV/m). Electron beam acceleration is realized in short (1-2ms) pulse mode in some devices or in continuous wave in case of others.
EXFEL or FLASH have been designed to be a short pulse machines. Nowadays switching from short pulse to long pulse or CW mode is investigated. Current paper describes extensions of the short pulse mode dedicated Low Level Radio Frequency (LLRF) control systems. Main goal of this accelerator sub-component is to provide accurate regulation of amplitude and phase parameters of accelerating field to achieve best energy transfer to the electron beam. Proposed modifications and adjustments have been introduce to verify system versatility in different cavities operation modes

support. LLRF system potential have been successfully verified with single cryomodule that consists of 8 superconducting structures (with 1,3 GHz fundamental frequency). The same system (with slightly adjusted software) is being used for both SP and CW operation.
CW scenario requires better energy management and precise control in case of cavities working with high quality factor conditions (Ql). System test results that almost fulfill short pulse linac regulation performance requirements in case of this challenging system configuration are also presented and discussed.

Minioral:

No

Description:

Speaker:

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Institute:

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Poland

576

PCIe Hot Plug support standardization challenges in ATCA

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Throughout the last decade, ATCA solidified its position as one of the main standards for advanced Physics instrumentation, in particular hard real-time control and data acquisition applications, using PCIe as the preferred communications protocol.
ATCA offers not only highly performant characteristics in data throughput, channel density or power supply/dissipation capabilities, but also special features for high-availability (HA), required for latest and upcoming large-scale endeavours, as is the case of ITER. Hot Swap is one of the main HA features, allowing for a board to be replaced within a Shelf, without powering-off the whole system, thus ensuring continuity of operation.
Platforms using PCIe on the Fabric Interface (PICMG 3.4) must be complemented with the PCIe Hot Plug functionality, so that hot insertion/extraction of (hardware) Boards is followed by the respective add/removal of the (software) PCIe devices and other higher-level interacting applications. However, PICMG 3.4 does not specify an implementation for Hot Plug.
From a customised Hot Plug solution, developed by IPFN for the ITER Fast Plant System Controller ATCA platform, this paper identifies the main issues for achieving PCIe Hot-Plug support in ATCA,

such as implementability of Hot Plug Elements, generation and management of Hot Plug Events, and compatibility with ATCA Hot Swap. Also addressed are matters of Hot Plug for PCIe external cable connections, as many PICMG 3.4 systems use external host computers. This paper aims to stimulate the discussion within the PICMG community towards a standardization of Hot Plug in ATCA.

Minioral:

Yes

Description:

PCIe

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Miguel Correia

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IPFN

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Portugal

625

442 The Phase-1 Upgrade for the Level-1 Muon Barrel Trigger of the ATLAS Experiment at LHC

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The Phase-1 Upgrade for the Level-1 Muon Barrel Trigger of the ATLAS Experiment at LHC

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The Level-1 Barrel Trigger of the ATLAS Experiment is based on Resistive Plate Chambers (RPC) detectors. The on-detector trigger electronics identifies muons with specific values of transverse momentum (pT) using of coincidences between different layers of detectors. Trigger data is then transferred from on-detector to the off-detector trigger electronics boards. Data is processed by a complex system, which combines trigger data from the barrel and the endcap regions, and provides the combined muon candidate to the Central Trigger Processor (CTP).
The system performed very well for almost a decade. However, to cope with continuously increasing LHC luminosity and more demanding requirements on trigger efficiency and performance, various upgrades for the full trigger system were already deployed, and others are foreseen in the next years. Most of the trigger upgrades are based on state-of-the-art technologies and allow designing more complex trigger menus, increasing processing power and data transfer bandwidth. Thus, it will be possible to send more trigger candidates, to perform topological selections, and to support new physics studies.
In this paper, we describe the design of the first prototype of the new Barrel Interface Board, designed around a Xilinx FPGA, which transfers RPC trigger data to the CTP system; the board supports the

optical transmission of the trigger data with fixed latency and new trigger algorithms. We discuss the design strategies, the hardware implementation and the results of the first functional and integration tests.

Minioral:

Yes

Description:

L2 muBarrel

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

441

The Phase-1 Upgrade of the ATLAS Level-1 Endcap Muon Trigger

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The LHC is expected to increase its instantaneous luminosity to 3.0 × 10ˆ34 cmˆ(-2)sˆ(-1) after the 'Phase-1' upgrade scheduled from 2019 to 2020. In order to cope with the high luminosity, an upgrade of the ATLAS trigger system is required. The level-1 Endcap Muon trigger system identifies muons with high transverse momentum by combining data from a fast muon trigger detector, TGC, and some inner station detectors. In the Phase-1 upgrade, a new detector called the New-Small-Wheel (NSW) will be installed in the inner station region. Finer track information from the NSW can be used as part of the muon trigger logic to enhance performance significantly.
In order to handle data from both TGC and NSW, some new electronics have been developed, including the trigger processor board known as Sector Logic (SL). The SL board has a modern FPGA to make use of Multi-Gigabit transceiver technology, which will be used to receive data from the NSW. The readout system for trigger data has also been re-designed, with the data transfer implemented with TCP/IP instead of a dedicated ASIC. This makes it possible to minimise the use of custom readout electronics and instead use some commercial PCs and network switches to collect, format and send the data.
This paper describes the aforementioned upgrades of the level-1 Endcap Muon trigger system. Particular emphasis is given to the electronics and its firmware.

Minioral:

Yes

Description:

L1 trigger

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

469

FELIX: the new detector interface for the ATLAS experiment

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During the next major shutdown (2019-2020), the ATLAS experiment at the LHC at CERN will adopt the Front-End Link eXchange (FELIX) system as the interface between the data acquisition, detector control and TTC (Timing, Trigger and Control) systems and new or updated trigger and detector front-end electronics. FELIX will function as a router between custom serial links from front-end ASICs and FPGAs to data collection and processing components via a commodity switched network. Links may aggregate many slower links or be a single high bandwidth link. FELIX will also forward the LHC bunch-crossing clock, fixed latency trigger accepts and resets received from the TTC system to front-end electronics. The FELIX system uses commodity server technology in combination with FPGA-based PCIe I/O cards. The FELIX servers will run a software routing platform serving data to network clients. Commodity servers connected to FELIX systems via the same network will run the new Software Readout Driver (SW ROD) infrastructure for event fragment building and buffering, with support for detector or trigger specific data processing, and will serve the data upon request to the ATLAS High Level Trigger for Event Building and Selection. This presentation will cover the design and status of FELIX, the SW ROD, and results of early performance testing.

Minioral:

Yes

Description:

FELIX (FE Link eXchange)

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

524

The Design and Performance of the Real-time Software Architecture for the ITER Radial Neutron Camera

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Co-authors: Bruno Santos [2]; Ana Fernandes [3]; Paulo Carvalho [1]; Jorge Sousa [4]; Bruno Gonçalves [3]; Marco Riva [5]; Cristina Centioli [6]; Daniele Marocco [6]; Basilio Esposito [5]; Carlos Correia [7]; Benoit Brichard [8]; Rita Costa Pereira [3]

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The neutron detection system for characterization of emissivity in ITER Tokamak during DD and DT experiments poses serious challenges to the performance of the diagnostic control and data acquisition system (CDAcq). Ongoing design of the ITER Radial Neutron Camera(RNC) diagnostic comprises 26 lines-of-sight(LOS) for complete plasma inspection. CDAcq system aims at meeting ITER requirements of delivering neutron emissivity profile real-time measurement with time resolution and control cycle time of 10ms at peak event rate of 2MEvents/s per LOS, with neutron spectra generation, neutron/gamma discrimination and pile up rejection. Neutron spectra can be totally processed in the host CPU or using processed data from the system FPGA[1]. The number of neutron counts extracted from the spectra is then used to calculate the neutron emissivity profile using an inversion algorithm. Moreover, it is required that the event based raw data acquired for post processing which can go up to 0.5GB/s per channel data throughput, is made available to the ITER data network without local data storage. The evaluation of real-time data compression techniques in RNC is depicted in another contribution to this conference[2].

To meet the demands of the project a CDAcq prototype has been used to design and test high-performance distributed software architecture taking advantage of multi-core CPU technology capable of coping with requirements. This submission depicts the real-time design architecture, real-time control cycle for ITER advanced plasma control, spectra construction algorithm and inversion algorithm to calculate the emissivity profile. Preliminary system's performance results with synthetic data are presented.

Minioral:

Yes

Description:

RT architecture

Speaker:

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Institute:

IPFN

Country:

Portugal

588

ECAL DAQ system: electronics auto-recovery and monitoring

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The Compact Muon Solenoid (CMS) is a general-purpose detector operating at the LHC. The CMS Electromagnetic Calorimeter (ECAL), based on PbWO4 crystals, has shown excellent performance with a very stable data acquisition system even during higher LHC luminosity peaks.

ECAL DAQ system follows a modular and scalar schema. During the data taking, the Front End electronics is prone to occasional errors, induced by particles interactions. If these errors are not handled opportunely they can cause data loss in the section affected or even blocking the data taking of the experiment.

To prevent these situations, an automatic recovery mechanism has been developed in the ECAL DAQ software. The software dedicated to the configuration of the boards have been modified to check periodically their status. Depending on the level of the error they can trigger a reconfiguration of a single component or of the full board, or even mask the affected section and exclude it from the resuming run.

In this frame it is crucial to provide to the experts a real time view of the electronics status. For this purpose a web application, running on a light JavaScript server framework based on Node.js and Express.js, has been developed.
It is composed by routines that cyclically collect the status of the electronics and expose the information to web requests. On client side, graphical interfaces, based on Vue.js libraries, ask for the data (only if new information are available) and show the main information of the electronics status and errors.

Minioral:

No

Description:

Ecal DAQ

Speaker:

Giacomo Cucciati

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CERN

Country:

Switzerland

665

600 First large-scale real-time drift compensation for Low-Level-RF-stations at the European XFEL

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600

First large-scale real-time drift compensation for Low-Level-RF-stations at the European XFEL

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For a reliable and robust operation of free-electron lasers with bunch-arrival time variations on the sub-10fs scale, the short-term and long-term RF stability of the cavity field is a crucial factor. The long-term RF stability depends mainly on temperature and humidity changes acting on various electronic subcomponents of the accelerator. For the European XFEL we used a drift compensation module operating at 1.3GHz to remove long-term amplitude and phase variations of the MicroTCA.4 Low-Level-RF control system on the fs-scale. The module showed excellent suppression of environmental temperature and humidity changes of about two magnitudes down to an amplitude and phase stability of 0.01%, respectively 0.01deg or 20fs (all peak-to-peak values). In this article we present the method, hardware, performance and operation of the module.

Minioral:

Yes

Description:

uTCA for LLRF

Speaker:

Krzysztof Czuba

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Country:

Poland

668

397 Design of 32-channel TDC Based on Single FPGA for μSR Spectrometer at CSNS

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Design of 32-channel TDC Based on Single FPGA for μSR Spectrometer at CSNS

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Muon Spin Rotation, Relaxation and Resonance (uSR) technology has an irreplaceable role in studying the microstructure and properties of materials, especially micro-magnetic properties. An experimental muon source is being built in China Spallation Neutron Source (CSNS) now. At the same time, a 128-channel uSR spectrometer as China's first uSR spectrometer is being developed. The time spectrum of uSR can be obtained by fitting the curve of positron count rate with time. This paper presents a 32-channel Time-to-Digital Converter (TDC) implemented in a Xilinx Virtex-6 Field Programmable Gate Array (FPGA) for measuring the positron's flight time of μSR Spectrometer. Signal of each channel is sampled by 16 equidistant shifted-phase 200 MHz sampling clocks, so the TDC bin size is 312.5ps. The measuring range is up to 327us. This TDC has the ability to store multiple hit signals in a short time with a deep hit-buffer up to 512. Time tag is added to each data to record the moment when the data was detected. Programmable time window and channel shielding give the flexibility to choose the time range and channels of interest. The delay of each channel can be calibrated. The data is transmitted to data acquisition system (DAQ) through Gigabit Ethernet. TDC and control logic are configured in real time by DAQ. The results of test show that the Full Width at Half Maximum (FWHM) precision of single channel is better than 273 ps with a low sensitivity to temperature and the linearity is pretty well.

Minioral:

Yes

Description:

FPGA-TDC

Speaker:

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Country:

China

664

595 Fixed latency fiber communication for JLAB's Hall B RICH detector

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595

Fixed latency fiber communication for JLAB's Hall B RICH detector

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A fixed latency Serializer-Deserializer(SerDes) is useful in detector electronics for the synchronization and triggering of data acquisition. It is not a common default feature of FPGA transceiver protocol packaging, but it can be custom built by logic in the FPGA fabric.

In this application we have a Xilinx Virtex-5 FPGA driving several GTP fiber transceivers from cards housed in a VXS crate talking to readout boards local to the detector, each hosting a Xilinx Artix-7. This communication runs a 16 bit bus at 125Mhz with a 2.5Gbps line rate.

The transceiver IP cores available on Xilinx parts utilize elastic buffers for various purposes. In order to achieve a fixed latency these buffers must be removed and replaced with custom firmware protocols for communication and link monitoring.

This custom firmware must ensure a stable link on startup, reset or power cycle, and maintain integrity. This includes clock management, word alignment, loss of sync detection, and initial phase alignment.

Minioral:

Yes

Description:

FPGA SerDes

Speaker:

Cody Dickover

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JLAB

Country:

USA

405

Configurable and Expandable High Speed Trigger Supervisor for Imaging Data Acquisition System.

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The FPGA based Trigger Supervisor for the JLab Imaging Data Acquisition (DAQ) system provides a high speed connection for a number of data acquisition (DAQ) instruments. An example of a DAQ instrument is the JLab Ethernet 250 MHz 16 channel Flash Analog to Digital Converter (EFADC16) which is the basis of a recently submitted JLab patent application. The Trigger Supervisor is composed of a novel arrangement of hardware and software structures to arrive at a high performance DAQ system. It can accommodate a system of a single DAQ instrument to a complex system composed of many DAQ instruments. Each individual instrument of the complex system can be located up to hundreds of feet apart. The functionality and operation of the Trigger Supervisor are both fully programmable. The DAQ system can be seamlessly expanded to accommodate more DAQ instruments as required. The cost is directly proportional to the complexity of the system.

Minioral:

No

Description:

Trigger supervisor

Speaker:

Hai Dong

Institute:

JLAB

Country:

USA

479

A PXI-based, Multi-channel Ultra-fast Data Acquisition System for Transient Pulsed Signal

Authors: Yafei Du[1]; Jun Wu[2]; Chen Yuan[2]

Co-authors: Haohan Yang ; Faqiang Zhang

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We design a high speed, high resolution data acquisition system(DAS) with 1Gsps sampling rate and 12-bit resolution, mainly applying to nuclear and particle physics experiments. The system consists of two PXIe-1084 chassis, each containing a controller card and 16 data acquisition cards at most. For every single card, the signal conditioning module incorporates one high precision Op Amps converting single-ended signals to differential signals(LVDS) with low additional noise level, and the data acquisition module combines a 12-bit folding interpolating ADC with a Xilinx Kintex-7 FPGA, implementing controls of A/D conversion and high speed data transmission through SFP interface using aurora protocol. All these cards of each chassis can be synchronized easily using timing and triggering with PXI resources. Besides, a simple software of our system is designed to display the captured waveform signal and communicate with the host PC for remote controlling. After careful calibration, primary measurements show that the digitizer achieves an analog bandwidth of higher than 250MHz and an ENOB of more than 9 bit at 1Gsps sampling rate. Due to such high speed and resolution, the system gain more ability to rapidly and precisely extract maximum information from radiation signals. Besides, with great scalability, the system can be used for modern big physics experiments. In addition, high speed data transmission is also an important key feature of our DAS.

Minioral:

Yes

Description:

1Gsps board

Speaker:

Yafei Du

Institute:

Tsinghua

Country:

China

521

Pixel Detector System for Pencil Beam Scanning Proton Therapy

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At the Paul Scherrer Institue (PSI) the Center for Proton Therapy operates 3 different Gantries for patient treatment using Pencil Beam Scanning (PBS) technology. To verify the quality of our PBS beam a new Pixel Detector based on simple and inexpensive printed circuit board (PCB) technology was developed.
The physical detector principle is an ionization chamber and has an active sensor area of 12x12 cm2 covered with 3600 pixels with a size of 2x2 mm2 each. On the readout side we are limited to 256 channels. To fill the gap between 3600 pixel and 256 signal channels we make use of the fact that with PBS only a small part of the detector area is irradiated at a time. With a PCB layout based on channel multiplexing, it was possible to keep the number of required readout channels below the given limit, while still reaching a reasonable measurement resolution.
The readout board itself is a PSI development as well. The core component is the ADAS1128 chip from ANALOG Devices featuring 128 input channels and a digital control interface for gain calibration, offset correction and current range adaptation. The Pixel Detector is highly integrated into the therapy control system through an FPGA based interface and allows detector readout highly synchronized with the beam delivery.
With the first prototype we performed measurements with proton beam and spot scanning technology. The PBS 2D-beamprofile could be reconstructed for all energies from 70 to 230 MeV at each position of the 12x12 cm2 detector area.

Minioral:

Yes

Description:

Pixel Detector

Speaker:

Michael Eichin

Institute:

PSI

Country:

Switzerland

609

Real-time Data Sharing Comparisons Between NSTX-U, DIII-D, and KSTAR

Authors: Keith Erickson[1]; M.D. Boyer[1]

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As Plasma Control Systems (PCS) grow beyond the resource constraints of single, monolithic computers, the need similarly increases for real-time communication between physical computers. Three experiments sharing a common baseline framework (the General Atomics (GA) PCS) approach the situation with similar high level concepts manifested through different lower level implementations. NSTX-U is building a native PCIe interconnect solution based on Dolphin products. DIII-D recently upgraded to an Infiniband solution. KSTAR is currently using a reflective memory infrastructure. These three approaches have differing characteristics and tradeoffs that affect the real-time system determinism, latency, and overall capability. They similarly have different implementation requirements and difficulties that affect scalability and flexibility of the resulting real-time systems. The Princeton University Plasma Physics Laboratory (PPPL) has gained experience working with these various implementations, and has developed a detailed analysis of appropriate use cases and considerations that affect real-time system design decisions. Additionally, the laboratory is supporting efforts to create real-time safe abstractions on top of the underlying architectures to establish a dynamic set of communication layer features adaptable to the limitations of the enabling technology.

Minioral:

Yes

Description:

Speaker:

Keith Erickson

Institute:

Princeton University

Country:

USA

715

609 Real-time Data Sharing Comparisons Between NSTX-U, DIII-D, and KSTAR

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587

A multi-channel digitizer board for the BDX experiment

Authors: Ameli Fabrizio[1]; Battaglieri Marco[2]; Andrea Celentano[2]

Co-authors: Manlio Capodiferro [1]; Tommaso Chiarusi [3]; Giacomo Chiodi [1]; Lorenzo Marsicano [2]; Paolo Musico [2]; Carlo Alessandro Nicolau [1]; Carmelo Pellegrino [3]; Luigi Recchia [1]; Daniele Ruggieri [1]; Lorena Stellato [1]

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Due to the lack of results by 'traditional'Dark Matter (DM) searches, the experimental activity extended to search for DM hints at different mass scales, through new experiments performed at accelerators. The Beam Dump eXperiment at Jefferson Laboratory aims to reveal dark matter particles produced in the interaction of an intense electron beam with the beam dump.
The electronic board presented in this work is a 12-channel digitizer oriented to High Energy Physics experiments. The main features are a low cost per channel, compared to equivalent boards, a flexible and high performance timing system, an adequate memory buffer, a versatile front-end circuitry applicable to different sensors, self-triggering algorithms based on waveform analysis.
The board is based on dual ADCs from Texas Instruments; the ADC family members are pin to pin compatible and allow a choice of 12 or 14 resolution bits and maximum sampling frequencies of 250 MHz. Front end sensors can be powered by the board itself with a regulated voltage up to 100 V.
The board accepts clock and timing signals for alignement to a common reference (typically a GPS receiver), relying on a PLL to reduce the input clock jitter. A WhiteRabbit optical interface is also present, as an alternative way to distribute timing.
Data collection and manipulation is accomplished by a commercial System-on-Module mezzanine board based on a Zynq7045 FPGA.
Waveforms passing a programmable threshold are timestamped and forwarded to DAQ for trigger application and event search. DAQ is effectively scalable according to channels number.

Minioral:

Yes

Description:

DAQ board

Speaker:

Ameli Fabrizio

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INFN

Country:

Italy

634

470 Single photon source driver designed in ASIC

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470

Single photon source driver designed in ASIC

Author: Bo Feng[1]

Co-authors: Futian Liang [1]; Xinzhe Wang [1]; Chenxi Zhu [1]; Yulong Zhu [1]; Ge Jin [2]

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Single photon source is an important part of quantum key distribution (QKD) system. In current, single photon source in QKD system is large in size and complex in structure. And the miniaturization of source is the development trend of QKD system. We integrate laser driver electronic module into one single ASIC chip, which can be used to drive the laser and we can greatly reduce the volume of the single photon source.
We present the design and simulation of our laser driver chip in the paper. The chip is fabricated in a 130 nm CMOS process. The main components of the chip are a pulse generator and a current driver module. The pulse generator is used to provide a pulse-width-adjustable drive signal by a delay line. The current driver module is used to produce an amplitude-adjustable current signal. The chip can produce a current signal with adjustable pulse width and amplitude. The range of pulse width is from 400ps to 4ns, and the range of amplitude is from 20mA to 120mA. The pulse width and amplitude of current signal is configured by a SPI bus.
The chip with a very small size can generate a current pulse signal of which the amplitude is up to 120mA and the pulse width is from 400ps to 4ns. It can meet the needs of the laser we used. Meanwhile, the design of the laser driver chip provides a direction for miniaturization of the whole QKD system.

Minioral:

Yes

Description:

single photon

Speaker:

Bo Feng

Institute:

USTC

Country:

China

667

389 Design of a Non-vacuum-cooling compact scientific CCD camera

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389

Design of a Non-vacuum-cooling compact scientific CCD camera

Author: Yi Feng[None]

Co-authors: Cheng Chen ; Dong-xu Yang ; Guang-yu Zhang ; Hong-fei Zhang ; Jian Wang ; Jian-min Wang ; Jin-ting Chen ; Yi Zhang ; Yi-ling Xu

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CCD was born in Bell Laboratories in 1969 and has been widely used in various fields. Its ultra-low noise and high quantum efficiency make it work well in particle physics, high energy physics, nuclear physics and astrophysics. Nowadays, more and more CCD cameras have been developed for medical diagnosis, scientific experiments, aerospace, military exploration and other fields. For the wide range of CCD cameras, a Non-vacuum-cooling compact scientific CCD camera has been developed, including FPGA-based low noise clock and bias driver circuit, data acquisition circuit, STM32-based temperature control design. At the same time, the readout noise of the imaging system is studied emphatically. The scheme to generate the CCD clock and the bias driving circuit through ultralow noise LDOs is proposed. The camera was tested in a variety of environments, and the test results show that the system can read at a maximum rate of 5M pixels/s and readout noise is as low as 9.29eˆ- when the CCD readout speed is 500K pixels/s. Finally, a series of stability tests were carried out on the camera system. The test showed that the system could work stably.

Minioral:

Yes

Description:

HW DAQ

Speaker:

Yi Feng

Institute:

USTC

Country:

China

395

A Driver ASIC for Scientific CCD Detectors Using 180nm Technology

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In order to implement the driver function for several types of scientific CCD detector, decreasing the size of electronics of CCD detector system, an ASIC chip of CCD driver is designed. It provides multi-channel clocks and bias voltage, called BCDA (Bias Clock Driver ASIC). In the BCDA chip, clock drivers and bias drivers have different designs.
For the different level requirements of bias voltage, two bias drivers are designed: one is to use low-voltage MOS transistors to design the bias voltage which is less than 5V; another is to use the high-voltage LDMOS transistors to design the bias voltage which is great than 5V. The high-voltage bias has the design with 8-bit current DAC and operational amplifier. The adjustable output range is from 8V to 30v.

A clock switch using rail-to-rail operations with the output range from 0V to 16V is designed to generate the clocks. Two different 8-bit current DACs are used to adjust the driver capability of clocks and the upper rail's voltage of clocks. And two clock drivers with driving capability of different orders of magnitude are designed.
The design of the chip has been finished using the Global Foundry 180nm BCDlite technology and taken into tape-out. During the conference, we will report the detail design and final test result.

Minioral:

Yes

Description:

Speaker:

Yi Feng

Institute:

USTC

Country:

China

394

A Time-to-Digital Converter Based on DLL Using 180nm Technology

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Co-authors: Dong-xu Yang ; Guang-yu Zhang ; Jie Gao ; Hong-fei Zhang ; Jian Wang

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Time measurement is the basic measurement requirement in high-energy physics experiment and also one of the two basic measurement (time measurement and energy measurement) in nuclear electronics. Time measurement in nuclear physics and particle physics experiments is mainly for high-precision measurement of short time intervals, while time-to-digital converters (TDCs) are the central components of time measurement. Now, most designs of TDC system rely on FPGAs to achieve high accuracy at the expense of resources, with large DNL and INL errors. In this paper, we use 180nm technology to achieve a TDC based on DLL with a combination of digital and analog processes. The measurement range of this TDC is 0 to 1.19us and the measurement accuracy is 150ps. The TDC includes a DLL-based delay-line with 150ps delay cell, a phase detector with 4ps discrimination, a charge pump with a minimum current of 1uA, a low-pass filter of 8.5pF and a digital encoder. We use DLL technology to solve the problem of delay time with temperature changes perfectly. At the same time, we have simulated TDC under different corners. The simulation shows that the differential nonlinear (DNL) error of delay-line is less than 0.033LSB and the integral nonlinearity (INL) error is less than 0.041LSB under typical corner. The design have been taken into tape-out, and we will report the test results in the conference.

Minioral:

Yes

Description:

FPGA TDC

Speaker:

Yi Feng

Institute:

USTC

Country:

China

512

FPGA code for the data acquisition and real-time processing prototype of the ITER Radial Neutron Camera

Authors: Ana Fernandes[1]; Rita Pereira[1]; Nuno Cruz[1]; Bruno Santos[1]; Paulo Carvalho[1]; Jorge Sousa[1]; Bruno Gonçalves[1]; Marco Riva[2]; Fabio Pollastrone[3]; Cristina Centioli[3]; Daniele Marocco [3]; Basilio Esposito[2]; Carlos Correia[4]; Benoit Brichard[5]

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[2] *ENEA*

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The main role of the ITER Radial Neutron Camera (RNC) diagnostic is to measure in Real-Time (RT) the plasma neutron emissivity profile at high peak count rates for a time duration up to 500 s. Due to the unprecedented high performance conditions and after the identification of critical problems, a set of activities have been selected, focused on the development of high priority prototypes, capable to deliver answers to those problems before the final RNC design. This paper presents one of the selected activities: the design, development and testing of a dedicated FPGA code for the RNC Data Acquisition prototype. The FPGA code aims to acquire, process and store in RT the neutron and gamma pulses from the detectors located in collimated lines of sight viewing a poloidal plasma section from the ITER Equatorial Port Plug #1. The hardware platform used was an evaluation board from Xilinx (KC705) carrying an IPFN FPGA Mezzanine Card (FMC-AD2-1600) with 2 digitizer channels of 12-bit resolution sampling up to 1.6 GSamples/s. The code performs the proper input signal conditioning using a down-sampled configuration to 400 MSamples/s, apply dedicated algorithms for pulse detection, filtering and pileup detection, and includes two distinct data paths operating simultaneously: i) the event-based data-path for pulse storage; and ii) the RT processing, with dedicated algorithms for pulse shape discrimination and pulse height spectra. For continuous data throughput both data-paths are streamed to the host through two distinct PCIe x8 Direct Memory Access (DMA) channels.

Minioral:

Yes

Description:

Neutron camera

Speaker:

Ana Fernandes

Institute:

IPFN

Country:

Portugal

607

Significant acceleration of development by automating quality assurance of a medical particle accelerator safety system using a formal language driven test stand

Authors: Michael Eichin[1]; Alexandre Mayor[None]; Harald Regele[2]; Martin Grossmann[None]; Damien Charles Weber[2]; Pablo Fernandez Carmona[2]

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[2] *Paul Scherrer Institut*

Corresponding Author: pablo.fernandez@psi.ch

At the Centre for Proton Therapy at the Paul Scherrer Institute cancer patients are treated with a fixed beamline and in two gantries for ocular and non-ocular malignancies, respectively. For the installation of a third gantry a new patient safety system (PaSS) was developed and is sequentially being rolled out to update the existing areas. The aim of PaSS is to interrupt the treatment whenever any sub-system detects a hazardous condition. To ensure correct treatment delivery, this system needs to be thoroughly tested as part of the regular quality assurance (QA) protocols as well as after any upgrade. In the legacy safety systems, unit testing required an extensive use of resources: two weeks per area in the laboratory in addition to QA beam time. In order to significantly reduce the time, an automated PaSS test stand for unit testing was developed based on a PXI chassis with virtually unlimited IOs that are synchronously stimulated or sampled at 1 MHz. It can emulate the rest of the facility using adapters to connect each type of interface. With it PaSS can be tested under arbitrary conditions. A VHDL-based formal language was developed to describe stimuli, expected behaviour and specific measurements, interpreted by a LabView runtime environment. This article describes the tools and methodology being applied for unit testing and QA release tests for the new PaSS. It shows how automation and formalization made possible an increase in test coverage while significantly cutting down the lab testing time and facility's beam usage.

Minioral:

Yes

Description:

Speaker:

Institute:

Country:

714

607 Significant acceleration of development by automating quality assurance of a medical particle accelerator safety system using a formal language driven test stand

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707

578 The Fermilab Test Beam Facility Data Acquisition System

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578

The Fermilab Test Beam Facility Data Acquisition System

Authors: Kurt Biery[1]; Eric Flumerfelt[2]; Adam Lyon[3]; Ronald Rechenmacher[1]; Ryan Allen Rivera[1]; Mandy Rominsky[3]; Lorenzo Uplegger[3]; Margaret Votava[2]

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The Real-Time Systems Engineering Department of the Scientific Computing Division at Fermilab has deployed set of customizations to our Off-The-Shelf DAQ solution (otsdaq) at the Fermilab Test Beam Facility (FTBF) to read out the beamline instrumentation in support of FTBF users. In addition to reading out several detectors which use various detection technologies and readout hardware, the FTBF Data Acquisition system (DAQ) can perform basic track reconstruction through the facility in real time and provide data to facility users. An advanced prototype coincidence module, NIM+, performs trigger distribution and throttling, allowing the beamline instrumentation to be read out at different rates. Spill data is saved to disk for studies of the facility performance, and hit data are also made available on the FTBF network for experiments'use. A web-based run control and configuration GUI are provided, and the online monitoring snapshots created after each beam spill are viewable from any computer connected to the Fermilab network. The integrated DAQ system for the facility provides users with tracking data along the beamline and a single location for obtaining data from the facility detectors, which set the baseline for qualifying their own detectors.

Minioral:

Yes

Description:

DAQ

Speaker:

Eric Flumerfelt

Institute:

FNAL

Country:

USA

577

Flexible and Scalable Data-Acquisition Using the artdaq Toolkit

Authors: Kurt Biery[1]; Eric Flumerfelt[2]; John Freeman[2]; Wesley Ketchum[2]; Gennadiy Lukhanin[1]; Adam Lyon[3]; Ronald Rechenmacher[1]; Ryan Allen Rivera[1]; Lorenzo Uplegger[3]; Margaret Votava[2]

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The Real-Time Systems Engineering Department of the Scientific Computing Division at Fermilab is developing a flexible, scalable, and powerful data-acquisition (DAQ) toolkit which serves the needs of experiments from bench-top hardware tests to large high-energy physics experiments. The toolkit provides data transport and event building capabilities with the option for experimenters to inject art analysis code at key points in the DAQ for filtering or monitoring. The toolkit also provides configuration management, run control, and low-level hardware communication utilities. Firmware blocks for several common data acquisition boards are provided, allowing experimenters to approach the DAQ from a higher level. A fully-functional DAQ "solution"of the toolkit is provided in otsdaq, sacrificing some flexibility in favor of being ready-to-use. artdaq is being used for several current and upcoming experiments, and will continue to be refined and expanded for use in the next generation of neutrino and muon experiments.

Minioral:

Yes

Description:

ArtDAQ

Speaker:

Eric Flumerfelt

Institute:

FNAL

Country:

USA

598

The WaveDAQ integrated Trigger and Data Acquisition System for the MEG II experiment

Author: Marco Francesconi[1]

Co-authors: Luca Galli [2]; Ueli Hartmann [3]; Fabio Morsani [4]; Donato Nicolò [5]; Stefan Ritt [6]; Elmar Schmid [3]

[1] *University and INFN of Pisa*

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[3] *PSI*

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The MEG II experiment at Paul Scherrer Institut aims at a sensitivity improvement on $\mu^+ \to e^+\gamma$ decay by an order of magnitude with respect to the former MEG experiment while keeping the same detection strategy. This is possible thanks to an higher segmentation of all detectors, which improves the resolutions and helps coping with twice muon stopping rate, mandatory to collect the required amount of statistics in three years.

The new WaveDAQ integrated Trigger and DAQ system has been developed to fit within the experiment upgrade, pushing further the performances of the DRS4 Switched Capacitor Digitizer allowing of GigaSample digitization of all the ˜9000 channels in a ad-hoc designed crate system.
The system design is highly scalable and can cover the TDAQ needs ranging from laboratory tests to medium scale experiments, like MEG II.
Each WaveDAQ input channel can provide biasing for SiPMs applications and a programmable high bandwidth frontend, removing the need of additional hardware; the trigger generation is fully programmable on a multiple-FPGA architecture interconnected by low latency links and capable of computing charge and time based selections in less than 500 ns.

We report the result of the full 1536 channel system demonstrator used in fall 2017 engineering run with the upgraded MEG II detectors, achieving the requested time resolution and stability and showing the possibility of real-time event selection based on charge measurement.

Minioral:

Yes

Description:

Speaker:

Marco Francesconi

Institute:

INFN

Country:

Italy

614

MDSplus - What is it and how did it happen?

Author: Thomas W. Fredian[1]

[1] *MIT*

MDSplus is a data acquisition and analysis system used worldwide predominantly in the fusion research community. It was based on the original system called MDS which was created in 1982 at the Plasma Science and Fusion center at MIT. Development of MDSplus began in 1987 by a collaboration of software developers who were charged with providing a data acquisition system for three new fusion experiments under construction: CMOD at MIT, ZTH at LANL and RFX at Padova, Italy.

The design of MDSplus combined the functionality of MDS with new features suggested by the developers from the other laboratories. The development of MDSplus used a RAD (rapid application development) approach before RAD became a mainstream methodology. MDSplus was implemented and ready for the initial operation of CMOD in 1991. Since that time, many other fusion facilities adopted MDSplus for data acquisition and/or for exporting their data to other sites. Today MDSplus is used around the world for fusion energy research, space exploration and other fields of science and technology. Work on MDSplus continues to enhance its capabilities, support more platforms, and improve its reliability. It is anticipated that MDSplus will continue to provide valuable tools for the fusion energy research community. This paper provides a brief introduction to MDSplus and discusses the history of its design and development.

Minioral:

Description:

Speaker:

Institute:

Country:

490

Real-time non-intrusive depth estimation of buried radioactive wastes based on approximate three-dimensional relative attenuation model

Authors: Ikechukwu Ukaegbu[1]; Kelum Gamage[2]

[1] *Lancaster University, UK*

[2] *Glasgow University*

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Please see the attached abstract and summary document.

Minioral:

No

Description:

radioactive waste

Speaker:

Kelum Gamage

Institute:

Lancaster University

Country:

UK

489

Localised response retrieval from Hamamatsu H9500 for a coded-aperture dual-particle imaging system based on an organic pixelated plastic scintillator (EJ-299-34)

Author: Michal Cieslak[1]

Co-author: Kelum Gamage [2]

[1] *Lancaster University, UK*

[2] *University of Glasgow, UK*

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See the attached abstract and summary.

Minioral:

No

Description:

MAPMT

Speaker:

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708

580 FELIX based readout of the Single-Phase ProtoDUNE detector

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580

FELIX based readout of the Single-Phase ProtoDUNE detector

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Large liquid argon Time Projection Chambers have been adopted for the DUNE experiment's far detector, which will be composed of four 17 kton detectors situated 1.5 km underground at the Sanford Underground Research Facility. This represents a large increase in scale compared to existing experiments. Both single- and dual-phase technologies will be validated at CERN, in cryostats capable of accommo- dating full-size detector modules, and exposed to low-energy charged particle beams. This programme, called ProtoDUNE, also allows for extensive tests of data acquisition strategies. The Front-End LInk eXchange (FELIX) readout system was initially developed within the ATLAS collaboration and is based on custom FPGA-based PCIe I/O cards, connected through point-to-point links to the detector front-end, hosted in commodity servers. FELIX will be used in the single-phase ProtoDUNE setup to read the data coming from 2560 anode wires organized in a single Anode Plane Assembly structure. With a continuous readout at a sampling rate of 2 MHz, the system must deal with an input rate of 96 Gb/s. An external trigger will preselect time windows of 5 ms with interesting activity expected inside the detector. Event building will occur for triggered events, at a target rate of 25 Hz; the readout system will form fragments from the data samples matching the time window, carry out lossless compression, and forward the data to event building nodes over 10 Gb/s Ethernet. This paper discusses the design and implementation of this readout system as well as first operational experience.

Minioral:

Yes

Description:

FELIX (FE Link eXchange)

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445

Lifetime Study of COTS ADC for SBND LAr TPC readout electronics

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Short Baseline Neutrino Detector (SBND), which is a 260-ton LAr TPC as near detector in Shot Baseline Neutrino (SBN) program, consists of 11,264 TPC readout channels. As an enabling technology for noble liquid detectors for neutrino experiments, cold electronics developed for extremely low temperature (77K–89K) decouples the electrode and cryostat design from the readout design. With front-end electronics integrated with detector electrodes, the noise is independent of the fiducial volume and about half as with electronics at room temperature. Digitization and signal multiplexing

to high speed serial links inside cryostat results in large reduction in the quantity of cables (less outgassing) and the number of feed-throughs, therefore minimizes the penetration and simplifies the cryostat design. Being considered as an option for the TPC readout, several Commercial-Off-The-Shelf (COTS) ADC chips have been identified as good candidates for operation in cryogenic temperature after initial screening test. Because of hot-electron effects on CMOS device lifetime, one candidate, ADI AD7274 fabricated in TSMC 350nm CMOS technology, has been used to conduct lifetime study in cryogenic temperature. The lifetime study includes two phases, the exploratory phase and the validation phase. This paper will describe the test method, test setup, observations in exploratory phase, and the lifetime projection that will be concluded with the test results in the validation phase.

Minioral:

Yes

Description:

ADC lifetime

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648

518 FPGA acceleration of Model Predictive Control for ITER Plasma current and shape control

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518

FPGA acceleration of Model Predictive Control for ITER Plasma current and shape control

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A faster implementation of the Quadratic Programming (QP) solver used in the Model Predictive Control scheme for ITER Plasma current and shape control was developed for Xilinx Field-Programmable Gate Array (FPGA) platforms using a high-level synthesis approach. The QP solver is based on the dual Fast Gradient Method (dFGM). The dFGM is essentially an iterative algorithm, where matrix-vector arithmetic operations within the main iteration loop may be parallelized. This type of parallelism is not well-suited to standard multi-core processors because the number of operations to be spread among processing threads is relatively small considering the time-scale of thread scheduling. The FPGA implementation avoids this issue, but it requires specific techniques of code optimization in order to achieve faster solver execution.

Minioral:

Yes

Description:

FPGA control

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703

546 General purpose readout board πLUP: overview and results.

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546

General purpose readout board πLUP: overview and results.

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Co-authors: Alessandro Gabrielli [2]; Gabriele d'Amen [3]; Fabrizio Alfonsi [3]

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This works intends to give an overview of the PCI-Express board πLUP, focusing on the motivation that led to its development, the technological choices adopted and its performance. The πLUP card was designed by INFN and University of Bologna as a possible readout interface to be used after the upgrade of the Pixel Detector of the experiments ATLAS or CMS at LHC. The same team in Bologna also designed and commissioned the ReadOut Driver (ROD) board currently implemented in all the four layers of the ATLAS Pixel Detector (Insertable B-Layer, B-Layer, Layer-1 and Layer-2) and acquired in the past years expertise on the ATLAS readout chain and the problematics arising in such experiments.
Although the πLUP was designed to fulfill a specific task, it is highly versatile and might fit a variety of applications, some of which will be discussed in this work. Two 7th-generation Xilinx FPGAs are mounted on the board: a Zinq-7 with an embedded dual core ARM Processor and a Kintex-7. The latter features sixteen 12.5 Gbps tranceivers, allowing the board to interface easily to any other electronic board, electrically and/or optically, at the current desired bandwidth of the experiments for LHC. Many data-transmission protocols have been tested at different speeds; results will be discussed later in the work.
Two batches of πLUP boards have been fabricated and tested; two boards in the first batch (version 1.0) and four boards in the second batch (version 1.1), encapsulating all the patches required for the first version.

Minioral:

Yes

Description:

PICe piLUP

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Nico Giangiacomi

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INFN

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Italy

520

Configuration Redundancy for Enhanced Reliability in SRAM-based FPGAs

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Digital off-detector electronics in trigger and data acquisition systems of High-Energy Physics experiments is often implemented by means of SRAM-based FPGAs, which make it possible to achieve reconfigurable, real-time processing and multi-gigabit serial data transfers. On-detector usage of such devices is mostly limited by their configuration sensitivity to radiation-induced upsets, which may alter the programmed routing paths and configurable elements.

In this work, we show a new technique for enhancing the usage of SRAM-based FPGAs also for on-detector applications. The proposed technique is capable of protecting the configuration pertaining to basic blocks such as look-up-tables and routing, but it can also address complex hard macros, such as high-speed IO transceivers (e.g. the Xilinx GTX). We show a demonstrator of our solution on benchmark designs, including a triple modular redundant design and a serial link (without redundancy) running at 5 Gbps, implemented in a Xilinx Kintex-7 FPGA.
We performed irradiation tests at Laboratori Nazionali del Sud (Catania, Italy) with a 62-MeV proton beam. The results show that our scrubbing technique made it possible to detect and correct all the radiation-induced upsets after a total fluence higher than $10^{11} cm^{-2}$. For both the redundant benchmark design and the serial link, the correct functionality was always restored after scrubbing the corrupted configuration bits and resetting the circuit. However, the redundant design has shown a significantly lower number of failures with respect to the serial link.

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689

474 The customization of White Rabbit for different applications

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474

The customization of White Rabbit for different applications

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White Rabbit is a new technology that can distributes precise time and frequency among thousands of nodes for long distance. The compatibility with standard Ethernet makes it ideal for applications that requires both precise time/frequency synchronization and bi-directional data exchange. Interests have been expressed to apply this technology in different fields, which also bring their specific requirements to customize or intergrade the WR technology that cannot be satisfied by the general solution provided by the WR developers. In this paper, we describe several projects that intergrade WR, the application and specific design of the WR related part will be given.

Minioral:

Yes

Description:

White Rabbit

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China

641

492 OpenCL implementation of an adaptive disruption predictor based on a probabilistic Venn classifier

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492

OpenCL implementation of an adaptive disruption predictor based on a probabilistic Venn classifier

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The ability and flexibility of the Open Computing Language (OpenCL) for task parallelization in heterogeneous computing platforms (FPGA, CPU, GPU) represent a remarkable advantage when designing advanced data acquisition and processing systems. This work shows a specific implementation of an adaptive probabilistic disruption predictor for fusion devices. This implementation uses OpenCL as base technology for the design cycle. The system was realized in two different platforms. The first one is an FPGA-based architecture that comprises a Cyclone V SoC in a DE1SoC development board. The second one is a GPU-based architecture that contains an AMDFireProW4300 inserted into a computer running Scientific Linux as Operating System. This contribution presents the methodology, the hardware/software system architecture, and the implementation results in both hardware platforms. The work is focused on the critical aspects involved in the design of these intelligent data acquisition and processing systems with OpenCL. When dealing with this technology, it is essential to be aware of aspects such as the significant differences in the design flow concept between FPGA and GPU implementations, or how to select the part of the algorithm that is better to be executed in each platform, which is not an easy task. The work addresses aspects such as how to optimize the pipelines in the FPGA implementation or how to arrange the work items in the GPU implementation to obtain the best performance. The test results show that it is possible to achieve prediction times shorter than 500 us with both solutions.

Minioral:

Yes

Description:

computing parallelization

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Country:

Spain

610

Dummy - pls ignore

Author: Martin Grossmann GMAIL[1]

[1] *Paul Scherrer Institute*

Compact portable 16k Digital MCA
Suited for high resolution Gamma Spectroscopy
Support continuous and pulsed reset preamplifiers
Software selectable coarse and fine gain
DB9 connector for preamplifier power supply
Features Pulse Height Analysis firmware for energy calculation
Different acquisition modes available: PHA and signal inspector for an easy setup and signal monitoring
USB and Ethernet communication interfaces
Supported by MC2Analyzer software GUI for configuration, acquisition, and data plotting

Minioral:

Yes

Description:

Speaker:

Institute:

Country:

716

Test for SOFE

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fdsöjhfdsalkjhfdsalkjhlkh

Minioral:

Yes

Description:

Speaker:

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Country:

695

522 Cavity Simulator for European Spallation Source

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522

Cavity Simulator for European Spallation Source

Author: Maciek Grzegrzółka[1]

Co-authors: Mateusz Lipinski [2]; Igor Rutkowski [3]; Krzysztof Czuba [4]

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European Spallation Source will be the brightest neutron source in the world. It is being built in Lund, Sweden. Over 120 superconducting cavities will be installed in the facility, each regulated by an individual LLRF control system. To reduce the risk of testing the systems on real cavities a Cavity Simulator was designed. It reproduces the behaviour of superconducting cavities used in the medium and high beta sections of ESS's Linac. The high power RF amplifier and piezo actuators parameters are also simulated.
Based on the RF drive and piezo control signals the Cavity Simulator generates the RF signals acquired by the inputs of the LLRF control system. This is used to close the LLRF feedback loop in real time. The RF front end of the Cavity Simulator consists of vector modulators, down-converting circuits, and a set of fast data converters. The cavity response simulation is performed in a high speed FPGA logic by a dedicated firmware, that was optimized to minimize the processing time. The device also generates clock, LO, and the 704.42 MHz reference signals to allow for system tests outside of the accelerator environment.
In this paper the design of the Cavity Simulator, description of the algorithms used in the firmware, and measurement results of the device are presented.

Minioral:

Yes

Description:

cavity simulation

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589

Real-Time Redundancy for the 1.3 GHz Master Oscillator of the European-XFEL

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Many modern large-scale facilities, like European X-ray Free Electron Laser (E-XFEL), require precise synchronisation, often down to femtosecond level. Even a very short interruption or an excessive glitch in the reference signal might break the precise time relations between subsystems. In such event, a time-consuming resynchronization process is required that renders the facility not available for the users until it is completed. Therefore, such events are highly undesirable.

In this paper, we present an autonomous redundancy solution for the European-XFEL's master oscillator that will guarantee a continuous delivery of the high-quality reference signal even in case of most of the potential failures. The concept and implementation are presented, as well as results from testing in the laboratory environment.

Minioral:

Yes

Description:

RT oscillator

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460

Network Time Synchronization of the Readout Electronics for a New Radioactive Gas Detection System

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In systems with multiple radiation detectors, time synchronization of the data collected from different detectors is essential to reconstruct multi-detector events such as scattering and coincidences. In cases where the number of detectors exceeds the readout channels in a single data acquisition electronics module, multiple modules have to be synchronized, which is traditionally accomplished by distributing clocks and triggers via dedicated connections.
To eliminate this added cabling complexity in the case of a new radioactive gas detection system prototype under development at the French Atomic Energy Commission (CEA), we implemented time synchronization between multiple XIA Pixie-Net detector readout modules through the existing Ethernet network, based on the IEEE 1588 precision time protocol. The detector system is dedicated to the measurement of radioactive gases at low activity and consists of eight large silicon pixels and two NaI(Tl) detectors, instrumented with a total of three 4-channel Pixie-Net modules. Detecting NaI (Tl)/silicon coincidences will make it possible to identify each radioisotope present in the sample. To allow these identifications at low activities, the Pixie-Net modules must be synchronized to a precision well below the targeted coincidence window of 500-1000 ns. Being equipped with a 1588 compatible Ethernet PHY that outputs a locally generated but system-wide synchronized clock, the Pixie-Net can operate its analog to digital converters and digital processing circuitry with that

clock and match time stamps for captured data across the three modules. Depending on the network configuration, the implementation is capable to achieve timing precisions between 300 ns and 200 ps.

Minioral:

No

Description:

Net Time sync

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613

General Challenges in Data Acquisition and Computing for the Proposed Electron Ion Collider (EIC)

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Description:

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Country:

673

416 A new all-digital background calibration technique for time-interleaved ADC using first order approximation FIR filters

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416

A new all-digital background calibration technique for time-interleaved ADC using first order approximation FIR filters

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This paper describes a new all-digital technique for calibration of the mismatches in time-interleaved analog-to-digital converters (TIADCs) to reduce the circuit area. The proposed technique employ first order approximation FIR filter banks, which do not need large number of FIR taps. In case of a four-channel 12-bit TIADC, the proposed technique improves SINAD of simulated data from 54dB to 61dB, and improves SINAD of measured data from 49dB to 53dB, while the number of FIR taps is only 31. In the case of slight mismatches, 22-bit FIR coefficient is sufficient to correct 12-bit signals, which makes it easy to implement this technique in hardware. In addition, this technique is not limited by the number of sub-ADC channels and is also suitable for wideband signals.

Minioral:

Yes

Description:

calibration algo

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China

693

511 A novel real-time radiation detector readout and acquisition system for PET

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511

A novel real-time radiation detector readout and acquisition system for PET

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The objective of this study is to develop a real-time multi-channel detector readout and data acquisition system for a compact silicon photomultiplier based Positron Emission Tomography (PET) scanner for preclinical radiotherapy. Without using ASIC, the system consists of simple op-aps and FPGAs and apply novel 1-bit sigma-delta modulation (SDM) method to have most circuit functions of signal conditioning, ADC, TDC, and monitoring of noise and semiconductor photon sensor's status be performed by FPGA. We aim to provide ASIC-equivalent performance and compact size, but with advantages of much lower cost, easier to implement, more flexible to change the configuration and functionality by programming for different detector characteristics or operating needs, and capable to continuously monitor the signal and sensor status during the operation. Specifically, analog signals from silicon photomultipliers will be read out and processed by a detector-level board to provide digitized output signals containing detected energy, timing and positioning information; each board can read out two 32-channel detectors with one onboard low-cost FPGA; total 24 detector-level boards will be linked and synchronized with a system-level FPGA board for PET data acquisition that includes event selection, data transfer and system control, etc. Preliminary study based on a 16-ch prototype detector-level board has demonstrated the design feasibility and shown promising results of circuit signal performance and initial radiation detector measurement. A DAQ system with multiple detector-level boards for PET coincidence data acquisition and imaging study is under development and will be reported at the conference.

Minioral:

Yes

Description:

MPPC

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515

Accurate Synchronization of Multichannel Acquisition for Field Digitizer Modules at CSNS-WNS

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The under-construction White Neutron Source at China Spallation Neutron Source (so-called Back-n) is a facility for nuclear data measurements which has planned seven spectrometers. As the differ-

ent of physical objectives, the requirements for readout electronics of each spectrometer differs from each other. To accommodate the variety of detectors, the general-purpose readout electronics with a unified structure has been proposed and applied to all spectrometers at Back-n, in which a field digitizer module (FDM) with two digitizing channels has been designed to obtain the full waveform data. In this paper, an accurate synchronous acquisition approach for multi FDMs is introduced. The trigger and clock module (TCM) in the general-purpose readout electronics synchronously fans out clock (125MHz) and trigger signals to each FDM channel separately through the dedicated differential star buses on the PXIe backplane. In FDM, a dual-loop PLL referenced by this synchronous clock generates a higher frequency clock (1GHz) as the digitizer sampling clock. After being divided by the sampling clock, the digitizer data clock (250MHz) is fed into a field programmable gate array (FPGA) for high speed data receiving and further as the global clock for FPGA firmware. To compensate the sampling offset caused by the skew discrepancy of digitizer clock, a FPGA-based TDC is implemented to accurately measure the time interval between the rising edge of global clock received at the FPGA and the global synchronous trigger signal. Test result shows that the synchronization performance of the multi-channel acquisition meets requirements.

Minioral:

No

Description:

DAQ board

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413

Design of a general purpose scalable DAQ system

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In nuclear detection and high energy physics experimentations, large amount of detectors are widely used, proposing great challenges to the data acquisition (DAQ) system in timing, trigger and high speed data transmission. A new general purpose DAQ system with high integration and scalability is being designed. Multiple boards are connected serially via bidirectional optical links at the line rate of 4.8 Gbps, which transmit trigger, data and control signals simultaneously. With the employment of GBT protocol, fixed latency can be achieved between the boards. The propagation delay along the serial link is computed automatically in the FPGA reaching the accuracy of nanosecond level in preliminary tests. The whole system is given high flexibility and universality under the design concept of separating general-used hardware from application specified parts. Each node is consisted of a carrier board and up to four dedicated mezzanine cards. Until now, the DAQ system with 12-bit 80MHz ADCs (64 channels on one board) has been developed and tested.

Minioral:

No

Description:

system

Speaker:

Yuyan Huang

Institute:

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Country:

China

563

Trigger Merging Module for J-PARC E16 Experiment

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Co-authors: Eitaro Hamada [2]; Hiroshi Sendai [2]; Kazuki Suzuki [1]; Kazuya Aoki [2]; Kyoichiro Ozawa [2]; Masahiro Ikeno [2]; Mashin Tanaka [2]; Megumi Naruki [1]; Ryotaro Honda [3]; Sakiko Ashikaga [1]; Satoshi Yokkaichi [4]; Tomohisa Uchida [2]; Tomonori Takahashi [5]; Youichi IGARASHI [2]

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An experiment to measure the spectral modification of vector mesons in nuclear medium is planned as the J-PARC E16. It will start at a J-PARC high momentum beam line in FY 2019. The number of total detector channels is 112,996.
The trigger decision is made from 2,620 ch discriminator output signals. The number is too large to handle with one module, therefore we have developed a new trigger merger board.
The trigger system consists of trigger merging modules, a trigger decision module and trigger distributing modules. The trigger merging module is named as TRG-MRG. For trigger decision and trigger distributing modules, the Belle-2 UT3 and Belle-2 FTSW are used, respectively. We have developed a merging module named TRG-MRG.
The TRG-MRG mainly consists of 256ch LVDS receivers, FPGA (Kintex7 160T-2) and 8ch optical transceivers (SFP+). The module detects leading edges of 256ch LVDS signals from discriminators at 500 MHz double data rate and outputs serialized timing data to the Belle-2 UT3 by Aurora 8B/10B protocol.
The detail of development and results of performance test of TRG-MRG will be presented.

Minioral:

Yes

Description:

Trigger

Speaker:

Masaya Ichikawa

Institute:

Kyoto University

Country:

Japan

652

534 Initial performance of Belle II High Level Trigger and Back End Processing in the Beam Commissioning

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Initial performance of Belle II High Level Trigger and Back End Processing in the Beam Commissioning

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The Belle II experiment, a new generation B-factory experiment, is about to start data taking from April this year. The data acquisition system (DAQ) is now ready and waiting for the beam commissioning.

The data are processed by the High Level Trigger(HLT) equipped with 1600 cores. A high granurality parallel processing is performed to keep up with the L1 trigger up to 30kHz with a typical event size of 100kB. A full event reconstruction is performed on HLT for the software trigger, and also the track information is fed back to the pixel readout to reduce the data size down to 1/10 by the matching with the track. The data are merged with the HLT output and stored in high speed RAID arrays. The merged data are also fed into a PC cluster called ExpressReco at a reduced rate for the monitoring purpose. ExpressReco is equipped with 160 cores for the fine event reconstruction with the pixel data and the detailed data monitoring is performed. The beam colliding position is obtained and is fed back to the accelerator.

This contribution reports the initial performance of HLT and ExpressReco in the beam commissioning, together with the various experience on the whole Belle II DAQ system during the commisioning period.

Minioral:

Yes

Description:

backend processing

Speaker:

Ryosuke ITOH

Institute:

KEK

Country:

Japan

462

T0 Fanout for Back-n White Neutron Facility at CSNS

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The main physics goal for Back-n white neutron facility at China Spallation Neutron Source (CSNS) is to measure nuclear data. The energy of neutrons is one of the most important parameters for measuring nuclear data. Method of time of flight (TOF) is used to obtain the energy of neutrons. The time when proton bunches hit the thick tungsten target is considered as the start point of TOF. T0 signal, generated from the CSNS accelerator, represents this start time. Besides, the T0 signal is also used as the gate control signal that triggers the readout electronics. Obviously, the timing precision of T0 directly affects the measurement precision of TOF and controls the running or readout electronics. In this paper, the T0 fan-out for Back-n white neutron facility at CSNS is proposed. The T0 signal travelling from the CSNS accelerator is fanned out to the two underground experiment stations respectively over long cables. To guarantee the timing precision, T0 signal is conditioned with good signal edge. Furthermore, techniques of signal pre-emphasizing and equalizing are used to improve signal quality after T0 being transmitted over long cables with about 100 m length. Experiments show that the T0 fan-out works well, the T0 signal transmitted over 100 m remains a good time resolution with a standard deviation of 25 ps. It absolutely meets the required accuracy of the measurement of TOF.

Minioral:

No

Description:

beam T0 board

Speaker:

Xuyang Ji

Institute:

USTC

Country:

China

498

Real-time Data Flow Control for CBM-TOF Super Module Quality Evaluation

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Super module assembled with MRPC detectors is the component unit of TOF spectrometer for the Compressed Baryonic Matter (CBM) experiment. Quality of super modules needs to be evaluated before it is applied in CBM-TOF. The maximum data rate is up to 6 Gbps at each sandwich TDC station (STS), which is used to digitize time signal exported from super module. In this paper, a real-time data flow control method is presented for quality evaluation. In this control method, data flow is divided into three types: scientific data flow with digitized time information, status data flow and control data flow. In scientific data flow, data of each STS is divided into 4 sub-flows, and is read out by a distributed network, which consists of multiple readout mother boards (DMBs) and readout daughter boards (DRMs) groups. Each DRM is expected to support Gigabit Ethernet transmission to DAQ at the rate of 400 Mbps. In status data flow, status data is aggregated into a specialized DMB and DRM group via crate backplane, and then is uploaded to DAQ. In control data flow, control data is downloaded to all DMB and DRM groups and STS in the opposite direction of status data flow. Preliminary test result indicates that average transmission capability of single DRM reaches 540 Mbps over the expectation of 400 Mbps. This data flow control method can meet the requirement of CBM-TOF supper module quality evaluation.

Minioral:

No

Description:

RT data flow

Speaker:

Wei Jiang

Institute:

USTC

Country:

China

477

Control and Readout Software in Superconducting Quantum Computing

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High-speed DAC and ADC boards as important parts of quantum computers are used to control and read out the states of qubits, their manipulation complexity is rapidly increasing as the number of qubits boosts. The low efficiency of communication, imperfections of electronic device and the coherent control of the qubits are gradually highlighted, which have become the bottleneck to scale up the qubits. To address the problems, we present a control and readout solution in this study. We adopted the C/S structure and developed two servers called the ADC server and DAC server which enable rapid physical experiments to implement. The DAC server realized waveform processing engine, which can not only mitigate the imperfections of the DAC itself, but also can compensate the transmission loss of circuit. To simplify the coherent control of device, we extract a logical layer for the server with corresponding physical resources and automatically aligned the timing of different channels. A simple data link layer protocol is designed for the high-bandwidth communication with ADC boards. According to the characteristics of low speed soft-core in FPGA, we design a multi-threaded communication mechanism to improve the overall data transmission efficiency of multiple DAC boards. By using these network optimization strategies, both data transmission rate of ADC and DAC boards can reach hundreds of Mbps.

Minioral:

Yes

Description:

ADC/DAC control

Speaker:

Cheng Guo

Institute:

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Country:

China

657

553 Development of Slow Control Package for the Calorimeter Trigger System at the Belle II Experiment

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Development of Slow Control Package for the Calorimeter Trigger System at the Belle II Experiment

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The Belle II experiment at the SuperKEKB e+e- collider in KEK, Japan does start physics data-taking from early of 2018 with primary physics goal that is to probe the New Physics effect using heavy quark and lepton weak decays. During trigger and DAQ operation upon beam collision, it is important that Belle II detector status have to be monitored during data-taking against an unexpected situation. Slow control system, built in the Control System Studio (CSS) which is a GUI window design tool based on Eclipse, is one of monitoring systems in Belle II operation. Database and archiver servers are connected to slow control system. Experimental parameters are downloaded to Belle II main database server which is based on PostgreSQL. Real-time results are stored in archiver server which is based on EPICS(The Experimental Physics and Industrial Control System) archiver appliances and tomcat which is open-source java servlet container. In this study, we report the development of slow control system for the Belle II electromagnetic calorimeter (ECL) trigger system.

Minioral:

Yes

Description:

Slow Control Trigger

Speaker:

Cheolhun Kim

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Korea

636

473 Real time data analysis with the ATLAS trigger at the LHC in Run-2

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630

455 A new high speed, Ultrascale+ based, board for the ATLAS jet calorimeter trigger system

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629

453 The design and performance of the ATLAS Inner Detector trigger in high pileup collisions at 13 TeV at the Large Hadron Collider

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623

425 Overview and performance of the ATLAS Level-1 Topological Trigger

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473

Real time data analysis with the ATLAS trigger at the LHC in Run-2

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The trigger selection capabilities of the ATLAS detector have been significantly enhanced for the LHC Run-2 in order to cope with the higher event rates and with the large number of simultaneous interactions (pile-up) per proton-proton bunch crossing. A new hardware system, designed to analyse real time event-topologies at Level-1 came to full use in 2017. A hardware-based track reconstruction system, expected to be used real-time in 2018, is designed to provide track information to the high-level software trigger at its full input rate. The high-level trigger selections are largely relying on offline-like reconstruction techniques, and in some cases multi-variate analysis methods. Despite the sudden change in LHC operations during the second half of 2017, which caused an increase in pile-up and therefore also in CPU usage of the trigger algorithms, the set of triggers (so called trigger menu) running online has undergone only minor modifications thanks to the robustness and redundancy of the trigger system, and the use of a levelling luminosity scheme in agreement with LHC and other experiments.

This presentation gives a brief yet comprehensive review of the real-time performance of the ATLAS trigger system in 2017. Considerations will be presented on the most relevant parameters of the trigger (efficiency to collect signal, CPU usage and output data rate) as well as details on some aspects of the algorithms which are run real-time on the High Level Trigger CPU farm.

Minioral:

Yes

Description:

RT analysis

Speaker:

ATLAS

Institute:

CERN

Country:

China

455

A new high speed, Ultrascale+ based, board for the ATLAS jet calorimeter trigger system

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To cope with the enhanced luminosity at the Large Hadron Collider (LHC) in 2021, the ATLAS collaboration is planning a major detector upgrade. As a part of this, the Level 1 trigger based on calorimeter data will be upgraded to exploit the fine granularity readout using a new system of Feature EXtractors (FEX), which each reconstruct different physics objects for the trigger selection. The jet FEX (jFEX) system is conceived to provide jet identification (including large area jets) and measurements of global variables within a latency budget of less then 400ns. It consists of 6 modules. A single jFEX module is an ATCA board with 4 large FPGAs of the Xilinx Ultrascale+ family, that can digest a total input data rate of ˜3.6 Tb/s using up to 120 Multi Gigabit Transceiver (MGT), 24 electrical optical devices, board control and power on the mezzanines to allow flexibility in upgrading controls functions and components without affecting the main board. The 24-layers stack-up was carefully designed to preserve the signal integrity in a very densely populated high speed signal board selecting MEGTRON6 as the most suitable PCB material. This contribution reports on the design challenges and the test results of the jFEX prototypes. In particular the fully assembled final prototype has been tested up to 12.8 Gb/s in house and in integrated tests at CERN. The full jFEX system will be produced by the end of 2018 to allow for installation and commissioning to be completed before LHC restarts in March 2021.

Minioral:

Yes

Description:

Trigger, board

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

453

The design and performance of the ATLAS Inner Detector trigger in high pileup collisions at 13 TeV at the Large Hadron Collider

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The design and performance of the ATLAS Inner Detector (ID) trigger algorithms running online on the High Level Trigger (HLT) processor farm for 13 TeV LHC collision data with high pileup are discussed. The HLT ID tracking is a vital component in all physics signatures in the ATLAS Trigger for the precise selection of the rare or interesting events necessary for physics analysis without overwhelming the offline data storage in terms of both size and rate. To cope with the high interaction rates expected in the 13 TeV LHC collisions the ID trigger was redesigned during the 2013-15 long shutdown. The performance of the ID Trigger in both the 2016 and 2017 data from 13 TeV LHC collisions has been excellent and exceeded expectations, even at the very high interaction multiplicities observed at the end of data taking in 2017. The detailed efficiencies and resolutions of the trigger in a wide range of physics signatures are presented for the Run 2 data, illustrating the superb performance of the ID trigger algorithms in these extreme pileup conditions. This demonstrates how the ID tracking continues to lie at the heart of the trigger performance which enables the ATLAS physics program, and will continue to do so in the future.

Minioral:

Yes

Description:

trigger

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

425

Overview and performance of the ATLAS Level-1 Topological Trigger

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In 2017 the LHC provided proton-proton collisions to the ATLAS experiment with high luminosity (up to 2.06x10^34), placing stringent operational and physical requirements on the ATLAS trigger system in order to reduce the 40 MHz collision rate to a manageable event storage rate of 1 kHz, while not rejecting interesting physics events. The Level-1 trigger is the first rate-reducing step in the ATLAS trigger system with an output rate of 100 kHz and decision latency of less than 2.5 μs. An important role is played by its newly commissioned component: the L1 topological trigger (L1Topo). This innovative system consists of two blades designed in AdvancedTCA form factor, mounting four individual state-of-the-art processors, and providing high input bandwidth and low latency

data processing. Up to 128 topological trigger algorithms can be implemented to select interesting events by applying kinematic and angular requirements on electromagnetic clusters, jets, muons and total energy. This results in a significantly improved background event rejection and improved acceptance of physics signal events, despite the increasing luminosity. This is becoming more and more important for analyses making use of low pT objects, like the Heavy Flavour and Higgs physics programme.
In this talk, an overview of the L1Topo architecture, simulation and performance results in physics analyses is presented.

Minioral:

Yes

Description:

system trigger

Speaker:

ATLAS

Institute:

CERN

Country:

Switzerland

532

Application of PROFINET IO in Neutron Scattering Instruments

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The control systems of all neutron scattering instruments implemented by the Jülich Centre for Neutron Science (JCNS) are based on Siemens PLC technology. Historically PROFIBUS has been used for the communication of PLCs with supervisory computers, decentral periphery systems and other PLCs. Today, PROFINET IO is the most commonly used industrial real time Ethernet system and naturally supported by Siemens PLC systems. As a consequence, all new neutron instruments of JCNS are based on PROFINET IO. For the interfacing to supervisory computers based on CPCI, a CPCI carrier board for PC/104-Plus mezzanines has been developed, allowing the transparent use of the Siemens PC/104-Plus PROFINET IO controller CP1604 in CPCI systems. Linux is used as the operating system for supervisory computers access and the software development employs the PROFINET IO-Base-API, commonly supported by Siemens PROFINET IO controllers. On top of this API, an application protocol for the communication with PLC-based motion systems has been implemented.

Minioral:

No

Description:

Profibus

Speaker:

Harald Kleines

Institute:

FZ Juelich

Country:

Germany

528

iFDAQ for the COMPASS experiment

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COMPASS, a fixed target experiment at the Super Proton Synchrotron (SPS) at CERN, developed a new Data Acquisition System (DAQ) using a novel approach to implement the event building network. The system exploits the application-optimized computation technology of Field Programmable Gate Arrays (FPGAs). In contrast to traditional event builders which base on distributed online computers interconnected via an Ethernet network, the building task is executed in hardware. A fast reaction time, higher parallelism of data processing, reduced costs, higher reliability, flexible topology, scalability, and compactness are the advantages of the FPGA-based event builders over the traditional architecture. Since the commissioning in 2014, the system extended and intelligent features were added. In 2017, the system was running with on spill data rate of 1.5 GB/s and achieved uptime of more than 99 percent. This performance is a result of perfect synchronization and intelligent data processing. The computational algorithms resolve inconsistency of data, ensure synchronous event assembly and delivery of consistent information to online computers. The data flow is controlled by throttling mechanism, which protects the system from crashes in case of high event and data rates. The last but not least is a continuous mode of data taking which performs stop and start of runs without downtime.

Minioral:

No

Description:

General DAQ

Speaker:

Igor Konorov

Institute:

TU Muenchen

Country:

Germany

437

A 5.5 ps Time-interval RMS Precision Time-to-Digital Convertor Implemented in Intel Arria 10 FPGA

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As an important part of the field programmable gate array (FPGA) market, Intel FPGA has also great potential for implementation of time-to-digital convertor (TDC). In this paper, the basic tapped delay line (TDL) TDC structure is adapted in Intel Arria 10 FPGA, which is manufactured with 20 nm process technology. Because of the serious bubble problem for FPGA made by state-of-art process, the ones counter encoding scheme is employed to maintain the delay elements in TDL resolvable for achieving high TDC time precision. The test of TDC bin width reveals that the characteristics of the delay chain are highly consistent with the fundamental structure of logic resource in the FPGA. To improve TDC time precision, four TDLs are combined parallel for final TDC implementation. Using two identical TDC channels, the average RMS precision for measurements of time-intervals in the range from 0 to 50 ns reaches 5.45 ps. The test results demonstrate that high performance TDC can be implemented in current Intel main-stream FPGAs as well.

Minioral:

Yes

Description:

FPGA-TDC

Speaker:

Jie Kuang

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USTC

Country:

China

622

422 Real-Time Betatron Tune Correction with the Precise Measurement of Magnet Current

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422

Real-Time Betatron Tune Correction with the Precise Measurement of Magnet Current

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The betatron tune, which is defined as the number of transverse oscillations in one turn of a ring accelerator, must be precisely controlled. This is because particular betatron tunes drastically increase the amplitudes of the oscillations so that many particles are lost from the ring sooner than designed. Since the betatron tune is controlled by the magnetic fields in the ring, the ripple of magnet current regulators directly displaces the betatron tune from its designated value.
We have developed a system which corrects the betatron tune displacement using precisely measured magnet current at the J-PARC Main Ring. Although it is possible to directly measure the betatron tune, the measurement involves the excitation of the betatron oscillation which is not allowed for the user operation. This is the reason that we plan to use magnet current to obtain the betatron tune during the user operation. The current ripple is generally not predictable so that the conversion from the current to the betatron tune must be done in real-time. In the system, the analog measured currents are converted to digital signals at each current regulator. The digitized signals are sent to the current regulator of correction magnets (corrector). At the corrector regulator, a FPGA board are used for the conversion from the current to the betatron tune. We will report the details of the system and some experimental results using the beam.

Minioral:

Yes

Description:

tuning algo

Speaker:

Yoshinori Kurimoto

Institute:

High Energy Accelerator Research Organization

Country:

Japan

449

Development of MicroTCA.4 based remote DAQ system for KSTAR Tokamak

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To standardize and simplify the control system at Korea Superconducting Tokamak Advanced Research (KSTAR), we develop 10G Ethernet based remote DAQ system. By separating the DAQ system and the host, the structure of the control system can be made more flexible. We have developed a DAQ module with a 10G Ethernet interface based on a MicroTCA.4 system designed to control devices in real time on a remote server via 10GE. To connect proposed device and host, we use real time network based on UDP multicast atop 10GbE cut-through packet switching infrastructure. This system is implemented using Zynq based MicroTCA.4 board, matched RTM board that has analogue input/output interface and power supply system. By using remote DAQ system, multiple host server

can subscribe the DAQ data without additional computational cost in real time. This system will be applied to control fueling system at KSTAR Tokamak.

Minioral:

No

Description:

MicroTCA DAQ

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giil kwon

Institute:

NFRI

Country:

Korea

706

559 Reduction Signals Method Preserving Spatial and Temporal Capabilities

561

Characterization of TOF-PET Detectors Based on Monolithic Blocks and an ASIC-Readout

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The aim of this work is to show the potential capabilities of monolithic crystals, coupled to large SiPM arrays to be considered as detector blocks for TOF-PET scanners. Monolithic blocks allow one to decode the 3D photon impact position. This approach, along with TOF capabilities, can be of high interest in clinical PET applications where a typical ring configuration is not used.
In this manuscript, we evaluate an ASIC based readout for digitizing all signals coming from analog photosensors. Validation results with one-to-one coupling resulted in a CTR as good as 200 ps FWHM.

Providing timing resolution when using detectors based on monolithic is however challenging. The wide distribution of scintillation light causes a poor SNR, which makes the system sensible to false triggering and to time walk errors. In this direction, we present a calibration method, designed to correct all recorded timestamps and also to compensate variations in time-paths among channels. Thereafter, a CTR improvement nearing 35% is observed for all measurements. Moreover, we show a novel approach which describes the use of weighted averaging methods to assign the timestamp to each gamma impact. This approach results in a further improvement of the CTR in the range of 100 ps FWHM, reaching a time resolution of 850 ps FWHM using large 50x50x10 mm scintillators coupled to 8x8 SiPM (6x6 mm2) arrays. These pilot studies show detector capabilities regarding TOF information when using monolithic scintillators.

Minioral:

Yes

Description:

ASIC HW

Speaker:

Efthymios Lamprou

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Country:

Spain

559

Reduction Signals Method Preserving Spatial and Temporal Capabilities

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Co-authors: Alfonso Perez ; Antonio J. González ; Edwin J. Pincay ; Efthymios Lamprou ; Filomeno Sánchez ; Gabriel Cañizares ; José Maria Benlloch ; Liczandro Hernández ; Marta Freire ; Sebastian Sánchez ; Victor Ilisie

In this work we show a method to reduce the number of signals to be processed from a detector block for gamma ray imaging. There have been investigations towards reducing the number of signals in order to specially decrease system costs. Anger logic is one of widest used approach, since it reduces the number of photosensor signals to only 4. Other approaches result into two projections, reducing the number of signals to the number of rows and columns in the photosensor array.
We show here a two-steps reduction scheme without degradation of the detector performance. On one step, we merge signals at the center and laterals of the detector block where less sampling is typically required. The goal is to feed the signals into an Application Specific Integrated Circuits (ASIC). Most of them have a number of input channels varying from 16 to 64. The current approach allows one to reduce the 144 signals of an array of 12x12 photosensors to only 64, keeping a good system performance regarding spatial, energy and timing resolution. On a second reduction step, a further reduction is applied by projecting the already reduced signal into X and Y projections. In the particular case of an array of 12x12 photosensors, only 8+8 signals are finally obtained.
We present data to compare the performance of gamma ray detector blocks with and without these reduction methods. We have evaluated spatial, energy and now also timing capabilities. Moreover, we have applied this method to monolithic and crystal arrays.

Minioral:

Yes

Description:

Speaker:

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Country:

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552

Progress on the Electromagnetic Calorimeter Trigger Simulation at the Belle II Experiment

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The Belle II experiment at KEK in Japan start beam collision from early of 2018 to probe a New Physics beyond the Standard Model by measuring CP violation precisely and rare weak decays of beauty, charm quark and tau lepton. The experiment is performed at the SuperKEKB e+e- collider with 80×10ˆ{34}cmˆ{−2}sˆ{−1} as an ultimate instantaneous luminosity. In order to develop and test an appropriate trigger algorithm under much higher luminosity and severe beam background environment than previous KEKB collider, a detail simulation study of the Belle II calorimeter trigger system is very crucial to operate Belle II trigger/DAQ system in stable. We report preliminary results on various trigger logic and efficiencies using physics and beam background events upon the Belle II Geant4-based analysis framework called Basf2.

Minioral:

No

Description:

Trigger Simulation

Speaker:

Insoo Lee

Institute:

Hanyang University

Country:

Korea

687

465 Quality Evaluation Electronics for CBM-TOF Super Module

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465

Quality Evaluation Electronics for CBM-TOF Super Module

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The Time-of-Flight (TOF) system, a spectrometer for charged hadron identification in the Compressed Baryonic Matter (CBM) experiment, is comprised with super modules. Each super module contains several multi-gap Resistive Plate Chambers (MRPCs) and provides up to 320 electronic channels in total for high-precision time measurement. During mass production of the MRPCs, it is necessary and important to do quality control work to ensure that the detectors achieve the targeted performance. In this paper, the electronics based on the PXI platform is proposed for the super module. The time of flight indicated by MRPC signals are digitized and buffered by the Time-to-Digital Converter (TDC). Around the same time, the dedicated trigger decision is generated and distributed to the TDC for selection of the effective time data from the buffer according to the arrival time. Then, the matched time data are transmitted to the TDC readout motherboard (TRM) for aggregation. In the end, the data readout module (DRM) allocated in a 6U PXI chassis exports the merged time data from the TRM though optical links to the data acquisition (DAQ) system through the Ethernet. The laboratory test results show that the quality evaluation electronics has the time resolution better than 20 ps. The initial cosmic ray test with MRPC detectors was also conducted to confirm the performance of data readout. The evaluation system can subsequently be used for quality evaluation of the CBM-TOF super module.

Minioral:

Yes

Description:

QE board

Speaker:

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451

Real-time State Monitoring System for Motor Based on Web

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Motor is the most widely used power equipment in the industrial field, and it is also an important key equipment in the industrial Internet of things (IIOT). The traditional way of motor monitoring is to monitor a single motor, and the collected data is not stored effectively, so that the data cannot be analyzed and processed and the value of the data is not fully utilized. With the development

of the technology of cloud computing and IIOT, the manufacturing process has many advantages, such as massive data storage, remote control and so on.At present, professional cloud services have reduced the traditional industry with cloud service threshold and improved the safety and diversity of cloud services, which provides effective technical guarantee for the product of intelligent motor related enterprises. This paper uses web technology and real-time data from acquisition system to realize real-time state monitoring for motor. The users can be informed the state of motor, and analyze the collected data at any time when they login the system. It is necessary to prevent or prejudge the fault of motor equipment in advance, and avoid major accidents as much as possible. It provides valuable experience and basis for routine maintenance and management of production equipment, and eliminates problems such as “over maintenance” or “under maintenance” during traditional periodic maintenance. The users can save costs and improve efficiency.

Minioral:

No

Description:

monitoring

Speaker:

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IPP Hefei

Country:

China

484

The Study of Multi-Layer sTGC Test System for ATLAS Phase-I upgrade

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ATLAS is one of the four experiments at Large Hadron Collider(LHC).LHC will be upgraded in the next several years aiming to new physics study. ATLAS experiment will fulfill Phase-I upgrade by 2020. The current ATLAS muon end-cap system(Small Wheel, SW) will be replaced with a completely New Small Wheel(NSW). The NSW is a set of precision tracking and trigger detectors able to work at high rates with excellent real-time spatial and time resolution. The small-strip Thin Gap Chamber(sTGC) will devote to trigger function in NSW.
sTGC contains pad, wire and strip readout. The pads on the four-layer sTGC quadruplets are used through a 3-out-of-4 coincidence to identify muon tracks roughly pointing to the interaction point(IP). They are also used to define which strips need to be readout to obtain a precise measurement in the bending coordinate for the event selection. The signals from strips and pads of sTGC quadruplets will be readout by two different front-end boards(FEB), strip FEB(sFEB) and pad FEB(pFEB), respectively. The FEB boards are mounted on the sTGC quadruplets.

This paper presents the study of multi-layer sTGC test system, and it is named Front End Boards Driver Card (FEBDC), which has the capability of handling four sFEBs and four pFEBs simultaneously. The connection and communication between FEBDC and the eight p/sFEBs are the same as a real sTGC Readout system. So the front-end chips on FEBs can be configured by the FEBDC and the raw data for the hit-events can be readout and sent to the FEBDC.

Minioral:

Yes

Description:

STGC DAQ board

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632

467 A readout method based on 10 gigabit Ethernet for silicon pixel detector

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467

A readout method based on 10 gigabit Ethernet for silicon pixel detector

Author: Hangxu Li[1]

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With the rapid development of network protocol, TCP/IP has been widely applied in various OS systems because of its advantages of high-speed network transmission and standardization. Furthermore, TCP/IP has the functions of retransmission and flow control, so it can ensure data's security and stability. In recent years, as a transmission Field-bus, it is also widely used in high-energy physics detector. This article describes a readout method using 10 gigabit network processor applied in silicon pixel detector which is a pixel detector designed for the High Energy Photon Source (HEPS) in China. The PHY layer and the MAC layer of this hardware are both instantiated in FPGA. The logic of hardware can process and read out the data of the detector, meanwhile, it wraps up data and send them to TOE (TCP Offload Engine). A kind of bus control protocol interface is also provided, which can facilitate the host computer to read and write the specific register directly through the

UDP protocol. Only a piece of FPGA can complete the processing of the TCP and UDP packets. It is important for the miniaturization of the detector.

Minioral:

Yes

Description:

10G readout

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China

501

Data Acquisition Software for quality evaluation of CBM-TOF super module detector

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Time-of-Flight system in CBM experiment is composed of super modules based on MRPCs for high resolution time measurement. In order to evaluate the quality of detectors during the mass production, a distributed data readout system is developed, in which each data readout module (DRM) board is based on the System-on-Chip technique and the Ethernet, so that data can be parallel transmitted to the back-end computer to meet with the high data rate of 6Gbps. In this paper, the data acquisition (DAQ) software is focused on event building, status monitoring, system controlling and data analyzing. It consists of three parts connected with Ethernet: Data Forwarding Node (DFN), Data Aggregation Node (DAN) and Graphical User Interface (GUI). DFN runs on the DRM board, aims at forwarding data to DAN or transmitting status and commands with GUI. DAN and GUI both run on the back-end computer. DAN is mainly responsible for data receiving and event building. GUI provides friendly and interactive interface for users to control and monitor the electronics system. It also contains offline data analysis which can call MATLAB engines to evaluate the quality of detector. Such hierarchical design is easy to upgrade, as the number of DFN can be configured according to the requirement of experiment, which is suitable for the distributed readout system, and GUI can be customized without any code modification. Laboratory test results show that the data transfer rate of a single data transmission path is about 550Mbps and confirm the function of the DAQ software.

Minioral:

No

Description:

overall DAQ

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Country:

China

431

An SOA based Design of JUNO DAQ Online Software

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The Online Software, manager of the JUNO data acquisition (DAQ) system, is composed of many distributed components working coordinately. It takes the responsibility of configuring, processes management, controlling and information sharing etc. The design of service-oriented architecture (SOA) which represents the modern tendency in the distributed system makes the online software lightweight, loosely coupled, reusable, modular, self-contained and easy to be extended. All the services in the SOA distributed online software system will send messages each to another directly without a traditional broker in the middle, which means that services could operate harmoniously and independently.
ZeroMQ is chosen but not the only technical choice as the low-level communication middle-ware because of its high performance and convenient communication model while using Google Protobuf as a marshaling library to unify the pattern of message contents. Considering the general requirement of JUNO, the concept of partition and segment are defined to ensure multiple small-scaled DAQs could run simultaneous and easy to join or leave. All running data except the raw physics events will be transmitted, processed and recorded to the database. High availability (HA) is also taken into account to solve the inevitable single point of failure (SPOF) in the distribution system. This paper will introduce all the core services' functionality and techniques in detail.
Index Terms—online software, service-oriented, broker less, HA

Minioral:

Yes

Description:

system

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Jin Li

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Country:

China

650

529 Ultra-precision DC source for Superconducting Quantum Computing

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529

Ultra-precision DC source for Superconducting Quantum Computing

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The Superconducting Quantum Computing (SQC) is one of the most promising quantum computing techniques. The SQC requires precise control and acquisition to operate the superconducting qubits. Ultra-precision DC source is used to provide a DC bias for the qubit to work at its operation point. The commercial precise DC sources are used in single or few qubits experiments. With the development of the multi-qubit processor, to use the same DC source device is impossible for its large volume occupation. And it is also impossible to optimize the large commercial device into a small size or design a compact device to match the commercial performance in a short time.

We study the requirements of the experiments, and set a goal of 2 ppm precision and 10 ppm over all drift in -2.5V to +2.5V range to satisfy the demands of the experiments for our self-design device. To keep the design as simple as possible to prevent any uncontrollable effects, we use a Zener diode as the voltage reference, low noise amplifiers to get the bipolar voltage references, 20-bit DACs to get a controllable output, ceramic PTC materials for temperature control, and one single chip for ethernet and DAC control.

The prototype is accomplished, and primary results show that the standard deviation of 2.5V is less than 2 uV, and the drift in 24 hours is less than 10 uV of 2.5V. We will try to optimize the long-term drift and present the design details and further test results in the paper.

Minioral:

Yes

Description:

Vreg for

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680

431 An SOA based Design of JUNO DAQ Online Software

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642

496 Scalable Self-Adaptive Synchronous Triggering System in Superconducting Quantum Computing

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637

477 Control and Readout Software in Superconducting Quantum Computing

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496

Scalable Self-Adaptive Synchronous Triggering System in Superconducting Quantum Computing

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Quantum computers can solve some specific problems which are deeply believed to be intractable for classical computers. However, building large-scale quantum computers should face lots of challenges. The high-precision synchronous control of all qubits is one of the key techniques we address. Our system serves the Superconducting quantum computing which requires plenty of arbitrary waveform generators (AWG) to work synchronously to drive the quantum processor. The system can achieve the synchronization trigger of all AWGs.
Firstly, the clock generation and distribution system is designed to provide synchronous high-performance reference clocks for each AWG with the synchronized precision less than 20 ps and clock jitters under 200 fs for the initial test, and it can be extended by increasing fan-out units. Next, we design a set of trigger generation firmware elaborately in FPGA, which is controlled by central-computer to generate triggers with configurable counts and intervals. Then the generated trigger fan out to 48

edge-aligned triggers to each AWG as the start signal via a star-like framework which is hardware-compatible with the clock system. Due to routing delay of trigger, reference clock is very likely to capture the rising-edge of the trigger causing a meta-stable state which makes AWGs unsynchronized. Therefore, we develop a self-adaptive firmware that can automatically adjust the trigger, once the meta-stability happens.
With this system, all AWGs can work synchronously, with a synchronization skew less than 20 ps. And the total number of AWGs can be expanded easily in order to manipulate more superconducting qubits.

Minioral:

Yes

Description:

Trigger Sync

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480

High Performance and Scalable AWG for Superconducting Quantum Computing

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Superconducting quantum computer is manufactured based on semiconductor process which makes Qubits integration possible. At the same time, this kind of Qubit keeps high performance on fidelity, de-coherence time, scalability and requires programmable (arbitrary waveform generator) AWG. In this paper, the AWG is implemented with 2 GSPS sampling rate and 16 bit vertical resolution and integrated with separate microwave devices onto a metal plate for scale-up consideration. A special waveform sequence output controller is designed to realize seamless waveform switching and arbitrary waveform generator. The jitter among multiple AWG channels is around 10 ps, INL/DNL is about 2 LSB, and tested Qubit performance of de-coherence time (T2*) achieved 33% promotion over commercial 1 GSPS, 14 bit AWG.

Minioral:

Yes

Description:

AWG

Speaker:

Jin Lin

Institute:

USTC

Country:

China

503

Upgrade of HADES data acquisition and event building software for FAIR phase 0

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The High Acceptance Di-Electron Spectrometer (HADES) is a versatile detector system that has been operational at the GSI heavy ion accelerator facility for about 15 years.

For the "FAIR phase 0"beam time campaign in summer 2018 a number of HADES components are being upgraded, such as the RICH and the ECAL. Both detectors will be read out by dedicated front-end boards with FPGA-based TDCs of the TRB3
family. These TDCs provide an excellent timing precision of about 15 ps. The expected increased data rates, and the necessary software calibration of each TDC channel in the new systems, require significant changes in the DAQ set-up.

This contribution will discuss the software aspects of the DAQ system, such as the network topology of front-end and event builders, implementing TDC calibration directly in event builder nodes, and reducing the amount of data stored on the disks.

Minioral:

No

Description:

DAQ boards

Speaker:

Serguei Linev

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Country:

Germany

547

Three - phase motor state monitoring and fault diagnosis system based on LabVIEW

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Absrtact: Motor is the most widely used production equipment in industrial field. In order to realize the real-time state monitoring and multi-fault pre-diagnosis of three-phase motor, this paper presents a design of three-phase motor condition monitoring and fault diagnosis system based on LabVIEW.The multi-dimensional vibration acceleration, rotational speed, temperature and current and voltage signals of the motor are collected with NI cDAQ acquisition equipment in real time and high speed. At the same time, the model of motor health state and fault state is established.The order analysis algorithm and the axis trajectory analysis algorithm are used to process the original data at an advanced level, and the diagnosis and classification of different fault types are realized.The system is equipped with multi - channel acquisition , display , analysis and storage . Combined with the current cloud transmission technology , we will backup the data to the cloud to be used by other terminals .

Minioral:

No

Description:

Motor phase

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China

448

Using Adjacent Data Retransmission to Improve the Transmission Efficiency of Multi-hop Relay Networks

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Data transmission systems are widely used in various aspects of life, industry, research and other fields, many of them require multi-hop transmission to achieve coverage extension and throughput enhancement, such as Wireless Mesh Network (WMN), Mobile Ad-hoc Network (MANET), Wireless Sensor Networks (WSN) and so on. The biggest problem of multi-hop transmission lies in that end-to-end transmission reliability and bandwidth utilization decrease since data transmission failures occur more frequently due to bit error rate (BER). This paper analyzes the impact of BER on the utilization of multi-hop relay transmission bandwidth and proposes a simple and flexible transmission mechanism suitable for multi-hop transmission scenarios. The simulation results of the proposed scheme show that the scheme can greatly improve the transmission efficiency under the scenario of high BER compared with the end-to-end transmission.

Minioral:

No

Description:

transmission efficiency

Speaker:

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Country:

China

662

574 System integration and initial performance of B2link in Belle II experiment

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661

573 Data analysis to evaluate the CPPF system in CMS trigger phase I upgrade

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574

System integration and initial performance of B2link in Belle II experiment

Authors: Zhen-An Liu[1]; Ryosuke ITOH[None]

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Belle2link(B2link) is an unified data collection system providing front-end data readout from all individual sub-detector systems, and at the same time providing on the other side of the system at the backend slow control functionalities to the frontend electronics for parameter settings. That is, via the links downward, slow control commands can be transmitted from backend to the frontend, and the slow control data(detector parameters) from frontend electronics can be transmitted back by sharing the same data link for the high speed normal data from the detector.

The system has been applied to all the Belle II subsystems:CDC,SVD,ECL,RICH,TOP and KLM before year 2017. Tests have been made with satisfactory and system with full drift chambers(CDC) and full electromagnetic calorimeter(ECL) has been been tested with cosmic ray in 2017. This presentation will talk about the final B2link integration and system test results.

Minioral:

Yes

Description:

System integration

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China

573

Data analysis to evaluate the CPPF system in CMS trigger phase I upgrade

Authors: Zhen-An Liu[1]; Libo Cheng[1]; Pengcheng Cao[2]; Jingzhou Zhao[3]; for CMS Collaboration[None]

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The CMS Level-1 trigger upgrade system consists of several layers of electronics with a large number of homogeneous cards based on the Micro-TCA(uTCA) standard. The CPPF(Concentration Pre-Processing and Fan-out)system belongs to one of the electronic layers, covering the Muon RPC Overlap and Endcap region, and provides preprocessing algorithm for track finding. It includes, in hardware, eight specially designed CPPF cards, one generic CMS card called AMC13, one commercial MCH card, and a Micro-TCA Shelf. Its functionality is realized with five firmware modules: TTC module, optical input module, optical output module, readout module, and a CORE module for cluster finding and transformation. In addition to the firmware functionality, online software is needed for controlling and monitoring each individual CPPF module and the whole CPPF system. This presentation will discuss the data analysis to evaluate the system.

Minioral:

Yes

Description:

Trigger

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Country:

China

464

Development of FEB Configuration Test Board for the ATLAS NSW Upgrade

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The FEB(front end board) configuration test board is developed aiming at the requirement of testing the new generation ASIC chips and its configuration system for ATLAS NSW(New Small Wheel) upgrade, this research studies the configuration of the key chips on the FEB–VMM3 and TDS2 using GBT-SCA, develops multiple level standards and communication protocol, and verifies the whole data link. It provides technical reference for prototype FEB key chip configuration and data readout, as well as the final system configuration.
The FEB configuration data is transmitted to FEB by the control room through L1DDC (L1 Data Driver Card). The communication between L1DDC and FEB adopts E-link communication protocol, and the interface adopts the miniSAS connector. The configuration functions that NSW needs to be completed by configuring each piece of FEB for Micromegas and sTGC detectors, each board should be equipped with GBT-SCA ASIC. A total of 1536 pieces of FEB for sTGC detectors, and A total of 4096 pieces of FEB for Micromegas detectors should be configured.
The FEB configuration test board realizes the operation and control of the SCA chip, including E-link, SPI, I2C, GPIO communication, implements the configuration of VMM3 and TDS2, while verifying the TDS2 4.8Gbps High-speed data transfer function. The test results show that the technology can meet requirements of the future configuration of FEB, and the FEB configuration test board also conducted electronic integration test in CERN, it completed communication with Pad trigger and Router board.

Minioral:

Yes

Description:

FEB test board

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682

436 A Design of FPGA Based Small Animal PET Real Time Digital Signal Processing and Correction Logic

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436

A Design of FPGA Based Small Animal PET Real Time Digital Signal Processing and Correction Logic

Authors: Jiaming Lu[1]; Lei Zhao[1]

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Small animal positron emission tomography (PET) is a high sensitivity and resolution PET device for small animal imaging. Flexibility, high efficiency, high precision charge measurement and position calculation are major demands of a practical PET system which asks for a high-quality analog front end and a digital signal processing module. To achieve higher efficiency and compatibility of multiple data processing modes, we design the real time digital signal processing logic of the small animal PET system, which implements 32-channel signal processing in a single Xilinx Artix-7 family of FPGA and integrates several functions, including 2D raw position calculation, crystal identification, events energy filtering, flood map and energy spectrum real time histogram, etc. A technical design of the Crystal Look-up Table (CLT) is applied here to reduce logic consumption in order to achieve the high integration and the simplification of the logic design. Besides, a series of on-line corrections are also integrated for higher resolution, such as, timing-energy correction, energy calibration to 511 keV photon peak with crystal granularity, timing offset correction with crystal granularity, etc. The pipe-line logic processes the signals at 125 MHz with a 1,000,000 events/s rate. To evaluate the performance of the logic, a series of initial testing are conducted. The results indicate that the logic achieves the expectations.

Minioral:

Yes

Description:

DSP

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670

410 An ultra-sensitive balanced detector with low noise for continuous-variable quantum key distribution

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410

An ultra-sensitive balanced detector with low noise for continuous-variable quantum key distribution

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Continuous-variable quantum key distribution (CVQKD) is of great significance for future information security. The CVQKD can achieve higher key rates over short distances and possesses the potential to communicate in daylight. Although the existing commercial balanced detectors are well established, they are not suitable for CVQKD because their CMRR is usually less than 40dB and the sensitivity is low. Therefore we developed a dedicated balanced detector for our CVQKD experiments with very low noise in a gain of 3.2E5 V/W.
Due to signal tail, charge-sensitive amplifier is no longer appropriate as the pulse repetition frequency in experiments increased from hundreds of KHz to dozens of MHz. To solve the problem, we use trans-impedance amplifier instead. A two-stage amplification circuit structure makes it possible to achieve an ultra-high sensitivity of 3.2E5 V/W while keeping an effective bandwidth of 70MHz. This paper introduces our low noise balanced detector. A JFET is connected between photodiodes and transimpedance amplifier to suppress the amplifier leakage current, reducing electrical noise. Benefit from this design, the RMS of noise voltage is 5.5mV, and it means an ultra-low noise equivalent power density of 2E-12 W/√Hz, only half of common low-noise commercial detectors. Two specially selected InGaAs PIN photo diodes are serially connected for photocurrent reduction and the CMRR eventually reached 55dB, about 15dB higher than commercial detectors. Compared with the existing slow CVQKD experiments performed in a stable fiber, our sensitive low-noise detector will be helpful to achieve a faster CVQKD in complex channel.

Minioral:

Yes

Description:

Quantum-key

Speaker:

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Country:

China

655

549 I2C management based on IPbus

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549

I2C management based on IPbus

Authors: Shiyu Luo[None]; Junfeng Yang[None]; Kezhu Song[None]; Tengfei Chen[None]; Tianbo Xu[None]; Hongwei Yu[None]; Cheng Tang[None]; Hongwei Zhao[None]

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CBM (Compressed Baryonic Matter) is mainly used to study QCD phase diagram of strong interactions in high and moderate temperature region. Before the next generation GBTx based CBM DAQ system is built up, the DPB (Data Processing Board) layer is used in data readout and data pre-processing, where a general FPGA FMC carrier board named AFCK is used. This paper mainly describes the management of the Inter-integrated Circuit (I2C) devices on AFCK and the FMCs it carries via IPBus, an FPGA-based slow control bus used in CBM DAQ system.
On AFCK, the connection of IPBus depends on the correct initialization of a set of I2C devices, including the I2C-bus multiplexer (choosing correct I2C bus), the clock crosspoint switch (providing the 125MHz needed by 1000BASE-X/SGMII), the serial EEPROM with a EUI-48 address (providing the AFCK MAC address). An independent initial module can execute an I2C command sequence stored in a ROM, through which the FPGA can write to/read from the I2C devices without IPBus, so that the related I2C devices are correctly initialized and the necessary preparation for the IPBus start-up is fulfilled. After the initialization, a Wishbone I2C master core is used as an IPbus slave and all other I2C devices can be configured directly via IPBus. All the design has been fully tested in the CBM DPB design.

Minioral:

Yes

Description:

IPBus

Speaker:

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China

647

514 High-power Piezoelectric Tuner Driver for Lorentz Force Compensation

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514

High-power Piezoelectric Tuner Driver for Lorentz Force Compensation

Author: Dariusz Makowski[1]

Co-authors: Aleksander Mielczarek [2]; Piotr Perek [2]; Aleksander Szubert [2]; Pawel Plewinski [2]; Grzegorz Jablonski [2]; Wojciech Cichalewski [2]; Andrzej Napieralski [2]

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Superconducting Radio Frequency (SRF) cavities are used in modern accelerators to efficiently accelerate particles. When cavity is supplied with pulsed RF field it undergoes a mechanical strain due to the Lorentz force. The resulting deformation causes dynamic detuning whose amplitude depends on mechanical properties of the cavity, RF pulse rate and their profile. This effect causes considerable loss of acceleration performance. Therefore, it is usually actively compensated, most commonly with fast piezoelectric actuators.
MicroTCA.4 standard was developed to accommodate control and data acquisition electronic systems of large-scale physics applications. The paper presents a design of high-power amplifier implemented using the MicroTCA.4 technology. The design of the driver was optimized for driving large-capacitance piezo actuators. Several possible architectures of the driver are presented and compared, taking into consideration the power and cooling limitations of MicroTCA.4. The design of a two-channel piezo driver and its initial laboratory test results are also discussed.

Minioral:

Yes

Description:

microTCA 4.

Speaker:

Dariusz Makowski

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Country:

Poland

487

A Zynq –based flexible ADC architecture combining real-time data streaming and transient recording

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The RFX-mod2 Nuclear Fusion experiment is an upgrade of RFX-mod. Among the other improvements in machine structure and diagnostics, a larger number of electromagnetic probes (EMs) is foreseen to provide more information about plasma instabilities and to allow an improved real-time plasma control. An Analog to Digital Converter (ADC) architecture able to provide both transient recording and real-time streaming is foreseen in RFX_mod2. Transient recording provides full speed data acquisition (up to 1 MSample/s) by recording data in local memory and reading memory content after the plasma discharge. Real-time streaming of subsampled data is required for active control. The chosen technology is based on the XILINX Zynq architecture that provides in the same chip a multicore ARM processor tightly couple to a FPGA. Time critical functions carried out by the FPGA in this context are:
1) The management of a circular data buffer and the DMA transfer in RAM of pre and post trigger samples after the trigger has been received;
2) Antialiasing filtering and subsampling of the samples to be streamed. The resulting samples are enqueued in a FIFO accessed by the processor.

The functions carried out by the processor are:
1) The management of the configuration setting, received via TCP/IP or HTTP. The processor validates the configuration and write the appreciate registers in the FPGA;
2) Offline data readout of acquired samples in transient recording;
3) Network data streaming of subsampled data read from the FIFO and sent in UDP packets to the active plasma control system.

Minioral:

Yes

Description:

Zynq DAQ

Speaker:

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644

506 FPGA IMPLEMENTATION OF RDMA-BASED DATA ACQUISITION SYSTEM OVER 100 GBE

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505

A GENERIC DAQ FRAMEWORK FOR HIGH PERFORMANCE 2D XRAY DETECTORS

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Scientific experiments rely on some type of measurements that provides the required data to extract aimed information or conclusions. Data production and analysis are therefore essential components at the heart of any scientific experimental application.
Traditionally, efforts on detector development for photon sources have focused on the properties and performance of the detection front-ends. In many cases the data acquisition chain was treated as a complementary component of the detector system that was added at a late stage of the project. In some cases, the data acquisition subsystems, although achieving minimum bandwidth requirements were kept relatively simple in term of functionalities, and this to minimize design effort, complexity and implementation cost.
This approach is changing in the last years as it does not fit new high performance detectors; industrial data acquisition protocols do not provide the required data throughput and implementing high performance schemes becomes much more difficult and resource consuming. Detector developers are changing their paradigm and moving into the development and implementation of reusable high performance data acquisition schemes that can be applied to different kind of detector devices.

This paper addresses the definition and development of a data acquisition framework, called RASHPA, which has been designed and optimised to be integrated in future light source detectors. This framework is conceived to be adopted by developers working with a variety of detection technologies and schemes and not specific to one detector. RASHPA however is optimised and will provide maximum added value when used with two dimensional area detectors.

Minioral:

No

Description:

Speaker:

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Institute:

ESRF

Country:

France

506

FPGA IMPLEMENTATION OF RDMA-BASED DATA ACQUISITION SYSTEM OVER 100 GBE

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[1] *ESRF*

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The ESRF has undertaken the implementation of a data acquisition framework for 2D-Xray detectors called RASHPA. It allows detectors to push data directly into one or more backend computers due to its RDMA feature. In principle, RASHPA is independent of the high speed data link type as long as it supports RDMA and network routability in order to dispatch data to multiple destinations. In a preliminary prototype, PCIe-over-cable was selected to be the candidate.
Despite the benefits of this type of link, for which the native RDMA feature is the most important, it presented strong limitations including the availability of COTS products in particular PCIe-over-cable adapters and switches in addition to the lack of standardization of optical cabling form.
Ethernet protocol is a standard way of communication and widely used in nowadays networks. Thanks to recent FPGA generations that embed a 100G MAC IP, the integration of such high bandwidth data link in next detector generations becomes possible. RDMA over Ethernet is a subject of many recent projects such as RoCE and iWarp.
In this work, the hardware implementation of a basic RDMA over UDP/IP Ethernet transmitter/receiver logic on a KCU116 (kintex ultrascale+) Xilinx development board is presented. A commercial 100Gb Mellanox board (MCX415A-CCAT) is used together with wireshark software to analyze the received packets. Obtained results show that one can reach a maximum stable performance of 95 Gbps with minimum packets size of 32KB. In the final paper, the FPGA implementation of the 100Gb Ethernet network will be detailed.

Minioral:

Yes

Description:

100GbE

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France

709

581 Java Driver Implementation for the Ethernet Flash ADC

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581

Java Driver Implementation for the Ethernet Flash ADC

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This paper describes the software developed for control configuration and data access of the Ethernet Flash ADC (EFADC) and the paired module known as the Ethernet Trigger Supervisor (ETS). The EFADC and ETS are a multiple-unit system designed to provide coincidence data acquisition in a modular form with 4 ns timing resolution. The paper briefly describes the EFADC and ETS hardware at the top level and delves into the detail of the control driver and the register architecture of each unit. Controllable functions of each module are discussed briefly while the methodology of configuration of the functions is describe in more detail. An overview of the API and its architecture is presented with some detail in the implementation of several of the objects detailed to clarify their functions. A brief review of the graphical user interface is also presented which has allowed the EFADC systems to be deployed in the field for plant biology applications and adopted for other data acquisition tasks.

Minioral:

Yes

Description:

Ethernet ADC

Speaker:

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JLAB

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USA

612

Progress in Particle Therapy Enabled by Real Time Technology

Author: David Meer[1]

[1] *Paul Scherrer Institute*

Overview of current research and technology in Proton and other Particle Therapy in clinical applications.

Minioral:

Description:

Speaker:

Institute:

Country:

605

Precision modeling and readout of germanium detector waveforms for MCMC machine learning

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The Majorana Demonstrator is a neutrinoless double-beta decay
experiment using high purity p-type point contact germanium detectors.
The waveforms produced by these detectors have subtle variation indicating the detailed energy and drift path information for each event. In
addition, the waveforms depend sensitively on crystal impurity levels, temperature, and operating voltage. We have developed a machine learning
algorithm which, given a set of calibration waveforms, can infer detector
parameters. Once these parameters are known, the high precision detector model can be used to fit the drift paths of individual waveforms. This
method can be used as a sensitive background rejection technique for the
Demonstrator or the proposed future LEGEND experiment. In order to
reach specific physics goals, the design of readout instrumentation must
be considered. The development of data acquisition technology for the
Demonstrator and future experiments is discussed.

Minioral:

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545

Design and development of the DAQ and Timing Hub for CMS Phase-2

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The CMS Detector will undergo a major upgrade for the Phase-2 of the LHC physics program, which will start around 2026. The detector will be read out at a rate of 750 kHz by some 50k high-speed optical links, for an average event size of 7.5 MB. In the baseline architecture for the Phase-2 DAQ, the optical links from detector front-ends are aggregated in detector-dependent ATCA based back-end boards.
A DAQ and Timing Hub (DTH) aggregates data streams from multiple back-end boards over point-to-point links. The DTH combines these streams to feed high speed commercial 100 Gb/s optical links, forming the data-to-surface (D2S) network. It provides buffering for time decoupling and transmission using a reliable high-level protocol, such as TCP/IP. The D2S links carry the data to surface, connecting the DTH output via standard network to I/O servers for the event building. The DTH is also distributing trigger accept and timing signals, as well as trigger control codes for calibration and synchronisation to the back-end electronics, from where they are redistributed to the front-ends.
This paper presents the system level functionality and performance requirements of the DTH. The DTH will have a modular design, where a fully equipped board has a 1.2 Tb/s DAQ bandwidth. The first step of the DTH development roadmap (P1) is currently under design. The goals and design of the P1 will be described. Results from implementation on Ultrascale development kits and a custom add-on board with serial HMC memories will be presented.

Minioral:

No

Description:

Timing Hub

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544

The CMS Data Acquisition System for the Phase-2 Upgrade

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The upgraded High Luminosity LHC, after the third Long Shutdown (LS3) will provide an instantaneous luminosity of 7.5 10**34 cm-2 s-1 (levelled), with a pileup of up to 200 interactions per bunch crossing. During LS3, the CMS Detector will undergo a major upgrade to prepare for the Phase-2 of the LHC physics program, starting around 2026.
The upgraded CMS detector will be read out at an unprecedented data rate of up to 50 Tb/s with an event rate of 750 kHz, selected by the level-1 hardware trigger, and an average event size of 7.5 MB. Complete events will be analysed by the High Level Trigger (HLT) using software algorithms running on standard processing nodes, and selected events will be stored permanently at a rate of up to 7.5 kHz for offline processing and analysis.
Tis paper will present, the baseline design of the DAQ and HLT systems for Phase-2, taking into account the projected evolution of high speed network fabrics for event building and distribution, and the anticipated performance of general purpose CPU. Implications on hardware and infrastructure requirements for the DAQ "data center" are analysed. Emerging technologies for data reduction are considered.
Novel possible approaches to event building and online processing, inspired by trending developments in other areas of computing dealing with large masses of data, are also examined.
Furthermore, opportunities offered by reading out and processing parts of the detector data at the machine bunch crossing rate (40 MHz), wherever the front-end electronics allows, are discussed.

Minioral:

No

Description:

DAQ Phase-2

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Switzerland

698

533 An sTGC Prototype Readout System for ATLAS New-Small-Wheel Upgrade

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533

An sTGC Prototype Readout System for ATLAS New-Small-Wheel Upgrade

Author: Peng Miao[1]

Co-authors: Feng Li [2]; Shengquan Liu [3]; Zhilei Zhang [3]; Xinxin Wang [4]; Tianru Geng [4]; Shuang Zhou [3]; Ge Jin [4]

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ATLAS will replace the muon end-cap detectors, the so-called Small Wheel(SW), with the New Small Wheel (NSW) in the Phase-I upgrade to enhance its high rate performance. Small-Strip Thin Gap Chambers (sTGCs), developing from the Thin Gap Chamber(TGC) technology but with much smaller strip pitch, have been selected as one of the main detector technologies to be used for the NSW. An sTGC quadruplet consists of four pad-wire-strip planes. To readout sTGC signals, two kinds of Front End Board (FEB)will be designed, pad Front End Board(pFEB) and strip Front End Board (sFEB). The pFEB with the maximum 192 channels is responsible for reading out pad and wire signals of each plane, while the sFEB with the maximum 512 channels is responsible for reading out strip signals of one gas-gap. This paper presents a readout system capable of testing one full-size sTGC quadruplet. It consists of 4 pFEBs and 4 sFEBs along with one specifically designed DAQ board. The FEBs use VMM3 ASIC for analog signal amplification and digitization. The DAQ board is able to configure and readout up to 8 FEBs through Gigabit Ethernet. This readout system can be used to evaluate the functionality and performance of sTGC prototype, and help optimize the design of the final pFEB and sFEB.

Minioral:

Yes

Description:

VMM3 ASIC DAQ board

Speaker:

Peng Miao

Institute:

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Country:

China

571

Real-time Data Acquisition and Processing System for MHz Repetition Rate Image Sensors

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One of the optimization goals of a particle accelerator is to reach the highest possible beam peak current. For that to happen the electron bunch propagating through the accelerator should be kept relatively short along the direction of its travel. In order to obtain a better understanding of the beam composition it is crucial to evaluate the electric charge distribution along the μm-scale packets. The task of the Electro-Optic Detector (EOD) is to imprint the beam charge profile on the spectrum of light of a laser pulse. The actual measurement of charge distribution is then extracted with a spectrometer based on a diffraction grating.

The article focuses on developed data acquisition and processing system called the High-speed Optical Line Detector (HOLD). It is a 1D image acquisition system which solves several challenges related to capturing, buffering, processing and transmitting large data streams with use of the FPGA device. It implements a latency-optimized custom architecture based on the AXI interfaces. The HOLD device is realized as an FPGA Mezzanine Card (FMC) carrier with single High Pin-Count connector hosting the KIT KALYPSO detector.

The solution presented in the paper is probably one of the world fastest line cameras. Thanks to its custom architecture it is capable of capturing at least 10 times more frames per second than fastest comparable commercially available devices.

Minioral:

Yes

Description:

Speaker:

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Institute:

University of Lodz

Country:

Poland

570

Framework for High-performance Video Acquisition and Processing in MTCA.4 Form Factor

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The video acquisition and processing systems are commonly used in industrial and scientific applications. Many of them utilize Camera Link interface for the transmission of a video stream from the camera to the host system.

The framework presented in the paper enables capturing such data, processing it and transmitting to the host CPU. It consist of MTCA.4-compliant frame grabber and a set of software libraries supporting several different cameras. It is designed for use in large scale physics experiments such as ITER

tokamak or European X-Ray Free-Electron Laser (E-XFEL), as well as in the Centre for Free-Electron Laser Science (CFEL).

The proposed video acquisition solution features the worlds first Camera Link frame grabber for the MTCA.4 architecture. Thanks to the modern FPGA circuit architecture, the deserialization is done using only the built-in ISERDES primitives, which reduces the costs and complexity of the required hardware.

Minioral:

No

Description:

Video DAQ

Speaker:

Aleksander Mielczarek

Institute:

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Country:

Poland

456

The development of a data acquisition system based on FPGA

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Co-author: JIE ZHANG [1]

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On one side, traditional data acquisition systems based on servers are widely used in high energy experiments. Because challenges from high data throughput, low latency, low power consumption and low cost, this traditional solution is hard to face them. On the other side, the community of Field Programmable Gate Array become large and mature, many functions such as 1 Gaps TCP/IP communication which was mainly realized in x86 server can be realized in Field Programmable Gate Array chips. So a new data acquisition system whose architecture is based on FPGA is researched and developed. There are several features for this system. First, this system could be communicated with readout electronics and upper computers by a 1 Gaps TCP/IP Ethernet. Second, experimental data from readout electronics could be stored in a SATA disk directly by Field Programmable Gate Array. Third, a data acquisition software is developed by web pages and stored in Field Programmable Gate Array. Users use a web browser to monitor the status of data acquisition system. Fourth, WebSocket protocol between user web browser and data acquisition system is used to make a browser send http responses automatically, in order to update the result of data acquisition web pages. Fifth, histograms and hitmaps used widely in experiments are generated in Field Programmable Gate Array, and will be showed in web pages. The power consumption and used resources will be evaluated at the same time.

Minioral:

No

Description:

FPGA daq

Speaker:

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Country:

China

569

Implementation of a High-Performance Pattern Recognition Associative Memory in an FPGA

Authors: Jamieson Olsen[1]; James Hoff[1]; Zhen Hu[1]; Sergo Jindariani[1]; Tiehui Ted Liu[1]; Jinyuan Wu[1]; Zijun Xu[2]

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Pattern recognition associative memory (PRAM) devices are parallel processing engines which are used to tackle the complex combinatorics of track finding algorithms, particularly for silicon based tracking triggers. PRAM development has been mostly limited to the realm of ASICs, which often leads to lengthy and expensive design cycles. FPGAs allow for quick iterations, making them an ideal hardware platform for designing and evaluating new PRAM features before committing to silicon. The FPGA implementation of PRAMs is also highly desirable for early performance studies; for example, it can bring system interface to maturity much sooner and minimize the number of ASIC design cycles. In this talk we present our new PRAM designs and discuss how logic blocks which were originally developed for ASICs are redesigned to take advantage of modern FPGA architectures to increase both speed and pattern density.

Minioral:

Yes

Description:

Pattern Recognition

Speaker:

Jamieson Olsen

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Country:

USA

567

Pulsar3a: Next Generation ATCA Full Mesh General Purpose FPGA Based Processing Board

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In this talk we present the Pulsar3a, our next generation full mesh enabled FPGA-based ATCA processing board. Originally motivated by silicon-based tracking trigger needs for HL-LHC experiments, the Pulsar3a is designed with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth interconnections. Based on Xilinx Ultrascale FPGAs, the Pulsar3a represents a significant step up from the Pulsar2b board in terms of logic resources (693k to 5M logic cells), I/O channels (40 to 96 serial transceivers) and I/O bandwidth (1 to 2 Tbps). Significant redesign of this board was necessary to address the challenges associated with increasing the I/O channel density and bandwidth. For example, the fiber optic transceivers have been relocated from the rear transition module to the front board and positioned near the FPGAs. Moving the optics inboard dramatically shortens the traces between the FPGA and optical transceivers and the Zone-3 connector bottleneck has been avoided completely; this change was necessary to achieve the stringent signal integrity performance required as data transmission rates approach 25 Gbps. Various hardware subsystems developed for the Pulsar2b, such as the direct connection between the FPGAs and the full mesh ATCA fabric interface and custom IPMC mezzanine, have been retained in the Pulsar3a design. These and many other Pulsar3a design details will be presented with a focus on the common challenges facing ATCA board designers, such as high-speed routing, high bandwidth interconnections, power thermal and related cooling issues, as well as the initial prototype performance results.

Minioral:

Yes

Description:

Next Generation

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Country:

USA

656

550 Environmental Monitoring for Belle II

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550

Environmental Monitoring for Belle II

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The Belle II experiment is just starting, to search for physics beyond the Standard Model in B, charm and τ decays using data with the integrated luminosity goal of $50\ \mathrm{ab}^{-1}$. Before the final data taking, Belle II phase 2 run is on-going at the time of the conference, until July 2018. In this presentation, we describe the environmental monitor system with the emphasis on the software tools to help the experts and the non-expert shifters who operate the experiment. monitoring tools are prepared on the control room especially for There are three tools, the monitoring GUI, the alarm system, and the archiver. The monitoring GUI shows the current state of detector and the alarm system generate warning states from monitored variables with sound and email notification. The archiver is collecting data on single server and provide collected data to any person.

Minioral:

Yes

Description:

GUI monitoring

Speaker:

Seokhee Park

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Country:

Korea

400

Nanoseconds Timing System Based on IEEE 1588 FPGA Implementation

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Clock synchronization procedures are mandatory in most physical experiments where event fragments are readout by spatially dislocated sensors and must be glued together to reconstruct the energy and interaction vertex information of incident particles. These distributed data readout topologies rely on an accurate time information available at the frontend, where raw data are acquired and tagged with a precise timestamp prior to data buffering and central data collecting. This makes the network complexity and latency, between frontend and backend electronics, negligible within upper bounds imposed by the frontend data buffer capability. The proposed research work describes an FPGA implementation of standard 1588 Precision Time Protocol (PTP) that exploits the CERN Timing, Trigger and Control (TTC) system as a local network multicast messaging media. The hardware implementation guarantees a clock synchronization beyond 4ns, overcoming the typical accuracy limitations inferred by computers Ethernet based Local Area Network (LAN). The validity of the proposed timing system has been proved in point-to-point data links as well as in star topology configurations over standard cat5e cables. In star topology configuration, in order to solve the marginal capturing phenomena, an hardware based finite state machine scans the bit period using a variable delay chain, and finds the optimal sampling point. The results achieved together with weaknesses and possible improvements are hereby detailed.

Minioral:

Yes

Description:

Timing

Speaker:

Davide Pedretti

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INFN

Country:

Italy

535

ALICE Central Trigger Processor for LHC Run 3

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ALICE (A Large Ion Collider Experiment) is one of the four main experiments at
CERN Large Hadron Collider. The ALICE collaboration plans a major detector upgrade during long shutdown 2,which is at present foreseen to start at the end of year 2018 followed by Run 3 starting in year 2021. The CTP will manage different interaction rates, 50 kHz in Pb-Pb up to few hundred kHz in pp collisions. The trigger system will also allow for different readout strategies. To cover these requirements the ALICE-CTP will be completely redesigned. The new CTP system consist in a new universal trigger board based in Kintex Ultrascale FPGA able to support up to 20 High-speed links and a novel Timing and Trigger Control system based on Passive Optical Networks. The new trigger downstream (CTP to Detectors) distribution is running with 9.6 GHz signal. The overview and current status of the ALICE-CTP will be presented.

Minioral:

Yes

Description:

Trigger

Speaker:

Luis Alberto Perez Moreno

Institute:

University of Puebla

Country:

Mexico

659

562 Radiation-Tolerant, High-speed Serial Link Design with SRAM-based FPGAs

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562

Radiation-Tolerant, High-speed Serial Link Design with SRAM-based FPGAs

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In the field of High Energy Physics experiments, high-speed serial links implemented on SRAM-based FPGAs have been extensively used in the trigger and data acquisition systems. Their application has been usually limited to the off-detector electronics, due to SRAM-based FPGA susceptibility to ionizing radiation effects. However, in order to use these devices in radiation environments, dedicated mitigation techniques can be adopted: information redundancy (typical of error correcting codes), hardware redundancy - such as triple modular redundancy (TMR) - and configuration scrubbing.
In this paper, we present a serial link running at 6.25 Gbps implemented in a Xilinx Kintex-7 FPGA which is protected against radiation effects by means of all the above-mentioned methods.
The link uses a self-synchronizing scrambler for data randomization and a Reed-Solomon encoder/decoder, whose error correction capability is increased by adopting the interleaving technique. The link can vary the protection level of the Reed-Solomon code to cope with different rates of radiation induced faults, trading the available bandwidth off for data redundancy. The reliability of the link is also improved by means different TMR strategies. Moreover, on the same FPGA, a scrubber repairs corrupted configuration frames in real-time.
We present the test results carried out using the fault injection method. We show the performance of the link in terms of mean time between failures (MTBF) of its subcomponents. We also present measurements of mean time between losses of lock of the link. Furthermore, we show the effective bit error ratio (BER) and FPGA current trends versus injected upsets.

Minioral:

No

Description:

SRAM

Speaker:

Sabrina Perella

Institute:

INFN

Country:

Italy

476

ATLAS Tile calorimeter calibration and monitoring systems

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The ATLAS Tile Calorimeter (TileCal) is the central section of the hadronic calorimeter of the ATLAS experiment. This sampling calorimeter uses steel plates as absorber and scintillating tiles as active medium. The light produced by the passage of charged particles is transmitted by wavelength shifting fibers to photo-multiplier tubes (PMTs), located in the outer part of the calorimeter. The readout is segmented into about 5000 cells, each one being read out by two PMTs in parallel. To calibrate and monitor the stability and performance of the full readout chain during the data taking, a set of calibration sub-systems is used. The TileCal calibration system comprises Cesium radioactive sources, laser, charge injection elements, and an integrator based readout system. Combined information from all systems allows to monitor and to equalize the calorimeter response at each stage of the signal evolution, from scintillation light to digitization. Calibration runs are monitored from a data quality perspective and used as a crosscheck for physics runs. Data quality in physics runs is monitored extensively and continuously. Any problems are reported and immediately investigated. The data quality efficiency achieved was 99.6% in 2012, 100% in 2015, 98.9% in 2016 and 99.4% in 2017.

Based on LHC Run-I experience, all calibration systems were improved for Run-II. TileCal performance during LHC Run-II, (2015-2017), is discussed, including calibration, stability, absolute energy scale, uniformity and time resolution. Results show that the TileCal performance is within the design requirements and has given essential contribution to reconstructed objects and physics results.

Minioral:

Yes

Description:

calibration, monitoring

Speaker:

ATLAS

Institute:

CERN

Country:

China

649

527 FLIT-level Infiniband network simulations of the DAQ system of the LHCb experiment for Run-3

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527

FLIT-level Infiniband network simulations of the DAQ system of the LHCb experiment for Run-3

Author: Flavio Pisani[1]

Co-authors: Domenico Galli [2]; Matteo Manzali [3]; Niko Neufeld [4]; Paolo Durante [4]; Rainer Schwemmer [4]; Sebastien Valat [4]; Tommaso Colombo [4]; Umberto Marconi [2]

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The LHCb (Large Hadron Collider beauty) experiment is designed to study differences between particles and anti-particles as well as very rare decays in the charm and beauty sector at the LHC. The detector will be upgraded in 2019 and a new trigger-less readout system will be implemented in order to significantly increase its efficiency and take advantage of the increased machine luminosity.

In the upgraded system, both event building and event filtering will be performed in software for all the data produced in every bunch-crossing of the LHC. In order to transport the full data rate of 32 Tb/s we will use custom FPGA readout boards (PCIe40) and state of the art off-the-shelf network technologies. The full event building system will require around 500 nodes interconnected together.

From a networking point of view, event building traffic has an all-to-all pattern, therefore it tends to create high network congestion. In order to maximize the link utilization different techniques can be adopted in various areas like traffic shaping, network topology and routing optimization. The size of the system makes it very difficult to test at production scale, before the actual procurement. We resort therefore to network simulations as a powerful tool for finding the optimal configuration.

We will present an accurate low level description of an Infiniband based network with event building like traffic. We will show comparison between simulated and real systems and how changes in the input parameters affect performances.

Minioral:

Yes

Description:

Inifiband simulation

Speaker:

Flavio Pisani

Institute:

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Country:

Switzerland

417

DREAM Based DAQ system for the BONuS12 Experiment at Jefferson Lab

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The BONuS experiment has been designed to study the free neutron structure at Jefferson Lab using spectator tagging technique in d(e, ep)X inelastic scattering. We detect the scattered electrons by the standard CLAS12 detector, but backscattered low momentum spectator protons in this experiment are detected installing a new RTPC detector. Signals on the RTPC readout are directly sent to the DREAM electronics which pre-processes those signals and buffers them in 512 cell circular memory. While processing signals, DREAM chip performs the amplification, filtering, shaping, discrimination and sampling. A FEU is used to assemble eight DREAM chips along with ADCs for getting digitized output data coherently. Each compact chip contains 64 channels, so we easily handle total 17280 readout pads of our detector using 34 FEUs. Gigabit Ethernet link are used to send out data from FEU to the backend unit, whereas a USB cable is used for the slow control of the FEUs and DREAMs. Slow-control allows to configure various parameters such as gain of the amplifier, shaping parameters, discrimination in the trigger building process and many more. We can also fix event-size from the slow-control, which qualifies DREAM for dead-timeless readout of upto 20MHz with a trigger rate upto 20KHz. During the last year, we performed a detailed study of DREAM performance with a prototype RTPC which provided some promising results. These results are very significant for BONuS12, and we believe it would be notable to other physics experiments as well.

Minioral:

Yes

Description:

chip use DREAM

Speaker:

Jiwan Poudel

Institute:

Old Dominion

Country:

USA

509

Streaming Readout of the sPHENIX Tracking System

Author: M. L. Purschke, for the sPHENIX collaboration[None]

The sPHENIX Collaboration at RHIC is upgrading the PHENIX detector in a way that will enable a comprehensive measurement of jets in relativistic heavy ion collisions. The upgrade will give the experiment full azimuthal coverage within a pseudorapidity range of $-1.1 < \eta < 1.1$.

Since the last conference, we have make significant progress with the readout of our calorimeters, which work with a "classic" triggered-event paradigm. At the same time, we have developed the prototype readout electronics for the Time Projection Chamber, which will operate in streaming, or trigger-less, readout mode. Most likely, another detector, our MAPS-based vertex detector (MVTX), will be read out in streaming mode as well.

We will present an overview of the DAQ system and the choices and current status of the readout electronics, firmware, and software components, especially with the streaming readout of the TPC.

Minioral:

Yes

Description:

streaming readout

Speaker:

Martin Purschke

Institute:

BNL

Country:

USA

491

An FPGA TDC Based on Multi-wave and Multi-chain Measurements Averaging Structure

Authors: Shen Qi[None]; Peng Shang[None]; Shengkai Liao[None]; Shubin Liu[None]; Qi An[None]; Chengzhi Peng[None]

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A high performance time-to-digital converter (TDC) based on multi-wave and multi-chain measurements averaging structure is proposed and implemented in FPGA in this paper. The wave union TDC and multi-chain averaging TDC has been used to improve both the timing resolution and precision, respectively. However, both structures have disadvantages compared with plain TDC based on single tapped-delay chain. The wave union TDC suffers from more dead times and the multi-chain TDC needs more logic resources. We combine both structures to make a new TDC which uses multi-chains and multi-wave unions (MCMW) simultaneosly. In this new MCMW TDC, the dead time and resource utilization can be balanced or switched to each other based on different requirements while ensuring the timing performance. So the MCMW TDC is more flexible and better than either

wave union or multi-chain TDC. The input signal is connected to multiple tapped-delay chains simultaneously (the chain number is M), and there is a fixed delay cell between every two adjacent chains. Each tapped-delay chain is a wave union TDC (the wave number is N). So there should be M*N TDC times generated for a single input signal. After calibration and averaging, the final TDC time is obtained. A MCMW TDC with 1 ps bin size and 6.0 ps RMS is obtained with M = 8, N = 13. For comparison, the plain TDC with M = N = 1 yields 31.2 ps bin size and 18.2 ps RMS.

Minioral:

No

Description:

multi-wave, multi-chain

Speaker:

Shen Qi

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China

691

487 A Zynq –based flexible ADC architecture combining real-time data streaming and transient recording

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616

388 Web-based Real Time Monitoring with HTML5

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388

Web-based Real Time Monitoring with HTML5

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Experiments in nuclear and plasma physics require real-time monitoring. In the past, dedicated control applications have been written for graphical display of process parameters. Modern web technologies allow nowadays the control and monitoring of real-time processes directly from any browser. This has the advantage that no software has to be installed, software updates are automatically reflected in the browser, and mobile devices with web browsers can be used to control experiments.

This paper describes a set of techniques which make this easily possible. A minimal web server based on the Mongoose Server is used to connect directly to the hardware for monitor and control. JavaScript Object Notation (JSON) is used to exchange data between the server and the browser, and Typed Arrays are used for high-speed waveform transfer.

The browser side uses Asynchronous JavaScript Extensions (AJAX) together with Remote Procedure Calls (JSON-RPC) to retrieve data from the web browser. The HTML canvas element is then used to render any graphics. Features of an oscilloscope implementation inside a web browser are shown and indications are give how to use these techniques for other applications.

Minioral:

Yes

Description:

Json

Speaker:

Stefan Ritt

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PSI

Country:

Switzerland

683

446 A General Purpose FPGA-based Programmable Digital Patter Generator

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446

A General Purpose FPGA-based Programmable Digital Patter Generator

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A fully synchronous programmable pattern generator is often required in modern physics experiments.
Typical cases are experiments that use Charge Coupled Device (CCD) as detectors or the design verification of electronics devices.
Most of the times commercial pattern generators are used but in some specific cases they are not practical or impossible to use. An alternative is to implement a pattern generator on a Field Programmable Gate Array (FPGA).
The proposed design feature 32 outputs a time resolution of 10 ns and a fully programmable structure that allows the generation of patterns from 10 ns to minutes of length. The architecture looks like a simple processor hence the pattern is defined writing a program that resides inside the FPGA' s memory.
A so-called time-slice represents the pattern generator's basic element. A time-slice is defined by a

steady state of the outputs. A pattern is defined by a sequence of time-slices that are concatenated and executed in sequence. A group of time-slices is called function and can contain up to 16 time-slices. 16 different functions can be defined.
The execution order of different functions is written in the program memory by means of instructions or Operation Codes.
The concept of pointers is also implemented to provide high flexibility in writing the program.
The sequence execution time is tightly controlled to ensure a resolution of 10 ns over the entire sequence without glitches and latencies. The design is written in vhdl and can be ported on all kinds of FPGA.

Minioral:

Yes

Description:

FPGA

Speaker:

Stefano Russo

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USA

696

523 Additive phase-noise in frequency conversion in LLRF systems

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523

Additive phase-noise in frequency conversion in LLRF systems

Author: Igor Rutkowski[1]

Co-author: Krzysztof Czuba [1]

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This contribution focuses on phase-noise added during frequency conversion in low level radio frequency (LLRF) control systems. The stability of beams'parameters in linear accelerators depends on the stability of amplitude and phase of the accelerating field. A LLRF control system regulates the electromagnetic field inside accelerating modules based on the input RF signals. Typically those signals are converted to an intermediate frequency (IF) using an active mixer. This field detection scheme necessitates synthesis of a heterodyne/local oscillator (LO) signal which is often generated using a passive mixer. Additive close–to-carrier phase noise can be observed in the investigated circuits.
According to the author's best knowledge, there is no work presenting research on the phase noise characteristics of an active mixer. The influence of the LO signal power level on the phase noise

of the output signal was measured and two hypotheses were made. Further measurements of the AM-PM and PM-AM conversion were made to verify one of the hypotheses.
The fidelity of the LO signal is partially determined by the phase noise of the IF signal. The possibility of constructing an analytical model for selected types of frequency dividers which are used for LO synthesis was considered.
The phase noise of the output signal of a passive mixer is typically calculated using a small-signal model based on modulation theory. Measurements'results indicate that the power level of the input signals has a non-linear effect on phase noise beyond the noise floor.

Minioral:

Yes

Description:

?

Speaker:

Igor Rutkowski

Institute:

University of Warsaw

Country:

Poland

586

Software-Defined Radio Readout System for the ECHo experiment

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Metallic Magnetic Calorimeters (MMCs) are calorimetric low-temperature particle detectors that are currently strongly advancing the state-of-the-art in energy-dispersive single particle detection. MMCs are typically operated at temperatures well below 100 mK and make use of a metallic, paramagnetic temperature sensor to transduce the temperature rise of the detector upon the absorption of an energetic particle into a change of magnetic flux. An efficient readout of large MMC arrays can be achieved through Microwave SQUID multiplexing. One of the pioneering applications of large MMC arrays is the "Electron capture in Holmium-163 experiment" (ECHo), which aims to investigate the electron neutrino mass in the sub-eV/c^2 range. ECHo will use up to 10^4 detectors running in parallel to acquire a high statistics spectrum in finite time. The readout of these detector arrays will be conducted using 15 independent FPGA based software-defined radio (SDR) systems, each connected to one microwave SQUID multiplexed readout line with 400 detector channels equally distributed between 4 and 8 GHz. This results in an input data rate of 2.4 Tb/s, which is processed in cascaded stages to channelizes the signals online. Afterwards, the event specific information is extracted in parallel for each channel and eventually stored in the backend server storage. The SDR consists of a two-stage RF mixing electronics, various high-speed, high-resolution DACs/ADCs, as well as a Zynq Ultrascale+ FPGA for the digital processing. This contribution will describe the SDR electronics for ECHo in detail and present the challenges associated with the integration of such heterogeneous systems.

Minioral:

No

Description:

Radio DAQ

Speaker:

Oliver Sander

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KIT

Country:

Germany

643

504 Real-time data compression for data acquisition systems applied to the ITER Radial Neutron Camera

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504

Real-time data compression for data acquisition systems applied to the ITER Radial Neutron Camera

Author: Bruno Santos[1]

Co-authors: Nuno Cruz [2]; Ana Fernandes [2]; Paulo Fortuna Carvalho [2]; Jorge Sousa [2]; Bruno Gonçalves [2]; Marco Riva [3]; Fabio Pollastrone [3]; Cristina Centioli [3]; Daniele Marocco [3]; Basilio Esposito [3]; Carlos Correia [4]; Benoit Brichard [5]; Rita Costa Pereira [2]

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The aim of the ITER Radial Neutron Camera Data Acquisition prototype is to sustain a 2 MHz peak event for each channel with 128 samples of 16 bits per event. The data is acquired and processed using an IPFN FPGA Mezzanine Card (FMC-AD2-1600) with 2 digitizer channels of 12-bit resolution sampling up to 1.6 GSamples/s, based on a PCIe evaluation board from Xilinx (KC705) installed in the host PC.
The acquired data in the event-based data-path is streamed to the host through the PCIe x8 Direct Memory Access (DMA) channels and the maximum data throughput per channel is ~0.5 GB/s of raw data (event base), ~1 GB/s per digitizer.
The prototype architecture comprises one host PC with two KC705 modules and four channels, producing up to ~2 GB/s in event mode and up to ~3.2 GB/s in continuous mode. To reduce the produced data throughput from host to ITER databases, the real-time data compression was evaluated using

the LZ4 lossless compression algorithm, which provides compression speed up to 400 MB/s per core. This contribution presents the architecture, implementation and test of the parallel real-time data compression system running in multiple isolated CPU cores. The average space saving and the performance results for long term acquisitions up to 30 minutes, using different data block size and different number of CPUs, are also presented.

Minioral:

Yes

Description:

Neutron camera DAQ

Speaker:

Bruno Santos

Institute:

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Country:

Portugal

701

540 Simulation System for the Wendelstein 7-X Safety Control System

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540

Simulation System for the Wendelstein 7-X Safety Control System

Author: Jörg Schacht[1]

Co-authors: Andreas Wölk [2]; Uwe Herbst [1]; Dirk Naujoks [3]; Steffen Pingel [1]

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The Wendelstein 7-X (W7-X) Safety Instrumented System (SIS) ensures personal safety and investment protection. The development and implementation of the SIS are based on the international safety standard for the process industry sector, IEC 61511. The SIS exhibits a distributed and hierarchical organized architecture consisting of a central Safety System (cSS) on the top and many local Safety Systems (lSS) at the bottom. Each technical component or diagnostic system potentially hazardous for the staff or for the device is equipped with an lSS. The cSS is part of the central control system of W7-X. Whereas the lSSs are responsible for the safety of each individual component, the cSS ensures safety of the whole W7-X device. For every operation phase of the W7-X experiment hard- and software updates for the SIS are mandatory. Finally, the safety programs of the central and local safety systems have to be verified for every development stage and validated against the

safety requirement specification.
This contribution focuses on the application of a model based simulation system for the whole SIS of W7-X. A brief introduction into the development process of the SIS and its technical realization will be give followed by a description of the design and implementation of the SIS simulation system using the framework SIMIT (Siemens). Finally, first application experiences of this simulation system for the preparation of the SIS for the upcoming operation phase OP 1.2b of W7-X will be discussed.

Minioral:

Yes

Description:

Simulation for Control

Speaker:

Jörg Schacht

Institute:

MPI

Country:

Germany

519

Study on the Real-time Lossless Data Compression Method Used in the Readout System for Micro-pattern Gas Detector

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The data compression technology now is fully developed and widely used in many fields such as communication, multi-media, image information processing and so on. The large physical experiments, especially the ones with Micro-pattern Gas Detectors (MPGD), which always have many readout channels and have a lot of data to be transferred and saved, are however relatively seldom use this technology. In this paper, the real-time lossless data compression method is proposed for a general-purposed MPGD readout system. The lossless data compression can reduce the data transmission bandwidth of the system as well as keep all information of the data. The compression method discussed in the paper mainly consists of two steps. The first step is to pre-process the data according to different characteristics of different signals and the second step is to compress the pre-processed data using common lossless compression algorithm. Besides, the whole compression method is implemented in FPGA and is able to run real-timely. The system is then used to readout two different kinds of signals and the compression rate can reach as high as 43% and 30% respectively.

Minioral:

Yes

Description:

Micromega

Speaker:

Zhongtao Shen

Institute:

USTC

Country:

China

530

A Control System of New Magnet Power Converter for J-PARC Main Ring upgrade

Authors: Tetsushi Shimogawa[1]; Yoshinori Kurimoto[1]; Yuichi Morita[1]; Kazuki Miura[1]; Daichi Naito[1]

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Japan Proton Accelerator Research Complex (J-PARC) aims at achieving a MW- class proton accelerator facility. One of the promissing solutions for increasing the beam power in Main Ring (MR) is to shorten the repetition period from current rating of 2.48 second to 1.3 second in the future. We have a plan to replace and develop the power convereters of main magnets for this upgrade. Accoding to develop the new power converter, we develop the new control system. This control system consists combination of units for each functions, which are Programable Logic Controller (PLC), a main control board for the feedback system, a reference signal generator and gate pulse generators. Considering a reproducibility in the mass-production and the facilitation of improving the control algorithm, the digital control system is adopted. We will report the design of this control system and some test result with a small power converter.

Minioral:

No

Description:

Control

Speaker:

Tetsushi Shimogawa

Institute:

JPARC

Country:

Japan

660

566 Phase drift compensating RF link for femtosecond synchronization of E-XFEL

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566

Phase drift compensating RF link for femtosecond synchronization of E-XFEL

Author: Dominik Sikora[1]

Co-authors: Krzysztof Czuba [1]; Paweł Jatczak [1]; Maciej Urbanski [1]; Holger Schlarb [2]; Frank Ludwig [2]; Heinrich Pryschelski [2]

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Modern high-energy particle accelerators and free-electron lasers incorporate large quantities of sensitive RF and microwave frequency devices distributed over kilometer distances. Such devices require extreme stable phase and time synchronization by means of high frequency signal distributed along the accelerator facility.

Coaxial cables are commonly used to distribute the reference signal over the large machine to synchronize electronic systems and they are the main source of undesirable phase drifts in the synchronization system. Signal phase drifts in cables are mainly caused by temperature and humidity variations and their values usually exceed required phase synchronization accuracy by more than order of magnitude.

There are several approaches to reduce signal phase drifts in coaxial cables. This paper describes the realization of active phase stabilization system based on interference phenomenon. A phase-locked signal from the transmitter is reflected at the end of a coaxial cable link. Directional couplers placed along the cable pick up the forward and reflected signals and interfere them to cancel out the cable phase drifts. Distributed hardware including interferometer controller/transmitter and receiver modules were built demonstrate system concept and performance. Link input and output devices used FPGA I/O boards with Ethernet interface to control system operation. Specialized firmware and software was developed to calibrate and control the system.

This paper describes the concept of interferometer link, designed hardware, basic control algorithms and performance evaluation results. The link prototype was built to distribute 1.3 GHz signal through a coaxial cable. Measured phase drift suppression factor value exceeded level of 100.

Minioral:

Yes

Description:

Synch at fs level

Speaker:

Dominik Sikora

Institute:

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Country:

Poland

593

The DAQ for the single phase DUNE Prototype at CERN

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DUNE will be the world's largest neutrino experiment due to take data in 2025. Here is described the data acquisition (DAQ) system for one of its prototypes - ProtoDUNE-SP due to take data in Q4 of 2018. ProtoDUNE-SP also breaks records as the largest beam test experiment yet constructed, and is a fundamental element of CERN's Neutrino Platform. This renders ProtoDUNE-SP an experiment in its own right and the design and construction have been chosen to meet this scale. Due to the aggressive timescale, off-the-shelf electronics have been chosen to meet the demands of the experiment where possible. The ProtoDUNE-SP cryostat comprises two primary subdetectors - a single phase liquid Argon TPC and a companion Photon Detector. The TPC has two candidate readout solutions under test in ProtoDUNE-SP - RCE (ATCA-based) and FELIX (PCIe-based). Fermilab's artDAQ is used as the dataflow software for the experiment. Custom timing and trigger electronics and software are also described. Compression and triggering will take the ˜480 Gb/s of data from the front-end and reduce it sufficiently to 20 Gb/s bandwidth to permanent data storage in CERN's EOS infrastructure.
˜

Minioral:

No

Description:

DAQ for prototype

Speaker:

Karol Hennessy

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UK

681

432 Nuclear Pulse Charge Measurement with a Method of Time over Linear Threshold

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432

Nuclear Pulse Charge Measurement with a Method of Time over Linear Threshold

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Time over dynamic threshold (TODT) method, proposed in our previous work, has been successfully used for nuclear pulse charge measurement in PET detectors. It has advantages of strict linearity, large dynamic range, and better energy resolution, but requires a relatively complex circuit to generate specific dynamic threshold. In this paper, we propose to replace the dynamic threshold by a simpler linearly increasing threshold (called as TOLT method) with the aim to simplify the threshold generation circuit meanwhile maintaining its high energy resolution. Mathematical analysis on this replacement and the related realization circuit are presented. By energy spectrum measurement of PET detectors, the method is evaluated. The energy resolutions of PET detectors, composed of a PMT coupled with LYSO and LaBr3 crystal, are measured as 12.54% and 5.18% respectively, which is equivalent to the result obtained by TODT method. The test results show that the TOLT method is more practicable for charge measurement of nuclear detectors.

Minioral:

Yes

Description:

Analog Method

Speaker:

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USTC

Country:

China

658

560 Study of Retina Algorithm on FPGA for Fast Tracking

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560

Study of Retina Algorithm on FPGA for Fast Tracking

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Real-time track reconstruction in high energy physics experiments at colliders running at high luminosity is very challenging for trigger systems. To perform pattern-recognition and track fitting, artificial Retina or Hough transformation algorithms have been introduced in the field which have usually to be implemented in the state of the art FPGA devices. In this paper we report on two possible FPGA implementations of the retina algorithm: one using online Floating-Point core and one using Look-up Table and fixed-point representation. Detailed measurements of the performance on hardware designs, including latency, FPGA resource and physics performance are investigated and compared. So far the Retina has mainly be used in a detector configuration made of parallel planes, without or with small magnetic field. In this note we also report on the simulated performance in a detector configuration made of concentric detection layers with high magnetic field.

Minioral:

Yes

Description:

Fast Tracking

Speaker:

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Country:

Belgium

628

450 Longitudinal Mode-by-Mode Feedback System for The J-PARC Main Ring

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450

Longitudinal Mode-by-Mode Feedback System for The J-PARC Main Ring

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The J-PARC Main Ring (MR) is a high intensity proton synchrotron, which accelerates protons from 3 GeV to 30 GeV.
The MR delivers $2.4¥times10^{14}$ protons per pulse, which corresponds to the beam power of 470 kW,
to the neutrino experiment as of February 2017,
and the studies to reach higher beam intensities are in progress.
During studies, we observed the longitudinal dipole coupled-bunch instabilities in the MR for the beam power beyond 470 kW.
To mitigate them for higher beam intensities, we have developed the longitudinal mode-by-mode feedback system.
The feedback system consists of a wall current monitor, a FPGA-based feedback processor, RF power amplifiers, and a RF cavity as a longitudinal kicker.
In the feedback processor, we utilize the single sideband filtering technique to detect the oscillation components of the individual coupled-bunch mode in the beam signal.
We present the design of the feedback system, especially the design detail of the digital filters in the feedback processor.
We also report the preliminary beam measurement results for evaluation of the system performance on detection and excitation of the selected modes.

Minioral:

Yes

Description:

Algorithm feedback

Speaker:

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Country:

Japan

654

543 Development and Characterization of a 3.2 Gb/s Serial Link Transmitter for CMOS Image Sensors Data Transmission in Subatomic Physics Experiment

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543

Development and Characterization of a 3.2 Gb/s Serial Link Transmitter for CMOS Image Sensors Data Transmission in Subatomic Physics Experiment

Author: Quan Sun[1]

Co-authors: Guangyu Zhang [2]; Datao Gong [3]; Binwei Deng [4]; Wei Zhou [5]; Bihui You [5]; Le Xiao [5]; Jian Wang [6]; Dongxu Yang [2]; Tiankuan Liu [3]; Chonghan Liu [1]; Di Guo [5]; Jun Liu [5]; Christine Hu [7]; Frederic Morel [8]; Isabelle VALIN [9]; Xiangming Sun [10]; Jingbo Ye [11]

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A serial link transmitter for CMOS image sensors in subatomic physics experiment is developed. It encodes 256-bit/10 MHz payload with two interleaved RS(31, 27) codes and transmits serialized data with a CML driver at 3.2 Gb/s data rate. With the RS codes, at most 4 symbols in the transmission could be corrected, corresponding to a 20-bit consecutive bits error. A charge-pump PLL generates 1.6 GHz clock for DDR operation from a 40 MHz reference. Pre-emphasis is employed in the transmitter, enabling serial data to be transmitted over low mass cables. Digital blocks are triplicated to resist SEU. The proposed transmitter has been fabricated in a 0.18 μm CMOS technology. A preliminary measurement gives a frame data rate of $3 \cdot 10^{-12}$ with a confidence level of 94.5%, corresponding to a BER for the payload of $1.2 \cdot 10^{-12}$ with a confidence level of 94.9%. The power consumption of the transmitter is 135 mW at a typical setting. It was irradiated to 4.5 Mrad(SiO_2) and no functionality degrading is observed. SEU measurement will be carried out and reported in the conference.

Minioral:

Yes

Description:

Speaker:

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Country:

China

675

419 A data transmission system for the phase contrast X-ray human computed tomography prototype

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419

A data transmission system for the phase contrast X-ray human computed tomography prototype

Author: rongqi sun[1]

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Theoretically, the cross section of X-ray phase shift caused by these low-Z elements is at least three orders of magnitude higher than the absorption. Thus the phase contrast X-ray imaging can offer better imaging contrast. A low-dose, large vision field and high phase contrast human CT prototype based on three-grating interferometry is in development by NSTL (national synchrotron radiation laboratory Hefei).
To achieve 200mm*200mm vision field, 43 detector boards are adopted in this prototype. Each detector board has 384 channels with 20 bit resolution. The acquisition starts once every 1.25ms, which means the total bandwidth is more than 250Mbps. Furthermore, as a spiral scanning device, the data of all detectors should be transferred form the rotator to the stator. Given all that, a data transmission system is designed to meet the data transfer requirement of this porotype.
The data transmission system proposed in this paper contains two parts: three Data Collection boards (DCB) mounted on the rotor of the slip ring and one data transmission board (DTB) on the stator. All data from the detectors are cached into the DDR3 memory chip. Two small form pluggable (SFP) modules on the DCB and DTB respectively realize the data transmission from the rotor to the stator.
The test result shows that this system can meet the requirement of data transmission for this prototype. We use this system to test the performance of 43 detectors successfully. This data transmission structure can be a guidance for similar device.

Minioral:

Yes

Description:

Algo

Speaker:

rongqi sun

Institute:

USTC

Country:

China

556

Survey and Test Environment for ITER EPP#12 Electrical Components

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The purpose of Equatorial Port Plug 12(EPP#12) is to provide common platform, support/container for five diagnostic plant systems and one glow discharging cleaning system(GDC). As port integrator, a team from Institute of Plasma Physics Chinese Academy of Sciences(CASIPP) performs the design work. The Instrument and Control(I&C) is an important part of system design. The main I&C functions will be implemented include temperature measurements of the port structures, electrical heater with temperature control during baking of windows and providing spare input measurement channel. The integrator should provide the embedded temperature sensors, associated cabling, electrical connectors and electrical feedthrough. Most electrical components will be deployed in port plug structure which Vacuum Quality Classification (VQC) is VQC1A, the highest level. All the electrical components in port plug structure should have high vacuum compatible and compliant to ITER Vacuum handbook. In this paper, we present the survey and research of electrical components for ITER EPP#12. And the design and implement of a test environment for electrical components which is based-on ITER CODAC is also described.

Minioral:

Yes

Description:

Speaker:

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China

392

Bonds for detection of very inclined “old” shower due to anti-aliasing filter in the Pierre Auger surface detector data acquisition system

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At large zenith angles the slant atmospheric depth to the ground level
is sufficient to absorb the early part of the shower that follows from
the standard cascading interactions, both of electromagnetic and hadronic type.
Nucleon induced showers are initiated at the top of the atmosphere.
For very inclined showe only muons
in showers survive. The fronts of deeply penetrating muon
showers have only a small longitudinal extension, which leads to short
detector signals. “Old”showers generate short traces of very similar shapes
at all core distances.

Inclined showers mainly composed of muons, allow a direct measurement of the muon content at ground level and as a consequence, they can be used to study mass composition and to test high-energy hadronic interaction models. The Pierre Auger Observatory is particularly well suited for the detection of inclined showers because the water Cherenkov tanks used for the surface detector act like volume detectors.

The standard data acquisition system quantizing the analog signals in ADCs, according to the “Golden rules”, is equipped with the anti-aliasing filter with the cut-off Nyquist frequency. However, very short pulses, typical for very inclined showers, are significantly suppressed by the anti-aliasing filter and their amplitude may be not enough to generate the 3-fold coincidence trigger.

The paper presents the theoretical analyses of the anti-aliasing Auger filter response as well analyses of measured Auger data. We conclude that for a detection of non-standard rare events maybe it is worth considering non-standard approach and resign with the standard Golden rules.

Minioral:

Yes

Description:

Anti-alias filter

Speaker:

Zbigniew Szadkowski

Institute:

University of Lodz

Country:

Poland

582

Development of a multichannel FPGA based high resolution Time-to-Digital Converter

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Time-of-Flight measurement is a powerful tool to distinguish particles in nuclear and hadron physics experiments. For such purpose, a low cost, multichannel and high resolution of better than 30 ps time to digital converter (TDC) is needed. In this work, a multichannel TDC is implemented in Xilinx Kintex-7 (XC7K160T-1).
The TDC employs tapped delay line (TDL) for fine time measurement. Each TDL is composed of a carry chain with 160 taps and measures both leading edge and trailing edge at sampling frequency of 625 MHz. The dead time of the measurement is 2 cycles of the sampling frequency (i.e. 3.2 ns). Auto calibration logic of the bin width is implemented with cascaded PLL and block RAM. The typical bin width is 11 ps. The measurement range is extended by a clock count based coarse time measurement up to 100 us. Time window matching sequence selects a valid hits in the specified time window. For data readout, 1 Gbps TCP/IP protocol based on SiTCP is used. The firmware is implemented with

Vivado 2017.4 for a demostrator module. The detail of the firmware design including floor planning and performance test will be presented.

Minioral:

Yes

Description:

FPGA-TDC

Speaker:

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Country:

Japan

434

Development of next generation LLRF control system for J-PARC rapid cycling synchrotron

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The low level rf (LLRF) control system for the rapid cycling synchrotron of the Japan Proton Accelerator Research Complex (J-PARC) started its operation in 2007. The key functions of the LLRF control system are the dual harmonic auto voltage control, which generates superposed voltages of the fundamental accelerating harmonic and the second harmonic in a single wideband magnetic alloy (MA) cavity, and the multiharmonic rf feedforward to compensate the beam loading in the MA cavity caused by high intensity beams. These functions are necessary to accelerate high intensity proton beams. The system has been working well without major problems for more than ten years. However, the old FPGAs (Xilinx Vertex-II pro etc.) are discontinued and not supported by the current development environment. It will be difficult to maintain the system in near future. Thus, we are planning to replace the existing VME-based LLRF control system with a new MicroTCA.4 based system. The system controls twelve cavities independently and calculates vector sum of the cavity voltages in real time for phase feedback.. Signal and data transfer between the modules is a key to realize the functions. In the existing system, the transfer is implemented not only the backplane but also serial link via cables between the VME modules. It is much more simplified in the new system thanks to the high speed communication capability of the MTCA.4 backplane. In this presentation, we present the configuration of the system under development, the implemented functions, and preliminary test results.

Minioral:

Yes

Description:

system

Speaker:

Fumihiko Tamura

Institute:

JPARC

Country:

Japan

420

Real-time Local Noise Filter in 3D Visualisation of CT Data

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[3] *Technische Universitaet Darmstadt*

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X-ray computed tomography (CT) imaging allows biologists to study the internal structure of living organisms with high spatial and temporal resolution. To control the flow of experiment, the online data visualisation is highly desirable. However, the noise inherent to the tomographic setup deteriorates the visual output preventing users from identifying the features. The problem is further complicated by a narrow dynamic range of the produced tomographic data that prevents simple greyscale thresholding approaches. On the other hand, the iterative approaches are not suitable for online visualisation due to slow speed and parametrisation. In this talk, we present a real-time visualisation service that provides a fast image preview during the data acquisition stage. Our approach suppresses the noise by a modified mean filter approach. To detect noise, we average nine uniformly distributed sub-regions: one central sub-region and eight diagonally spread sub-regions. Each sub-region averages its six adjacent neighbouring voxels. The resulting average (average of 9 sub-regions) is subjected to the Otsu threshold where a value lower than the threshold is treated as noise. To evaluate the efficiency of our filter, we compare against four other local filters regarding entropy and processing time. The results demonstrated significant improvement of the visual quality with processing time still within the millisecond range.

Minioral:

Yes

Description:

Algo

Speaker:

Nicholas Tan Jerome

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KIT

Country:

Germany

390

Detection of Weak Near-Infrared Signal Based on Digital Orthogonal Vector Lock-in Amplifier

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Co-authors: Yi-hao Zhang ; Shu-cheng Dong ; Jin-ting Chen ; Feng-xin Jiang ; Zhi-yue Wang ; Ya-qi Chen ; Hong-fei Zhang ; Jian Wang

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A near-infrared (NIR) measurement based on digital orthogonal vector lock-in amplifier (LIA) is present in this paper. NIR sky background radiation is very weak. To detector the signals obscured by noise, the best way achieved is to use a chopper to modulate the detected signal and using a LIA to demodulate. The effect of 1/f noise of detector, dark current and other noises can be reduced to get sufficient signal-to-noise ratio (SNR). The orthogonal vector LIA can avoid the phase shift on the accuracy of measurement by two orthogonal components. In order to simplify the system, a digital algorithm is adopted to realize the LIA which is operated in a microcontroller with ARM cortex-M4. Data is obtained through ADC and the detector signal is amplified and filtered. Then the phase sensitive detection (PSD), low-pass filter (LPF) and amplitude phase calculation are performed. The digital method can greatly simplify the circuit, and conveniently adjust the time constant of the LPF to realize the different equivalent noise bandwidth (ENB). The algorithm has the specification of high precision, flexible usage, simple implementation and low computation resource. By using this method, the weak infrared signal submerged by the noise can be obtained, which extremely improves the detection capability of the system.

Minioral:

No

Description:

Method/HW

Speaker:

Qi-jie Tang

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Country:

China

510

The Large Synoptic Survey Telescope Data Acquisition System

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The Large Synoptic Survey Telescope Camera (LSSTCam) will be the largest digital camera ever constructed for astronomy. Containing 189 16-megapixel science sensors, it will produce volumes and rates of data more commonly found in large particle physics detectors than astronomical instruments. However, there are features that make the design of the LSSTCam DAQ uniquely challenging.

The 142 high-speed serial links must penetrate a cryostat in limited space. Client machines will connect to an Ethernet, extended with a Dense Wavelength Division Multiplexing (DWDM) 100 km. The image data must be buffered for multiple days within the DAQ system allowing operations to proceed in the absence of a connection to the base facility. Each of the 3.2-gigapixels will be read out with 18-bit accuracy. When observing, an image will be acquired every 15 seconds. The image will be transferred in no more than 2 seconds. This results in a peak data rate of 3.6 gigabytes/second. The core portion of the DAQ hardware is a 14-slot ATCA shelf containing 112 processing nodes, 288 channels of 3.125 Gbps serial links, 240 solid state drives, and 112 external 10G Ethernet connections for client machines. Prototypes of all hardware have been built and are in use by LSSTCam subsystems for development. Construction of the production system is ongoing.

Minioral:

Yes

Description:

General DAQ

Speaker:

John Gregg Thayer

Institute:

SLAC

Country:

USA

611

SHIELDS-1, The First NASA Langley Research Center Materials Small Satellite

Part of NASA Langley's pioneering research and development has been with materials and structures with multiple historical contributions. NASA Langley has led space technology development of materials with space experiments.

Minioral:

Description:

Speaker:

Institute:

Country:

407

The Electronics Design of Error Field Feedback Control System in KTX

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KTX (Keda Tours eXperiment) is a new RFP (reversed field pinch) device at the University of Science and Technology of China. The unique double-C design of the KTX makes modifications and investigations of power and particle control easy, but the error field of slit zone in the new design should not be neglected. The objective of this paper is to introduce a new active feedback control system which can change the voltage between the unique double-C structures to make the toroidal field better. FPGA is the central part of the whole system to control all the process, because it can manipulate and transmit the data from coils in real time. There are 2 high-speed 8-channels ADCs in the system to convert the analog signal from 16 Rogowski coils which can detect dynamic eddy current of copper shells near the vertical gap. FPGA also control the external power amplifier to change the voltage between the unique double-C structures by commanding 16 high-speed DACs to give the RFP device a feedback. Result indicated that the error field in KTX device was reduced, and the system could successfully achieve fast matrix calculation with lower delay.

Minioral:

Yes

Description:

feed-back control

Speaker:

Xu Tianbo

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Country:

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538

The Use of Java in Online Event Building and Recording at Jefferson Lab

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The CODA data acquisition software at Jefferson Lab uses Java extensively. In particular, we used Java to code the distributed event builder and event recorder. Although Java is not generally regarded as real-time software, we have taken advantage of several techniques that allow the event builder to handle the data rates being produced by the front end. In this paper, we describe these techniques and discuss the relative merits of using the Java language in this context.

Minioral:

Yes

Description:

JAVA for EB

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700

538 The Use of Java in Online Event Building and Recording at Jefferson Lab

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401

Two FPGA Case Studies Comparing High Level Synthesis and Manual HDL for HEP applications

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Real time data acquisition systems in nuclear science often rely on high-speed logic designs to reach the fast data rate requirements. They are mostly coded in a hardware description language (HDL). However, in recent years, so-called high level synthesis (HLS) software has appeared, some with the notable advantage that they rely on the widespread C/C++ syntax. This paper's aim is to outline differences between HDL and C++ HLS based designs for two real time data acquisition modules used in nuclear science. The first module is a real time crystal identification module, and the second is a compact event timestamp sorting module.
For the crystal identification module, both HDL and HLS versions have the same event processing interval, and the HLS implementation consumes twice as many lookup tables and flip flops as the HDL version. On the other hand, the HLS version took half the time to write and debug. For the sorter module, the HLS version requires about 3 to 4 times more logic resources, with a slightly longer interval. The challenge for this module is that some pipeline shortcuts cannot be automatically inferred from simple C++ and must be explicitly written in. This second HLS module was also completed in half the time compared to the original HDL code. While not intuitively applicable to all problem

types, HLS is nonetheless a compelling alternative to custom HDL or Verilog implementations for real time systems in nuclear and plasma science.

Minioral:

Yes

Description:

HDL code

Speaker:

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USA

575

The LHCb DAQ system for the LHC Run3.

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In order to optimise its physics reach in the LHC Run3, for the years 2020 and beyond, the LHCb Collaboration decided to re-optimise the detector and the data acquisition system. The new detector will operate at the LHC bunch-crossing frequency of 40˜MHz, without a first level hardware trigger. The implementation of the data-acquisition and of the online computing system for the software trigger are challenging, since of the expected data rate to manage amounts to about 40˜Tb/s.The system can be built at an affordable cost only by using of-the-shelf hardware as much as possible. However, technologies available evolve very quickly, thus the system architecture has to be flexible enough to avoid too strong bounds to a specific technology, and let us free to choose it until the last moment. We present the system architecture, the different implementation options we are studying along with measurements from these studies and will explain the decision criteria and technology drivers for choosing the components for the final system.

Minioral:

No

Description:

DAQ

Speaker:

Umberto Marconi

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Country:

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551

Lessons learned from commissioning and first colliding beam data of the Belle II imaging Time Of Propagation Detector

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While the imaging Time Of Propagation (iTOP) subdetector of the Belle II experiment was installed in May, 2016, the commissioning and operation of this complex detector has been a challenge. This novel readout consists of 64 independent "board stacks", each of which contains 128 channels of precision single-photon timing readout. To accomplish this sixteen 8-channel IRSX ASICs and mounted on 4 carrier cards along with a Zynq-7 FPGA. These 4 FPGAs communicate of dedicated gigabit links to a master Zynq-7 FPGA mounted on a so-called SCROD, or master control card, along with a large DDR RAM for holding calibration constants. Both the logic and processor cores are used to provide on-the-fly pedestal subtraction and precision timing feature extraction. Timing, trigger and data are provided by Belle II standard fiber optic link (Belle2link) and custom programming and trigger/timing distribution (FTSW). Performance results from final global cosmic ray running and first collision data will be presented. Particular emphasis will be placed on problems encountered and lessons learned.

Minioral:

No

Description:

Lesson Learned

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Country:

USA

666

604 Management Software and Data Exchange Protocol for the INFNLNS Accelerators Beamlines

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604

Management Software and Data Exchange Protocol for the INFNLNS Accelerators Beamlines

Authors: Gianfranco Vecchio[1]; Luigi Cosentino[2]; Sara Rita Pulvirenti[3]; E. Furia[4]; S. Cavallaro[4]; B. Diana[4]; S. Aurnia[4]

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My presentation will describe the design and the development of an innovative management software for the accelerators beamlines at INFN-LNS. The Graphical User Interface, the data exchange protocol, the software functionality and the hardware will be illustrated.
Compared to traditional platforms for the accelerators console, at INFN-LNS we have developed a new concept of control system and data acquisition framework, based on a data structures server which so far has never been used for supervisory control.
We have chosen Redis as a highly scalable data store, shared by multiple and different processes. With such system it is possible to communicate cross-platform, cross-server or cross-application in a very simple way, using very lightweight libraries.
A complex and highly ergonomic Graphic User Interface allows to control all the parameters with a user-friendly interactive approach, ensuring high functionality so that the beam operator can visually work in a realistic environment.
All the information related to the beamline elements involved in the beam transport, can be stored in a centralized database, with suitable criteria to have a historical database.

Minioral:

Yes

Description:

Controls Software

Speaker:

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651

531 LHCb full-detector real-time alignment and calibration: latest developments and perspectives

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531

LHCb full-detector real-time alignment and calibration: latest developments and perspectives

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A key ingredient of the data taking strategy used by the LHCb experiment at CERN in Run-II is the novel real-time detector alignment and calibration. Data collected at the start of the fill are processed within minutes and used to update the alignment, while the calibration constants are evaluated hourly. This is one of the key elements which allow the reconstruction quality of the software trigger in Run-II to be as good as the offline quality of Run-I. The most recent developments of the real-time alignment and calibration paradigm enable the fully automated updates of the RICH detectors' mirror alignment and a novel calibration of the calorimeter systems. Both evolutions improve the particle identification performance stability resulting in higher purity selections. The latter leads also to an improvement in the energy measurement of neutral particles, resulting in a 15% better mass resolution of radiative b-hadron decays. A large variety of improvements has been explored for the last year of Run-II data taking and is under development for the LHCb detector upgrade foreseen in 2021.These range from the optimisation of the data samples selection and strategy to the study of a more accurate magnetic field description. Technical and operational aspects as well as performance achievements are presented, focusing on the new developments for both the current and upgraded detector.

Minioral:

Yes

Description:

Trigger

Speaker:

Dorothea Vom Bruch

Institute:

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Country:

Switzerland

454

Online track reconstruction on GPUs for the Mu3e and LHCb experiments

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As the data rate produced by modern particle physics experiments increases, the demands on the computing performance of data selection processes grow. Therefore, Graphics Processing Units

(GPUs) are being considered for this task. This talk focuses on their use in the online event selection for the Mu3e experiment and within studies of track reconstruction for the LHCb experiment.

The Mu3e experiment searches for the lepton flavour violating decay $\mu \to e^+e^-e^+$ by using a silicon tracking detector. During the first phase of the experiment, 10^8 μ/s will be available, resulting in a data rate of ˜10 GB/s, which needs to be reduced by at least a factor 100. Within the signal selection process running on a GPU, the helical tracks are fitted with a 3D fit optimized for multiple scattering dominated resolution, and vertices are defined based on simple geometric criteria. With this algorithm, 98% of signal decays are selected, while reducing the data rate by a factor of 140. On an Nvidia GTX1080Ti GPU, a throughput rate of 2×10^6 events/s has been measured using simulated data, so the selection process can run on the hardware planned for the experiment.

The LHCb experiment is designed to study the decay of B hadrons at the LHC. Beginning in 2020, the first trigger level, implemented in software, will have to reduce the event rate of 30 MHz by at least a factor 30. To meet this demand, possibilities on GPUs are being explored and preliminary results of such studies will be shown.

Minioral:

Yes

Description:

GPU reconstruction

Speaker:

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Institute:

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Country:

Switzerland

599

Real time data access log analysis system of EAST tokamak based on spark

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The experiment data generated by the EAST device is getting larger and larger, and it is necessary to monitor the MDSplus data storage server on EAST. In order to facilitate the management of users on the MDSplus server, a real-time monitoring log analysis system is needed. The data processing framework adopted by this log analysis system is the Spark Streaming framework in Spark ecosphere, whose real-time streaming data is derived from MDSplus logs. The framework also makes use of key technologies such as log monitoring, aggregation and distribution with framework likes Flume and Kafka,which makes it possible for MDSplus mass log data processing power.The system can process tens of millions of unprocessed MDSplus log information at a second level, then model the log information and display it on the web.This report introduces the design and implementation of the overall architecture of real time data access log analysis system based on spark.Experimental results show that the system is proved to be with steady and reliable performance and has an importanl application value to the management of fusion experiment data.

Minioral:

No

Description:

Speaker:

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Country:

China

615

387 A programmable clock generator for automatic Quality Assurance of LOCx2

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399

Design of remote control software of near infrared Sky Brightness Monitor in Antarctica

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The Near infrared Sky Brightness Monitor(NISBM) aims to measure near infrared sky background of Kunlun station in Antarctic. NISBM mainly consists of an InGaAs detector with TEC cooling, a chopper and a scanning mirror. The scanning mirror can be controlled to rotate to scan the sky from 0°to 180°. Electromechanical control and weak signal readout functions are accomplished by the same circuit system.

Considering the harsh environment in the Antarctic, a multi-level remote control software system is designed and implemented using EPICS and WEB-based infrastructure. EPICS IOCs are developed to control each hardware module independently via serial port communication with the STM32 microcontroller in DAQ board of NISBM. The Tornado web framework and PyEpics are also introduced in the Web-based infrastructure. As a client of the EPICS framework, PyEpics is used to monitor or change the EPICS Process Variables. Tornado is responsible for the specific operation process of inter-device collaboration, and expose interfaces to the user interface to make calls. To realize automatic observation, a set of xml-based configuration format is designed and observers can make own observation plan using this format. The back-end of Tornado is designed as master-and-agent architecture. The master and agent nodes communicate with each other through the web-socket protocol, so multiple agent nodes can be deployed.

The GUI is implemented in the form of single-page application using Vue which communicates with

Tornado through WebSocket and AJAX request. The web page integrates device control, data curve drawing, alarm display, auto observation and other functions together.

Minioral:

No

Description:

EPICS

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China

391

The operational and control software of Multi-channel Antarctic Solar Telescope

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MARST (Multi-channel Antarctic Solar Telescope) aims to observe the Sun in multiple wavebands at Antarctic. It will be the Chinese first Solar telescope in Antarctic. The telescope has two tubes, corresponding to Photosphere observation which uses 11 filters and Chromosphere observation in Hα waveband. We need to coordinate two tubes to observe at the same time. The telescope will observe the Sun for a long time which needs, so we also need a self-guiding module to improve tracking precision. Besides, performing solar specific flat-field exposure is necessary for analyzing. EPICS is introduced to control each hardware and an autonomous observation system based on RTS2 is designed under such demands.
We wrote EPICS application modules is developed for each device: telescope mount & focuser, filter wheel, Hα filter, dome with webcam, Andor CCD and PI CCD. We also integrated EIPCS modules into RTS2 framework with an XML configuration. To control these applications autonomously we developed an rts2 executor module is developed. In the executor, two plan classes are instantiated to control two sets of filters and CCDs, and ensure only one could control the mount at the same time. Different types of plan are designed to describe different series of process with different priority. For example, flat-field plan is performed in higher priority. To improve tracking precision, we calculate centroid of each image to get the offset, then apply the correction to the telescope during observation process.

Minioral:

Yes

Description:

Multi-channel Antarctic Solar

Speaker:

Jian Wang

Institute:

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Country:

China

387

A programmable clock generator for automatic Quality Assurance of LOCx2

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The ATLAS Liquid Argon Calorimeter (LAr) Phase-I trigger upgrade requires high-speed, low-latency data transmission to read out the LAr Trigger Digitizer Board (LTDB). A dual-channel transmitter ASIC LOCx2 have been designed and produced. In order to ensure all the LOCx2 chips behave properly, a Quality Assurance have to be conducted before assembly. The problem I am trying to solve in this project is to yield a clock signal with continuously adjustable frequency and phase offset to generate and control an eye diagram for the QA. By configuring the registers of an any-frequency generator IC, Si5338, the clock signal whose frequency range from 5Mhz to 200Mhz have been properly produced. For the purpose of further development, a C-language based DLL which packs up the function of adjusting frequency and setting phase offset was designed and built , and several evaluation was perform to ensure the robustness. It is a programmable clock generator with the interface –USB and easy to be integrated a test setup system. Through programming, the frequency of clock generator can be configured and changed in real time and integrated to an automatic test program.

Minioral:

Yes

Description:

clock

Speaker:

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Country:

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516

Trigger Selection System for CBM-TOF Super Module Quality Evaluation

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The Compressed Baryonic Matter-Time of Flight (CBM-TOF) wall uses high performance of Multi-gap Resistive Plate Chambers (MRPC) assembled in Super module (SM) detectors to identify charged particles with high channel density and high measurement precision at the Compressed Baryonic Matter (CBM) experiment. During the mass production, the quality of each SM should be evaluated. For the convenience of testing and analyzing the MRPCs, a conventional frontend triggered mode is adopted for the evaluation system. In this triggered system, a global trigger signal should be generated to select the effective data from the raw hit data buffer. In this paper, a hierarchical trigger selection system for quality evaluation of the CBM-TOF SM detector is presented. In the first state, the Time-to-Digital Converter (TDC) draws effective hit information from the detectors, and then transfers them to the TDC readout motherboard (TRM). Where the hits collected from TDC are further processed in to generate sub-trigger information. In the second state, TRMs transfers all the sub-trigger information to trigger module (TM) allocated in a PXI 6U crate through optical links. With a proper selection algorithm, a global trigger signal is finally generated, which is then distributed synchronously to each front digitizer channel for trigger match. Test results confirm the function of the trigger selection system and indicate that it can works well.

Minioral:

No

Description:

Trigger

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686

461 Prototype of Front-end Electronics for PandaX-4ton Experiment

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461

Prototype of Front-end Electronics for PandaX-4ton Experiment

Authors: Shuwen Wang[1]; Zhongtao Shen[2]; Keqing Zhao[2]; Changqing Feng[2]; Shubin Liu[2]

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At the China Jinping Underground Laboratory, the PandaX-4ton (Particle AND Astrophysical Xenon phase IV) in planning is a dark matter direct detection experiment with dual-phase Xenon. PandaX-4ton, compared to PandaX-II, has more readout channels and higher time precision requirements. Once incoming WIMPs (Weakly Interacting Massive Particles) collide with Xenon atom, prompt scintillation photons (S1) and delayed electroluminescence photons (S2) are collected by the PMTs, and then fed into front-end electronics which are introduced in this paper. In order to precisely obtain the wave and time information carried by the PMT signals, and to maximally cover the signal dynamic range, a high-gain preamplifier and an eight-channel digitizer with 14-bit resolution and 1 GSps sampling rate have been designed. Besides, the clock synchronization circuit within the digitizer is well-designed to align all the PMT channels. The digitizer also contains gigabit fiber to exchange data with trigger and data acquisition system. The performance of the front-end electronics can meet the requirements for the PandaX-4ton.

Minioral:

Yes

Description:

FE board

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626

443 Scanning Test System of p/sFEB for the ATLAS Phase-I sTGC Trigger Upgrade

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443

Scanning Test System of p/sFEB for the ATLAS Phase-I sTGC Trigger Upgrade

Author: Xinxin Wang[1]

Co-authors: Feng Li [2]; Peng Miao [3]; Shengquan Liu [1]; Zhilei Zhang [1]; Shuang Zhou [1]; Tianru Geng [4]; Ge Jin [4]

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The ATLAS detector which is one of the four experiments at Large Hadron Collider will fulfill Phase-I upgrade to extend the frontier of particle physics. The upgrade will replace the inner detector (Small Wheel, SW) of the end-cap muon spectrometer with the "news mall wheel"detector (NSW), which consists of the Small-strip Thin Gap Chamber(sTGC) and Micromegas (MM). The Pad Front End Board (pFEB) on sTGC is developed to gather and analyze pads trigger. The Strip Front End Board (sFEB) is developed to accept the pad trigger to define the regions-of-interest for strips readout. About 2000 p/sFEBs will be produced for final delivery and engineering backup. Before the p/sFEBs are mounted on the detector, we need to test the performance of all the p/sFEBs. The performance testing of each p/sFEB includes baseline test, threshold DAC calibration, internal test pulse DAC calibration, gain test and dead channel test, each of which are very important for the front-end electronic system. Therefore, the scanning test system is designed according to the test requirements of the p/sFEB. In this test system, a simulation signal board is developed to generate different types of signal to the p/sFEB. PC software and FPGA XADC cooperate to achieve the scan test of analog parameter. The PC software is written based on Qt platform using the standard C++. The automatic test function of the pFEB has been successfully realized. This system has the advantages of convenient GUI, smooth operation, convenient user operation and good stability.

Minioral:

Yes

Description:

DAQ Board

Speaker:

Xinxin Wang

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China

712

585 Design and test of sTGC front-end electronic interface board

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585

Design and test of sTGC front-end electronic interface board

Author: Xu Wang[1]

Co-authors: Jinhong Wang [1]; Liang Guan [2]; Xiong Xiao [1]; Junjie Zhu [1]

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Small-strips Thin Gap Chamber(sTGC) is one of the detectors on new small wheel(NSW) which is an important part of Atlas Phase-I upgrade. We will present our design and test results for the sTGC front-end electronic interface board, which aims to demonstrate the functionality and interface of ASICs on the sTGC front-end board. VMM, TDS(Trigger Data Serializer), SCA(Slow Control Adapter) and ROC(Read-out Controller) are the new ASICs designed for sTGC, which has complex functions and massive ports. The sTGC front-end ASICs interface board provides us a good chance to study and understand the configuration, function test and data transition of these ASICs, find potential problems and gain experience. On the other hand, due to the output of TDS has a speed of 4.8Gbps, which requires the jitter clean clock, the interface board has SMA test point for both the input clock and the clock output of ROC in order to validate the clock jitter. The interface board also have the same connectors so it can be connected to other electronics to demonstrate the performance of high speed output with long cables.The studies on the interface board will provide us chances to understand the performance of the sTGC front-end ASICs and give feedback to the ASIC design and guidance for the design of the final sTGC front-end boards.

Minioral:

Yes

Description:

STGC DAQ board

Speaker:

Xu Wang

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University of Washington

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USA

564

Upgrade of the Analog Integrator for EAST Device

Authors: Yong Wang[None]; Zhenshan Ji[1]; Shi Li[None]; Zhanghou Xu[2]; Zuchao Zhang[1]; Feng Wang[None]

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Integrators are fundamental instruments to recover differential signals from magnetic probes in Experimental Advanced Superconducting Tokamak (EAST) experiments. While previous analog integrators are single-ended input, which has low common mode rejection ration (CMRR), a kind of difference integrator is introduced which has the same structure as the standard difference amplifier. The linear fitting method is used to determine the effective drift slope, which is used to rectify the integration signal in real time. To improve the maintainability and testability of the integrator system, a new integrator controller was developed, which uses an ARM micro-controller and the lightweight IP protocol stack to realize the network control. The tests show that the upgrade integrator works well, its CMRR is high up to 125 dB when the common voltage is 1.5 V, and the processed integration drift is less than 200 uVs during 1000 s integration, which is much better than the previous integrator.
Key words: integrator; CMRR; drift; ARM

Minioral:

No

Description:

HW DAQ

Speaker:

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Country:

China

452

An FPGA Based Fast Linear Discharge Method for Nuclear Pulse Digitization

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Inspired by Wilkinson ADC method, we implement a fast linear discharge method based on FPGA to digitize nuclear pulse signal. In this scheme, we use a constant current source to discharge the charge on capacitor which is integrated by the input current pulse so as to convert the amplitude of the input nuclear pulse into time width linearly. Thanks to the high precision of TDC measurement that we have achieved in FPGA, we can increase the current value of the discharge to make the discharge time short, so as to obtain a small measurement of dead time. We has realized a single channel fast linear discharge circuit which contains only one dual supply amplifier, two resistors and one capacitor. The rest part can be implemented in an FPGA (Field Programmable Gate Array). Leakage current from the sensor would cause the base line drifting slowly, which can influence the measuring precision. Our method solve this problem without losing the linearity of measurement. We have built the circuit and experimental setup for evaluation. Using them to measure energy spectrums of PET detectors of PMT coupled with LYSO and LaBr3 crystal, the energy resolution is 12.67% and 5.17% respectively. The test results show that our circuit is rather simple, stable and conducive for multi-channel integration.

Minioral:

Yes

Description:

Algo Wilkinson ADC

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Country:

China

440

Study on timing performance of a readout circuit for SiPM

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In recent years, SiPM photoelectric devices have drawn much attention in the domain of time-of-flight-based Positron emission tomography (TOF-PET). Using them to construct PET detectors with excellent coincidence time resolution (CTR) is always one of research focus. In this paper, a SiPM readout pre-amplifier based on common-base current amplifier structure followed by a Pole-Zero (PZ) compensation network is constructed, and the main factors that affect the timing performance of the PET detector are investigated. By experimental measurement, we found that the CTR is heavily related to the bandwidth of the amplifier, bias voltage of SiPM, comparator threshold, and PZ network parameter. The test setup has two detectors, one with LYSO crystal (3 mm x 3 mm x 10 mm) coupled with a Hamamatsu SiPM (S12642-0404), and the other with LaBr3 coupled to a PMT-R9800. After the optimization of the readout circuit with related factors, the CTR between the two detectors is measured as 266ps FWHM. The test result is a helpful guideline for the readout ASIC chip design in our next step.

Minioral:

Yes

Description:

SiPM timing

Speaker:

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672

415 Design of Readout Electronics for CEPC Semi-Digital Hadronic Calorimeter Pre-research

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415

Design of Readout Electronics for CEPC Semi-Digital Hadronic Calorimeter Pre-research

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This research is intended to provide a feasible readout system for high granular Semi-Digital Hadronic CALorimeter (SDHCAL) in the proposing high energy Circular Electron Positron Collider (CEPC). A system including readout pads array, Front-end Electronics Board (FEB) and Detector InterFace (DIF) board is designed and fully tested. This system is applied on a double layers GEM detector. The effective area of GEM detector is 30cm $\times$ 30cm with the readout segment sized 1 cm$\times$1cm. The FEB is equipped with low consumption daisy-chained chips named MICROROC (MICRO-mesh gaseous structure Read-Out Chip). The DIF board is in charge of slow control distribution and data transmission. An auto test method is developed to calibrate the system quantitatively. As a result, the RMS noise of the system is below 0.35fC. The dynamic range is up to 500fC and the gain variation is better than 1% among channels. Cosmic-ray test shows the crosstalk between neighboring pads is less than 1.5%. The results obtained with small size detector show that the scheme is successful and can be applied on the large sized GEM detector readout.

Minioral:

Yes

Description:

system

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Yu Wang

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Country:

China

435

DepFET Movie Chip (DMC) - enabling ultra high speed mega pixel full frame data acquisition for the DepFET direct electron detector (EDET DH80K) system

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Based on the technology of the pixel detector (PXD) at the Belle II experiment @KEK/Japan a direct electron detector system was developed for time-resolved imaging applications. It consists of four two-side buttable all silicon modules (512x512 pixels each) capable to capture full frame images in a burst mode with up to 100 pictures @80k frame rate.
To realize the necessary 26Mbit memory for the local frame storage array and the sequencer memories under the tight space conditions a TSMC 40nm technology was chosen.
To send out the captured picture data sets to the following DAQ, up to 8 middle speed serial links and a cross bar switch like routing structure are implemented.
Selected sub-circuits, as the PLL, a fine grained delay unit and the SRAM IP integration were already successfully verified with a test chip manufactured via an Europractice miniasic run in the same technology.
The DMC is fully controllable via a standard JTAG interface, where all configuration registers are implemented as JTAG chain extensions and well described in a standard conform extended Boundary Scan Description Language (BDSL) file. The python based test-bench preparation includes serial vector file (SVF) format generation based on this BSDL file and a small sequencer compiler. With these a digital full system verification of the all silicon module was performed to check the system behavior before the final submission.

Minioral:

Yes

Description:

chip, image collection

Speaker:

Andreas Wassatsch

Institute:

MPI

Country:

Germany

481

Upgrade of data acquisition and control system for microwave reflectometry on Experimental Advanced Superconducting Tokamak

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Upgrade of reflectometry is ongoing on Experimental Advanced Superconducting Tokamak (EAST) for more comprehensive measurement of plasma density profile and fluctuation. To satisfy requirements of upgraded reflectometry, a new Data Acquisition and Control System(DACS) has been developed.
The profile reflectometry works in 30-110GHz (X-mode) and 40-90GHz(O-mode) with 5 receivers. Each receiver outputs in-phase and quadrature signals simultaneously, so 10 signals need be acquired. Considering beat frequency of 4-10MHz, sampling rate is set as 60 MSPS, and total data rate is 1.2 GB/S. The PXIe-based DACS includes two 8-channel 14-bit 250MSPS digitizers. Data from digitizers is stored in a disk array (RAID 0) with data throughput capacity of 3.6 GB/S. Meanwhile, selected data is transported to a FPGA based real-time computing module, which utilize a pre-trained neural network to invert raw data to plasma density profile. A dedicated 5-channel 250MSPS arbiter waveform generator (AWG) is developed to control voltage control oscillators for frequency sweep. A timing module receive the trigger and clock signal from central controller and synchronize all the digitizers and AWG.
The fluctuation reflectometry operates on 16 fixed frequency points in 50-110GHz (X-mode) and 20-60GHz (O-mode). Receiving antennas are placed on two different poloidal positions to do corelation measurement. Totally, there are 64 signals to be acquired. 8 8-channel 14-bit 60MSPS digitizers are added. The sample rate is 4 MSPS and total data rate is 512 MB/S.
Now the new reflectometry is being installed on EAST, and Its performance will be tested in experimental campaign of 2018.

Minioral:

Yes

Description:

reflectrometry

Speaker:

Fei Wen

Institute:

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Country:

China

536

A Time Stretch Supply Method to Reduce the Power Line Loss

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For a cable based sensor network, power line loss restricts the cable length and cable copper diameter. In this paper, we propose a time stretch method to reduce the power line loss for a sensor network. A sensor network usually works in burst mode, when it works a high current consumption is required, while in idle state it need little power energy. This method uses a super capacitor to collect and store the energy in idle time for each Sensor Unit (SU), so when it changes to active state the SU can use the local power to work, and would not absorb high current from the cable. Since the power line loss is proportional to the square of the current, the lower current can reduce the line loss significantly.

The results shows that this method can reduce the line loss to less than 10%. This method can be used to extend the length of the sensor network cable, or make it is possible to use much finer cable copper core.

Minioral:

Yes

Description:

method for line power loss

Speaker:

Jie Wu

Institute:

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Country:

China

653

536 A Time Stretch Supply Method to Reduce the Power Line Loss

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459

Register-Like Block RAM with Boundary Coverage and Its Applications for High Energy Physics Trigger Systems

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In high energy physics experiment trigger systems, block memories are utilized for various purposes, especially in binned searching algorithms. In these algorithms, the storages are demanded to perform like a large set of registers. The writing and reading operation must be performed in single clock cycle and once an event is processed, the memory must be globally reset. These demands can be fulfilled with registers but the cost of using registers for large memory is unaffordable. Another common requirement is the boundary coverage feature during reading process. When a memory bin is addressed, the stored contents in the addressed bin and its neighboring bin must be output simultaneously. In this paper, a register-like block memory design scheme is described, which allows updating memory locations in single clock cycle, reading two adjacent bins and effectively refreshing entire memory within a single clock. The implementation and test results are presented.

Minioral:

Yes

Description:

Algo RAM access, address

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Jinyuan Wu

Institute:

FNAL

Country:

USA

710

583 An FPGA-Driven Signal Generator for the Barrier Bucket System at COSY

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583

An FPGA-Driven Signal Generator for the Barrier Bucket System at COSY

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At the Cooler Synchrotron (COSY) in Juelich a barrier bucket RF system is used to manipulate the proton beam. Such a system can compensate the energy loss in the target and allows for a mostly constant intensity most of the time. The barrier bucket signal is a short pulse like a single sine period. To provide this signal we developed a signal generator based on a XILINX ZC706 evaluation board.

The internal ARM processor is used for the communication over ethernet. Four wave forms are stored in memory tables with a width of twelve bit and a size of 256 words each. The selected table is read out synchronously with the revolution of the COSY beam. A 16 bit parallel input provides an additional amplitude information. The memory words and this amplitude are multiplied and then fed to an attached DAC to generate the analog signal.

The challenge was the variable frequency. The revolution frequency of COSY changes from about 0.4 MHz to about 1.6 MHz. With 256 data points per resolution the DAC is fed with a frequency in the range of 115 to 404 MHz.
Our understanding was always that the core frequency of an FPGA has to be constant and that PLLs follow frequency changes only slowly.
But we showed that we can increase the frequency from 128 MHz to 400 MHz within 200 ms without the internal PLL of the FPGA losing its lock.

Minioral:

Yes

Description:

FPGA

Speaker:

Peter Wüstner

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FZ Juelich

Country:

Germany

572

EAST Real-Time VOD System Based on MDSplus

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As with EAST（Experimental Advanced Superconducting Tokamak）experimental data analyzed by more and more collaborator, the video from 2D camera which directly reflecting the spatially distributed phenomena in high-temperature plasma, attracts more and more researchers'attention. EAST now have four high-speed cameras and the image capture rate is very from 120 to 1000 frames per second. Archiving and retrieving the video is a challenge for repositories and network. The real-time VOD（Video On Demand）system based on MDSplus [1] allows users viewing the plasma discharge video through Web browser and analyzing the video frames by jScope in real time as same as the other signal data which is also stored in the MDSplus database. The system mainly includes the frames storage and video synthesis. The storage strategies of the camera data into MDSplus will be described to realize instantaneity. The video synthesis technology will be presented to retrieve frames from MDSplus and synthetic video to be displayed on demand. The system offers a uniform way to access the signal data and video during the EAST experiment, which is more convenient and faster than the formal VOD system [2] based on the traditional SQLServer database.

Minioral:

Yes

Description:

Video DAQ

Speaker:

Jinyao Xia

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IPP Hefei

Country:

China

548

Multi-Code-Rate Correction Technique with IR-QC-LDPC: An application to QKD

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Information Reconciliation is a mechanism that allows to purge the discrepancies between two correlated variables. It is a necessary component in each key agreement protocol where the key has to be transmitted through a noisy channel. Note that it is very important to reveal unnecessary information in order to maximize the shared key length in a Quantum Key Distribution(QKD) protocols.

In this paper, we propose a simple encoding and decoding method for irregular-quasic-cyclic low-density parity-check (IR-QC-LDPC) codes. which have an efficient encoding/decoding algorithm due to the cyclic structure of their parity-check matrices. The code can be multi-rate. The proposed encoding/decoding method is applicable to parity-check matrices having dual-diagonal parity structure with different column weight. The proposed scheme first generates message bits, then giving the message bits, the parity bits for the first sub-block will be generated, after exploiting the dual-diagonal structure all parity bits are found through correction. The decoding adopts normalized min-sum algorithm. The whole verification of encoding and decoding algorithm are simulated with MATLAB, the maximum bit error rate is 6% when the frame error rate is less than 1% after error correction. We designed and implemented the whole verification algorithm in the same Field Program Gate Array(FPGA). Based on FPGA the throughput for encoding is 183.36Mbps while the average decoding throughput is 27.85Mbps with random bit error rate between $1\% - 6\%$.

Minioral:

No

Description:

Code correction

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China

411

A 3.8ps RMS time synchronization implemented in a 20 nm FPGA

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A 3.8ps RMS time synchronization implemented in a 20nm fabrication process ultrascale kintex Field Programmable Gate Array (FPGA) is presented. The multi-channel high-speed serial transceivers (e.g., GTH) play a key role in a wide range of applications, such as the quantum key distribution systems. However, owing to the independent clock divider between the serial data clock and the parallel data clock in each GTH channel, the random skew would appear among the multi channels every time the system powers up or resets. Although the FPGA provides a phase alignment method itself, the observed jitter of ˜100ps is far from meeting the demands of extreme precision in many areas. To compensate this skew, a protocol combined of a high-precision time-to-digital converter (TDC) and a tunable phase interpolator (PI) is presented. The TDC based on the carry8 primitive is applied to measure the phase difference of each parallel clock with a bin size of ˜11ps. The embedded tunable PI in each GTH channel has a step precision of ˜3.5ps bin size and ˜0.7ps root mean square (RMS). The final time synchronization of multi channels features a RMS of ˜3.8ps, much better than the prior FPGA phase alignment method. Besides, a desirable time offset of every channel can be implemented with a closed-loop control.

Minioral:

Yes

Description:

time synch

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620

407 The Electronics Design of Error Field Feedback Control System in KTX

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468 Technique of active phase stabilization for the interferometer with 128 actively selectable paths

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468

Technique of active phase stabilization for the interferometer with 128 actively selectable paths

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A variable-delay optical interferometer with 128 actively selectable delays and a technique of active phase stabilization were innovatively designed and applied for the first time in the experiment of round-robin differential phase shift quantum key distribution (RRDPS-QKD). According to the RRDPS protocol, larger number of delay channels in interferometer can ensure higher tolerance of bit errors, eliminating the fundamental threshold of bit error rate of 11% in traditional BB84 protocol. Therefore, an interferometer with 128 selectable delay paths is constructed and demands the ability of fast switching at the rate of 10 kHz, which requires dynamic stability of multiple paths. Thus, a specific designed phase stabilization technique with closed real time feedback loop is introduced to guarantee the high visibility of interferometer selections dynamically. The active phase stabilization technique employs a phase modulator (PM) driven by a DAC to adjust the relative phase between the two arms of the interferometer. By monitoring photon counting rates of two Up-Conversion Detectors (UCD) at two output ports of the interferometer, a Field Programmable Gate Array (FPGA) calculates and finds the optimal code value for the DAC, maintaining a high visibility of the interferometer every time a new light path is selected. The visibility of most of the 128 interferometer selections can simultaneously be maintained over 96% during the QKD, which strongly supports the experiment.

Minioral:

Yes

Description:

interferometer

Speaker:

Yu Xu

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China

713

597 Data Acquisition in Phase II Run of the Belle II Experiment

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597

Data Acquisition in Phase II Run of the Belle II Experiment

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The Belle II experiment, a next generation experiment in the field of flavor physics, is scheduled to start in 2018. The main purpose of the experiment is to search for physics beyond the standard model with high-precision measurement of B meson decays. The luminosity of SuperKEKB accelerator, an asymmetric electron/positron collider, will be 40 times as much as that of the previous KEKB accelerator and the Level-1 trigger rate is estimated to reach as much as 30 kHz. The readout system of the Belle II experiment receives a large amount of data from different front-end electronics of several sub detectors, process and send data to the back-end system where the online event-rate reduction is performed by a high-level trigger system. After the phase I run for accelerator commissioning without the Belle II detector in 2016, the phase II run is scheduled to start in Feb. 2018, where data from the first beam collision will be taken. In the phase II run, all Belle II sub-detectors are used, while the innermost vertex sub-detectors are partially installed. In this contribution, performance of the Belle II readout system in the first beam run as well as the results of a large-scale performance measurement with dummy data will be reported.

Minioral:

Yes

Description:

DAQ

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Satoru Yamada

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Japan

472

High-speed RF Switch Electronics for picking up of Electron-Positron Beam Bunches

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In modern electron positron colliders, both the electron and the positron runs in the tunnel, such as Circular Electron Positron Collider (CEPC) to be built and Beijing Electron Positron Collider (BEPCII). To guarantee good quality of the beam, beam diagnostics is indispensable. To achieve beam measurement of the electron and positron beams, picking up of these two different bunches

in real time is an important task. Since the time interval between the adjacent electron and positron bunch is quite small, for example 6 ns in CEPC, high speed switch electronics is required. The paper presents the prototype design of a high-speed Radio Frequency (RF) electronics which is able to pick up nanosecond positron-electron beam bunches, with a switching time less than 6 ns. We also conducted initial tests in the laboratory to evaluate the performance of the electronics, and the results indicate that this module can successfully achieve bunch signal pick up within 6 ns time interval. The electronics makes it possible to measure electron and position beams respectively, thus improving the beam quality.

Minioral:

Yes

Description:

RF, beam

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Liujiang Yan

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Country:

China

404

High Resolution X-ray Imaging Using Monolithic Silicon Pixel Sensor

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A high resolution X-ray imaging system based on ALPIDE, a CMOS monolithic active pixel sensor (MAPS), is presented. ALPIDE is a 15 mm × 30 mm large MAPS with 512 × 1024 27 μm × 29 μm pixels that are read out in a binary hit/no-hit fashion, and with the control and readout system, it can detect the max particle rate of 100 MHz / cm^2, and achieve the spatial resolution of around 5 μm. The imaging system counts the incident X-ray photon hits on every ALPIDE pixel per exposure to produce a gray scale image. Imaging results of grating patterns and insect specimens are presented.

Minioral:

Yes

Description:

X-ray imaging

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Country:

China

705

558 Final design of the readout system for Triple-GEM detectors for the CMS forward muon upgrade

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704

557 Design of a common verification board for different back-end electronics options of the JUNO experiment

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557

Design of a common verification board for different back-end electronics options of the JUNO experiment

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The Jiangmen Underground Neutrino observatory (JUNO) is a neutrino medium baseline experiment in construction in China, with the goals to determine the neutrino mass hierarchy and to perform precise measurements of several neutrino mass and mixing parameters. A large liquid scintillator (LS) volume will detect the antineutrinos issued from nuclear reactors. The LS detector is instrumented by 17000 large photomultiplier tubes. One of the innovative aspects of JUNO is its electronics and readout concept. The JUNO electronics readout system consists of two parts: the front-end electronics system performing analog signal processing (the underwater electronics) and after about 100 m cables, the back-end electronics system, outside water, consisting of the DAQ and trigger. One of the main challenges of the whole electronics system is the fast data link (250 Mb/s) combined with power delivery over 100 m Ethernet cables.
Three different options have been considered to connect the front-end and the back-end systems, depending on the DAQ data volume and the way to deliver the power to the underwater system.

In order to test the three options in an efficient and fast way, a common baseboard with interfaces to different mezzanine boards has been designed. We will present the 3 options and report on the details of the baseboard design as well as on its performance.

Minioral:

Yes

Description:

Hardware test?

Speaker:

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558

Final design of the readout system for Triple-GEM detectors for the CMS forward muon upgrade

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In this contribution we will present the readout system being designed for triple-GEM detectors that should be installed in 2019-2020 in the CMS muon endcap system for the LHC high luminosity phase. Beginning of 2017, 10 triple-GEM detectors equipped with VFAT2 front-end chips and readout system version 2 have been for the first time installed in CMS. Lessons learnt from this so-called "slice test"has led to a more robust version, V3, the final version.

The readout system being designed takes full advantage of current generic developments introduced for the LHC upgrades: CTP7 AMC boards host in micro-TCA crates for the off-detector electronics, the Versatile Link with the GBT chipset to link the front-end electronics to the micro-TCA boards. In addition, the CMS AMC13 micro-TCA board will be used to interface the back-end electronics to the central CMS DAQ system. Finally, the FEAST DC-DC converters are used to power the on-detector electronics.

The triple-GEM detectors are read-out by a new front-end chip, the VFAT3 running at 320MHz, compatible with the GBT chipset. In addition, a few hardware components have been developed specifically for this project: the GEM Electronic Board (GEB) and the Opto-Hybrid board. The Opto-Hybrid is a small (typically 10 x 20 cm2) mezzanine equipped with a Xilinx Virtex6 FPGA and the GBT chipsets.

We will report on the latest status of the whole readout system with special focus on the changes compared to the version 2, on slice test results and first tests of the final version.

Minioral:

Yes

Description:

VFAT2 chip

Speaker:

Yifan Yang

Institute:

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Country:

Belgium

631

458 The Design and Testing of the Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS New Small Wheel Upgrade

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The Design and Testing of the Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS New Small Wheel Upgrade

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The Address in Real Time (ART) Data Driver Card (ADDC) is designed to transmit the trigger data in the Micromegas detector of the ATLAS New Small Wheel (NSW) upgrade. The ART signals are generated by the front end ASIC, named VMM chip, to indicate the address of the first above-threshold event. A custom ASIC (ART ASIC) is designed to receive the ART signals from the VMM chip and do the hit-selection processing. Processed data from ART ASIC will be transmitted out of the NSW detector by GBTx serializer and VTTx optical transmitter module through fiber optical links.
The ART signal is critical for the trigger selection in ATLAS experiment thus the functionality and stability of the ADDC is very important. To ensure extensive test of the ADDC, a test platform based on FMC card and special firmware/software are developed. This test platform works with the commercial Xilinx VC707 FPGA development kit, it can test all the functionalities and long term stability of the ADDC even without other NSW electronics boards. This paper will introduce the design, test procedure and preliminary test results of the ADDC and the FMC based test platform.

Minioral:

Yes

Description:

trigger alog and address

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BNL

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USA

499

The Framework Design of the Detector Control System of JUNO

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The Jiangmen Underground Neutrino Observatory (JUNO) is the second phase of the reactor neutrino experiment. The detector of the experiment was designed as a 20k ton LS with a Inner diameter of 34.5 meters casting material acrylic ball shape. Due to the gigantic shape of the detector there are approximate 10k monitoring point of temperature and humidity. There are about 20k channels of high voltage of array PMT, electric crates as well as the power monitoring points. Since most of the first phase software of the DCS was developed on the framework based on windows, which is limited by operation system upgrade and commercial software, the framework is necessary for DCS of JUNO. The paper will introduce the Design of the framework of the DCS based on EPICS (Experimental Physics and Industrial Control System) running Linux OS. The implementation of the IOCs of the high-voltage crate and modules, stream device drivers, and the embedded temperature firmware will be presented. The software realization and the remote control method will be presented as well as the development of the GUIs by CSS (Control System Studio). The framework can be widely used in the project with the similar hardware and software interfaces.

Minioral:

Yes

Description:

EPICS

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692

500 Design of TDC ASIC based on Temperature Compensation

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500

Design of TDC ASIC based on Temperature Compensation

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On the basis of requirement of CSNS, we designed a TDC chip with temperature compensation function in this paper, which employed TSMC 180nm process. Using delay unit bufx8 as the major method, delay lines in each level delayed input signal line through the bufx8 unit to realize fundamental measurement function. The time intervals of two fixed delay standard pulses did not change with temperature variation via intra-chip phase-locked loop. After that, the two standard pulses were sent to TDC internal delay line and measured their values. Then the measured values and standard values were compared. According to the result of comparing and decision switch, the structure of delay lines was reconstructed and their levels were recorded at the same time. We could ensure that the total length of the effective delay line were close to clock cycle as much as possible under the current temperature. The chip was tested after the completion of design. It was found that the time resolution of TDC ASIC was 73ps under 1.8V power supply at room temperature while the time resolutions were 103ps and 62ps at 85° and 0°, respectively.

Minioral:

Yes

Description:

Temp compensation

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433

An Ultra-high Speed Waveform Digitizer for the Applications of ICF Experiment

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In the inertial confinement fusion (ICF) experiment, there is a growing demand for ultra-high speed waveform digitizer, so as to realize the accurate measurement of various physical quantities for plasma diagnosis. However, the commercial oscilloscopes are of low precision and large volume for some physical experiments. Especially in the ICF experiment with strong radiation, whether using long cables to keep the oscilloscopes away from the radiation or shielding the oscilloscopes in the experimental field is not convenient for accurate measurement.
Aimed at this demand, we design an ultra-high speed waveform digitizer which can meet the requirements of a variety of measurements such as time, energy and pulse waveform discernment and so on in ICF experiment. The digitizer consists of three parts: analog-to-digital conversion, cache, and data up-link. The detector signal is digitized through fast ADC. Then, the digital data is cached in an external DDR3 memory stick through FPGA. The data can be uploaded to PC via Ethernet.
The waveform digitizer has 10 bits with a sampling rate of 5G/s and bandwidth of 1G, the ENOB reaches 8.2bit@120M. The capacity of the DDR3 memory stick is 4GB so that it can record signals longer than 600ms. In the strong radiation environment of "Sheng Guang II" ICF experiment with the laser power of 0.3 PW, the digitizer works well. Contrast tests with a commercial oscilloscope (Tektronix DPO4104B 5G/s BW1G) show that it performances much better.

Minioral:

Yes

Description:

acq board

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694

513 A multi-channel DAQ system based on FPGA for long-distance transmission in nuclear physical experiments

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513

A multi-channel DAQ system based on FPGA for long-distance transmission in nuclear physical experiments

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As the development of electronic science and technology, electronic data acquisition(DAQ) system is more and more widely applied to nuclear physics experiments. Workstations are often utilized for data storage, data display, data processing and data analysis by researchers. Nevertheless, the workstations are ordinarily separated from detectors in nuclear physics experiments by several kilometers or even tens of kilometers. Thus a DAQ system that can transmit data for long distance is in demand. In this paper, we designed a DAQ system suitable for high-speed and high-precision sampling for remote data transfer. An 8-channel, 24-bit simultaneous sampling analog-to-digital converter (ADC) named AD7779 was utilized for high-speed and high-precision sampling, the maximum operating speed of which runs up to 16 kilo samples per second(KSPS). ADC is responsible for collecting signals from detectors, which is sent to Field Programmable Gate Array(FPGA) for processing and long-distance transmission to the workstation through optical fiber. As the central processing unit of DAQ system, FPGA provides powerful computing capability and has enough flexibility. The most prominent feature of the system is real-time mass data transfer based on streaming transmission mode, highly reliable data transmission based on error detection and correction and high-speed high-precision data acquisition. The results of our tests show that the system is able to transmit data stably at the bandwidth of 1Gbps.

Minioral:

Yes

Description:

std daq

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Country:

China

690

483 Time of flight Measurement Electronics for Back-n at CSNS

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483

Time of flight Measurement Electronics for Back-n at CSNS

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Back-n is a white neutron beam line at China Spallation Neutron Source (CSNS). The time structure of the primary proton beam make it fully applicable to use TOF (time-of-flight) method for neutron energy measuring. We implement the TOF measurement on the general -purpose readout electronics system which is designed to adapt all of the seven detectors in Back-n. The general-purpose readout electronics system is based on PXIe (Peripheral Component Interconnect Express eXtensions for Instrumentation) platform, which is composed of FDM (Field Digitizer Modules), TCM (Trigger and Clock Module), and SCM (Signal Conditioning Module). T0 signal synchronous to the CSNS accelerator represents the neutron emission from the target. It can be considered as the start time of TOF. The trigger and clock module (TCM) receives, synchronizes and distributes the T0 signal to each FDM based on the PXIe backplane bus. Meantime, detector signals after being conditioned are fed into FDMs for waveform digitizing, which can be considered as the time of capturing neutrons, i.e. the stop time of TOF. FPGA-based TDC is implemented on FDM to accurately acquire the interval between the time of T0 arriving at FDM and the time of neutrons being captured. There is also a FPGA-based TDC on TCM to accurately acquire the interval between asynchronous T0 signal and the measurement electronics. These results are used for TOF measurement. This method for TOF measurement is efficient and not needed for additional modules. Test result shows the accuracy of TOF is sub-nanosecond and applicable for Back-n.

Minioral:

Yes

Description:

TOF

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619

403 Application of FPGA Acceleration in ADC Performance Calibration

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403

Application of FPGA Acceleration in ADC Performance Calibration

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In recent years, high speed and high resolution analog-to-digital converter (ADC) is widely employed in many physical experiments, especially in high precision time and charge measurement. The rapid increasing amount of digitized data demands faster computing. FPGA acceleration has an attracting prospect in data process for its stream process and parallel process feature. In this paper, an ADC performance calibration application based on FPGA acceleration is described. FPGA reads the ADC digitized data stream from PC memory, process and then write processed data back to the PC memory. PCIE bus is applied to increase the data transfer speed, and floating point algorithm is applied to improve the accuracy. The test result shows that FPGA acceleration can reduce the processing time of the ADC performance calibration compared with traditional method of C-based CPU processing. This frame of PCIE-based FPGA acceleration method can be applied in analysis and simulation in the future physical experiment for large ADC array, such as CCD camera and waveform digitization readout electronics calibration.

Minioral:

Yes

Description:

ADC calibration Algo

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428

Readout method based on PCIe over optical fiber for CBM-TOF super module quality evaluation

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The Compressed Baryonic Matter (CBM) experiment will investigate the QCD phase diagram at high net baryon densities and moderate temperatures. CBM Time of Flight (TOF) system is composed of super modules containing high performance Multi-gap Resistive Plate Chambers (MRPCs). During

the mass production, each super module assembled with MRPCs needs quality evaluation, which includes time measurement and data readout. Read out electronics encounter the challenge of reading data from a super module at a speed of about 6 Gbps. In this paper, a read out method based on PCIe over optical fiber is proposed for CBM-TOF super module quality evaluation. The digitized data from super module will be concentrated at the front-end electronics, and then be transmitted to a PCIe switch module (PSM) over optical fiber using PCIe protocol. The PSM is directly plugged into the motherboard via gold fingers at the backend data acquisition server. With this readout method, a high-speed transmission rate can be reached. Furthermore, a PSM can receives data from several super modules simultaneously, which is important to improve the evaluation efficiency. This readout method simplifies the architecture of readout electronics and supports long distance transmission between frontend and backend.

Minioral:

No

Description:

readout scheme

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423 JUNO DAQ Readout and Event Building Research

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423

JUNO DAQ Readout and Event Building Research

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Abstract ： The Jiangmen neutrino experiment(JUNO) will design, develop and operate an internationally leading neutrino experimental station to measure the order of neutrino mass, accurately measure neutrino mixing parameters, and carry out many other scientific frontier studies. The entire experimental system includes a detector system, an electronics system, and a data acquisition (DAQ) system. Data flow is the core of JUNO DAQ system. Readout and Event Building (EB) are two key aspects of data flow. Based on the requirement analysis of JUNO DAQ, this thesis proposes a data flow schema of distributed network readout and second-level event building. Focusing on the design performance index of JUNO DAQ, the performance of the readout module and event building module, the number of readout processes and event building processes deployed on each node, the ratio of readout nodes and event building nodes and scalability of the two modules are discussed in detail. The results of the research provide a reference for further optimization of the JUNO DAQ

data flow framework.
Keywords：JUNO DAQ; readout；event building；data flow；performance；deployment

Minioral:

Yes

Description:

system

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402

Study of Full Parallel RS(31,27) Encoder for a 3.2 Gbps Serial Transmitter in 0.18 um CMOS Technology

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A full parallel Reed Solomon encoder is developed for a 3.2 Gbps serial transmitter. The code structure is two interleaved RS(31,27) codes. One RS(31,27) code has 135 information bits and 20 redundancy bits. A frame has the information rate of 0.844 and provides the capability of correcting 20 bits consecutive errors. Two encoder modules work in parallel and send the encoded data to an interleave module. We tried the regular serial structure and a novel parallel structure to develop the RS encoder. The regular serial structure has a data output width of 5 bits, so it needs a 320 MHz clock to achieve the 3.2 Gbps speed requirement. The parallel structure requires acceptable more area, but only a 10 MHz clock is needed. The 3.2 Gbps serial transmitter is used for a CMOS monolithic active sensor application. This transmitter has been verified in 0.18 um CMOS Technology. A matched RS decoder is implemented on a Xilinx Kintex-7 FPGA board.

Minioral:

No

Description:

Data encoding

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393

Design of a general scientific CCD simulation and test system based on FPGA

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With the rapid development of electronicsal technology, the scientific CCD detector has been widely used in many fields such as astronomy, medicine and industry due to its ultra-high quantum efficiency and ultra-low readout noise. In order to verifyfacilitate rapid the functions and performances test of the of the scientific CCD controller rapidly, a general simulation and test system based on FPGA is designed to test the overall function and performance of the CCD controller. The simulation and test system meets the test requirements of different types of CCD, such as detecting different signals of the CCD controller including power supply, fan, temperature control module, crystal oscillator, shutter and clock-bias generator. Furthermore, the video signal of the CCD detector can be simulated and superimposed with random noise to verify the performance of the video sampling circuit of the CCD controller. For generating a simulated video waveform of CCD detector, digital DDS waveform generation method was used and a high-speed TRNG generator based on oscillation ring in FPGA was designed and used as random noise data. The simulation and test system was successful used for the CCD controller which was designed for E2V CCD47-20 detector.

Minioral:

Yes

Description:

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463

The uTCA Fast Control board for generic control and data acquisition applications for HEP experiments

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The uTCA Fast Control board (uFC) is an FPGA-based μTCA compatible Advanced Mezzanine Card (AMC) for generic control and data acquisition applications in high energy physics (HEP) experiments. Built around the Xilinx Kintex-7 FPGA, the uFC provides users with a platform which has access to on-board FPGA Mezzanine Card (FMC) sockets with a large array of configurable I/O and high-speed links up to 10 Gbps. This paper presents test results from the first set of pre-production prototypes and reports on applications in High Energy Photon Source in China.

Minioral:

Yes

Description:

uTCA control

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475

APA integration test for the ProtoDUNE-SP LAr TPC at CERN

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As an important prototype of Deep Underground Neutrino Experiment (DUNE) far detector, ProtoDUNE single phase (ProtoDUNE-SP) with a total liquid argon (LAr) mass of 770 ton, represents the largest monolithic single-phase LAr TPC detector to be built to date. The detector elements, consisting of 6 Anode Plane Assemblies (APAs), 3 Cathode Plane Assemblies (CPAs), are housed in a cryostat that will contain the LAr target material. The development of readout electronics has been following an integral concept, which includes the APA, cold electronics (CE), signal feed-through assembly and warm interface electronics.
Since August 2017, the APAs have started to be instrumented with readout electronics for integration test and moved into the cryostat one by one at CERN. With the benefits of the well-designed CE

developed for extremely low temperatures (77K-89K), the equivalent noise charge (ENC) measured on an induction wire (U or V) of APA is less than 500 e- at 159K with peaking time of 2us, for a collection wire (X) the ENC is less than 400 e-. The projected ENC of the single-phase DUNE far detector will meet the requirement which is to be less than 1000 e- for induction wires under the situation of expected worse case instantaneous charge arriving at the APA from a minimum-ionizing particle (MIP). According to the current schedule, ProtoDUNE-SP will complete APA integration test by May 2018.

Minioral:

Yes

Description:

Detector?

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617

396 Design of Voltage Pulse Control Module for Free Space Measurement-Device-Independent Quantum Key Distribution

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396

Design of Voltage Pulse Control Module for Free Space Measurement-Device-Independent Quantum Key Distribution

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Measurement-device-independent quantum-key-distribution protocol (MDIQKD), which is immune to all hacking attacks on detection, guarantees the security of information theoretically even with single-photon detectors, whose performance is not perfect. Fiber channel is used by the previous MDIQKD experimental device. However, the signal attenuation increases exponentially along with the transmission distance increases. But using free space as the channel for signal transmission, with the signal attenuation increases squarely (without considering the scattering of the atmosphere), the signal attenuation trend can be effectively reduced. In order to implement free space MDIQKD experiments, a modulation module is needed to modulate the wide pulse chopping, decoy-state, normalization, phase encoding and time encoding. In this paper, we present a design of Voltage Pulse Control Module (VPCM) for free space MDIQKD. The main function of voltage pulse control is as a modulation circuit, with a total of 5 Digital to Analog Converter (DAC) outputs. The output

voltage of 5 DACs can be adjusted from 0V to 6V in 0.05V steps. And all 5 DACs have adjustable delay times of ± 15ns in 100ps steps. The rising edge of the DAC outputs is about 1ns, and the maximum amplitude can reach 7V with a 50Ω impedance. And with the increase of power, we can get a flatter pulse, which can better serve the subsequent optical modulator. After that, we are going to implement a system with clock frequency up to GHz. By increasing the clock frequency, we expect that the security key rate can be further increased.

Minioral:

Yes

Description:

Key

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702

541 A low power DAQ system with high-speed storage for submersible buoy

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541

A low power DAQ system with high-speed storage for submersible buoy

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Submersible Buoy (SB) is an important apparatus capable of long-term, fixed-point, continuous and multi-directional measurement of acoustic signals and hydrological environment monitoring in the harsh marine environment, providing important information for hydrological environment research, marine organism research and protection.
The SB has long runtimes and recovery cycles, and the entire system is powered by batteries. So, the DAQ system should be as low-power as possible due to the requirement of long-term, stable underwater operation. Meanwhile, the DAQ system also demands large capacity storage because of long runtime and relatively high sampling rate. Owing to the wide distribution of the SB, the DAQ system must ensure high-speed data storage as well as high-speed upload path to the host when

retrieving data in order to reduce data collection time and improve the extraction efficiency. Given all above, this paper proposes a DAQ system, which consists of multi-channel ADCs for hydrophones signal digitization; one Spartan-6 FPGA for data package, capture and compression; SD card for short-term data storage; SSD for long-term data storage along with dual Gigabit Ethernet for data upload. Preliminary test shows that the DAQ system can achieve high-speed data conversion, storage and readout at comparatively low-power.

Minioral:

Yes

Description:

hardware

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Zhilei Zhang

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Country:

China

539

The application of precision time protocol on EAST timing system

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The timing system focuses on synchronizing and coordinating each subsystem according to the trigger signals. The former timing system was based on commercial off-the-shelf devices and a set of synchronized optical network which was made up of several pairs of multi-mode fibers. The expensive PXI devices and inconvenient extension methods compel maintainers to upgrade the timing system to meet the ever increasing demands of the experiments. A new prototype timing slave node based on precision time protocol has been developed using ARM STM32 platform. The proposed slave timing module is tested and experimental results show that the synchronization accuracy between slave nodes is in sub-microsecond range. This paper will introduce the features of the precision time protocol and the details about the system architecture, slave timing module platform and test results will be described in this manuscript.

Keywords: trigger; precision time protocol; STM32

Minioral:

Yes

Description:

Time protocol

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591

New version of High Performance Compute Node for PANDA TDAQ system

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PANDA is a general purpose hadron spectrum to be installed in the high energy storage ring of the Future Anti-proton and Ion Research facility-FAIR, in Germany. Physics simulation shows that the event rate for PANDA experiment is about 20MHz, and event size from 1.5KByte to 4.5KByte per event. Considering background, the relative data rate to the TDAQ system will be as high as 200 GByte per second. xTCA frame will be appropriate scheme for PANDA TDAQ system.
New version of High Performance Compute Node is the key module for PANDA TDAQ system. Xilinx Ultrascale FPGA is used for data parallel processing. RocketIO hard core in FPGA used for high speed data transmission. DDR4 is used for mass data buffering. 10 Gigabit Ethernet is designed for data output. Gigabit Ethernet Switch is designed for AMC cards Ethernet port, ATCA Ethernet Switch, RTM Ethernet port switching, which can be used as slow control channel. Backplane of ATCA board is designed as full mesh topology for data sharing between every compute node. IPMC/MMC platform is designed following xTCA specification. New version Compute Node is finished. Latest testing result will be shown in the meeting.

Minioral:

Yes

Description:

HP DAQ

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679

430 Design of readout electronics of scintillators and SiPMs for CEPC ECAL preresearch

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430

Design of readout electronics of scintillators and SiPMs for CEPC ECAL preresearch

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The Circular Electron Positron Collider (CEPC) is a proposing electron positron collider in China which aims for generating a very high center-of-mass energy colliding above 250GeV in where Higgs events are produced with considerable luminosity. The high granularity Electromagnetic Calorimeter (ECAL) is included in calorimeter system which is mainly responsible for the measurement of photon. A Particle Flow Algorithm (PFA) based ECAL solution will utilize about 400k channels /mˆ3. Here we will present a design of readout electronics based on SPIROC2b for the CEPC ECAL with high granularity scintillants and SiPMs. The readout electronics consists of Front-End-Board (FEB), Data InterFace Board (DIF) and Data Acquisition Board (DAQ). The FEB carries SiPMs (S12571-010P), scintillants (PSD) and front-end ASIC (SPIROC2b). Here we present a simplified version which only include FEB and DIF and tests are based on this simplified version.
Electronic tests, radioactive source X-ray tests and cosmic ray tests were conducted to this system. The results indicate that a charge dynamic from 80fC –300pC @ S/N=4 is successfully achieved and MIPs is separated from pedestal. A 90Sr 2.28MeV electron deposited energy spectrum is also measured by this system. We will also present an electronic calibration method in this design which could automatically calibrate each channels when SPIROC2b do not provide a calibration pin.

Minioral:

Yes

Description:

SiPM

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678

429 A Front-end Signal Digital Acquisition System In Intensive Electromagnetic Field Circumstance

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429

A Front-end Signal Digital Acquisition System In Intensive Electromagnetic Field Circumstance

Author: He Zhou[1]

Co-authors: Jin Ge [1]; Lian Chen [1]; Feng Li [1]

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In Inertial Confinement Fusion(ICF), the laser-driven magnetic-flux compression can suppressing the heat losses through electron confinement, thus increasing the ion temperature as well as the neutron yield. The pulse magnetic field is created by discharging a high-voltage capacitor through a small wire-wound coil, and the Rogowski coil is used to measure the discharge current which can describe the corresponding magnetic field waveforms. In the ICF experimental, the signal from the Rogowski coil is usually transmitted to the oscilloscope through a long-distance coaxial cable. However, the electromagnetic interference caused by high-power loser will greatly affect the signal transmission.
A front-end signal digital acquisition system prototype is designed. The prototype is installed in an aluminum box and placed as close as possible to the Rogowski coil. The enclosure of the box is well grounded and sealed to shield the electromagnetic interference. The signal generated by the Rogowski coil passes the protection and shaping circuit. Then the signal is digitalized by the analog-to-digital convert(ADC), and the digital signal is recorded in field-programmable gate array(FPGA). The triple modular redundancy(TMR) is used to reduce the impact of signal-event upset(SEU) in the strong radiation environment. After the implosion process, the data is transmitted to the server by the wireless interface.
The outfield test result shows that the prototype can has a comparable performance as the oscilloscope for pulse magnetic field measurement.

Minioral:

Yes

Description:

system

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471

Cascading Sensor Network Clock Synchronization Scheme

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In this paper, we propose a hybrid clock synchronization architecture for a cascaded sensor network based on GPS time service and synchronous frame protocol. The sensor's upper-level unit is called sensor management unit (SMU) which synchronizes the local clock with the GPS and then use the broadcast sync frame to synchronize the clock of the sensor chain. In this paper, we build a link of 20 cascaded sensors to measure the center frequency and clock stability. The results showed that the center frequency deviation was 0.037 Hz and the stability was 0.045 ppm to 0.066 ppm .The stability of GPS is 0.06ppm, the scheme has achieved the effect similar to installing GPS chip on every sensor.

Minioral:

No

Description:

clock Synch

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517

Testing of Front-End Readout Prototype ASICs Designed for WCDA in LHAASO

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The Large High Altitude Air Shower Observatory (LHAASO) is a multipurpose complex which aims at discovery of cosmic ray origin. In LHAASO, the Water Cherenkov Detector Array (WCDA) is one of the key detectors, which consists of more than 3000 Photomultiplier Tubes (PMTs). Both high precision time and charge measurement are required over a large dynamic range from 1 Photon Electron (P.E.) to 4000 P.E. To simplify the circuits and improve the system reliability, front-end ASICs (Application Specific Integrated Circuits) are specially designed and tested. As for time measurement, the signal is fed to the discrimination circuits inside the ASIC and then digitized by the following FPGA-based Time-to-Digital Converter (TDC). As for charge measurement, we designed the amplification & shaping circuits integrated within one ASIC and an Analog-to-Digital Converter (ADC) integrated in another ASIC. Tests were conducted to evaluate the performance of these prototype ASICs, and the results indicate that the time resolution is better than 250 ps RMS and the charge resolution is better than 10%@1 P.E. and 1% @ 4000 P.E.

Minioral:

Yes

Description:

ASIC

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China

502

A High Precision Signals Readout System for Micromegas Detector Based on the VMM

Author: Shuang Zhou[1]

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Micromegas detector is a gas detector with parallel plate structure, and it consists of a conversion gap in which radiations liberate ionization electrons and a thin amplification gap. The signal of the micromegas detector consists of two parts: the electron peak and the ion tail. The electronic signal just keeps few nanoseconds, which is used for precise time measurement. The ion signal carries most of the signal energy, and it is used to reconstruct particle energy. The micromegas detector has the advantages of high counting rate, high gain, good time resolution and position resolution, excellent radiation-hardened performance, large sensitive area and readout convenience. This paper introduces a signals readout electronics system for micromegas detector based on VMM chips. The VMM is the front end ASIC to be used in the front end electronics readout system of both the micromegas and sTGC detectors of the New Small Wheels Upgrade project. The VMM is designed by Brookhaven National Laboratory, and each chip is composed of 64 linear front-end

channels. Each channel integrates a low-noise charge amplifier (CA) with adaptive feedback, test capacitor, and adjustable polarity (to process either positive or negative charge). Based on those characteristics, the VMM is applicable for the signals readout system of multichannel detectors. The readout system consists of three parts: the front-end board, the data acquisition board, and the host computer with the control software.

Minioral:

Yes

Description:

DAQ board

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711

584 A 14 Gbps low power VCSEL driver for high-energy physics experiments

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584

A 14 Gbps low power VCSEL driver for high-energy physics experiments

Author: Wei Zhou[1]

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We present the design and the preliminary test results of a dual-channel VCSEL-driver ASIC, LOCld65 with the aim of introducing it for the upgrade of the front-end readout system of the ATLAS Liquid Argon Calorimeter. LOCld65 is fabricated in a commercial 65-nm CMOS process, and each

channel operates up to 14 Gbps. LOCld65 provides a perfect match to lpGBT, which is a single-channel 10 Gbps serializer-deserializer ASIC developed chiefly for HL-LHC upgrades. Each channel of LOCld65 can be turned off individually thus providing a flexible solution on the front-end module design. LOCld65 can also be used for general optical transmission applications in high-energy physics experiments.

The analog core of LOCld65 consists of a continuous-time equalizer, a four-stage limiting amplifier, and a high-current differential driver. The programmable equalizer can effectively mitigate the high-frequency loss due to the traces on the printed circuit board. A shared inductive-peaking technique is adopted to extend the bandwidth and reduce the chip area. A programmable active feedback circuit is used to optimize the gain and bandwidth in different process corners. The two-channel design is fabricated on a 1 mm x 1 mm die area and packaged in a 24-pin QFN package.

We have preliminary eye mask test results for LOCld65. It passed at 10-Gbps and 14-Gbps with an 850-nm 10-Gpbs VCSEL. The power dissipation of each channel is 58 mW with a 6-mA modulation current and a 2-mA bias current. We plan to test the radiation effects, including SEE and TID in the future.

Minioral:

Yes

Description:

14Gbps ASIC

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China

685

457 Design of Mesh-Signal Readout Electronics for PandaX-III prototype TPC

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414

Development of the Front-End Electronics for PandaX-III Prototype TPC

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The Particle And Astrophysical Xenon Experiment III (PandaX-III) is an experiment to search for the Neutrinoless Double Beta Decay (NLDBD) using 200 kg radio-pure high-pressure gaseous xenon TPC with Micromegas detectors at both ends and cathode in the middle. A small-scale TPC equipped with 7 Microbulk Micromegas detectors is developed as the prototype detector. 128 channels are readout following an X-Y design with strips of 3 mm pitch (64 channels each direction) from one Micromegas module. Highly integrated front-end electronics composed of 4 front-end cards with 1024 readout channels is designed to readout the charge of Micromegas anode signals, digitize the waveform after shaping and send compressed data to back-end electronics. The cornerstone of the front-end electronics is a 64-channel application specific integrated circuit which is based on a switched capacitor array. The integral nonlinearity of the front-end electronics is less than 1% with 1 pC. The noise (RMS) of each readout channel is less than 0.9 fC with 1 μs peaking time and 1 pC range. Using the radioactive source 137Cs, joint-test of front-end electronics with the prototype TPC was carried out and the hit map of 7 Micromegas has been reconstructed.

Minioral:

Yes

Description:

system

Speaker:

Danyang Zhu

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China

457

Design of Mesh-Signal Readout Electronics for PandaX-III prototype TPC

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The Particle And Astrophysical Xenon Experiment III (PandaX-III) is an experiment to search for the Neutrinoless Double Beta Decay (NLDBD) using high-pressure gaseous xenon TPC with Micromegas detectors at both ends and cathode in the middle. At the first phase of the experiment, there are

41 Micromegas detectors at each TPC end-plate. A small-scale TPC equipped with 7 Micromegas detectors is developed as the prototype detector. There are 128 strip signals and one mesh signals from the Micromegas module.
The Mesh Readout Card (MRC) is designed to readout all mesh signals from the end-cap on one side and generate individual 'Mesh-trigger'signals. These trigger signals can combine with the anode strip signals to help the track reconstruction. There are 41 input analog channels on one MRC, and 8 input channels with 2 ADCs has been welded for joint-test with the prototype TPC. Each channel uses discrete components containing a charge sensitive amplifier and a CR-RC2 shaper to readout the charge from mesh. The waveform of each shaper output is sampled by ADC channel, processed by an FPGA chip and sent to back-end electronics via an optical link. The integral nonlinearity of the MRC is less than 3% with 5.5 pC range. The noise (RMS) of each readout channel is less than 1.25 fC with 1 μs peaking time and 5.5 pC range. The performance of the MRC meets the requirements of the PandaX-III prototype TPC.

Minioral:

Yes

Description:

TPC, micromega board

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Country:

China

444

Preliminary Design of Integrated Digitizer Base for Photomultiplier Tube

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The photomultiplier tubes (PMT) are popularly used in high energy physics experiments, nuclear related experiments, medical equipment and other fields. The conventional readout system with PMTs use the discrete or integrated pulse shaping circuits and FADC boards which are based on NIM or VME system to implement the data acquisition function. In many applications, there are only several PMTs used in whole system, or in some distributed applications, long distance analog cable with high voltage power cable are not applicable due to tremendous channels and enormous distributed space. The integrated digitizer base is designed for neutron scintillator detector with two PMTs used to measure the background radiation and neutrino experiments with more than 20000 PMTs aim to geometrical neutrino explorer, they all will be deployed in China Jinping underground Laboratory (CJPL). There is only one Gigabit unscreened twisted-pair cable needed for data, power and synchronized timing. Over 800 Mbps TCP data throughput and more than 10W power can be supplied with 50ns synchronized precision. The pulse shaping analog circuit, Giga-sample per-second analog to digital converter, precision DC offset trimming circuit, real time trigger scheme, data buffering and transmission, tunable high voltage generator and OLED user interface are all integrated in the digitizer base, and it can be plug with PMT directly. This paper will illustrate

the system architecture, hardware design, software development and preliminary test result for this integrated readout electronics.

Minioral:

No

Description:

Digitizer

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671

412 Design of Front End Electronics for direct dark matter detection based on LAr

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412

Design of Front End Electronics for direct dark matter detection based on LAr

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Liquid argon (LAr) with a high light yield of approximately 40 photons per keV is an attractive target for the direct detection of WIMPs, which are well motivated galactic dark matter candidates. In this paper, we present a front end electronics design for a LAr dark matter detector with the scintillation read out by PMT, which has an input dynamic range from 5pC to 1nC, and high resolution that single photoelectron can be distinguished. The design is consists of 8 preamplifier modules (PAMs), 2 Front end Digital Modules (FDMs) and a Trigger Clock Module (TCM). The FDMs are each equipped with two 14-bit 1-GSPS analog-to-digital converters (ADCs), and the performance of prototype FDM had been test in lab (e.g. Enob is 10.18 bits @175MHz). Moreover, this prototype FDM had been tested with LAr detector collaboratively and test results are also presented.

Minioral:

Yes

Description:

system

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Country:

China

621

408 The Proton Beam Realtime Monitor System in CSNS

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497

Data Acquisition System for the CSNS Neutron Beam Monitor

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At the first three instruments of the China Spallation Neutron Source (CSNS) in China, seven neutron beam monitors were installed and commissioned in August 2017. Each of these monitors has its own FPGA electronics and GUI acquisition program based on version 4 of the Experimental Physics and Industrial Control System (EPICS). In this paper we show how data acquisition, visualization and interaction with the experiment control system are laid out, as well as some first results and performance data.

Minioral:

Yes

Description:

Beam monitoring

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408

The Proton Beam Realtime Monitor System in CSNS

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To meet the increasing demand from user community, China is now building a world-class spallation neutron source, called CSNS(China Spallation Neutron Source). It can provide users a neutron scattering platform with high flux, wide wavelength range and high efficiency. CSNS construction is will completed in this year. There are three neutron instruments in CSNS, which are GPPD, SANS and RM. CSNS Experimental Control System is in charge of the operation of NS target and instruments.
In CSNS, proton beam current is used to normalize neutron flux. Proton charge is measured bunch by bunch and stamp the timestamp. This value is broadcasted to every instrument for online use and stored in database for offline use. A special system based on WR and LXI protocol was developed and several hardware was produced. And device driver, DAQ based on EPICS and analysis software were also developed.This paper will introduce the hardware and software design of this system. Some test and running result were also introduce in this paper.

Minioral:

Yes

Description:

Beam monitoring

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565

Vertical Slice System Demonstration of a Tracking Trigger using an Associative Memory Approach

It has become evident that the development of a Level 1 tracking trigger system is crucial for the success of the HL-LHC physics program at the CMS experiment. The high pile-up and high occupancy conditions anticipate an input data rate into the tracking trigger system of ˜100 Tbps. This, combined with the 4 s latency required the L1 track finding trigger stage introduce an unprecedented set of challenges requiring the most advanced real time processing technology. A silicon-based Level 1 tracking trigger system has never been realized under these conditions., It is therefore mandatory

to demonstrate its feasibility at the system level. Recently, the HEP community has made significant progress in the area of fast track finding using ASICs and FPGAs. This includes a successful vertical-slice demonstration for a CMS tracking trigger at Level 1 for the HL-LHC era, developed by a Fermilab/LPC R&D collaboration. The demonstration solves the data delivery problematic using an ATCA, full-mesh based, system architecture. It uses a fast pattern recognition algorithm, based on associative memories, that can be implemented on specialized ASICs, or on modern FPGAs when the pattern bank size needed is not very large, followed by precision track fitting implemented on dedicated FPGAs. The demonstration system achieved excellent performance in terms of tracking efficiency and momentum resolution, within a very short latency (2.5 s). The details of the demonstration will be presented, with highlights on the new techniques developed to address the unique challenges at the chip, board, and system level.

Minioral:

Yes

Description:

Tracking, AM

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Zhen Hu

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