Contribution ID: **494** Type: **Poster**

Improved thermal performance of an updated NSTX-U inner divertor

Wednesday 7 June 2017 13:40 (2 hours)

An improved inboard divertor has been designed for NSTX-U with higher divertor heat flux capability, robustness to halo current strikes and improved bakeout temperatures. The ATJ graphite inboard divertor tiles of the original NSTX-U design may have been subject to radial forces from halo currents which were not effectively resisted by the t-slot tile clamping. The clamping force could have been increased to resist these forces, but the stress in the t-slot cut of the tiles would have left insufficient margin for the thermal stresses induced by the divertor heat flux. In addition, due to an oversight during the design of the NSTX upgrade, one of the inner poloidal field coils, specifically PF-1b, was thermally close-coupled to the horizontal section of the inboard divertor flange, which was intended to be heated with hot helium during bakeout. This led to a compromise between achieving adequate temperature for bakeout and protecting the electrical insulation of PF-1b. NSTX-U was unable to achieve a proper high temperature (350℃) bakeout of the inner divertor. The new design of the tiles and their mounting system increases the thermal heat flux and halo current capability of the divertor and the thermal decoupling of the inboard divertor from the PF-1b allows proper bakeout in preparation for high performance plasmas in NSTX-U during the next run period.
This work is supported by US DOE Contract No. DE-AC02-09CH11466

Eligible for student paper award?

No

Author: Mr MARC, Sibilia (PPPL)

Co-authors: Mr BROOK, Arthur (PPPL); Ms CIUMMO, Carmela (PPPL)

Presenter: Mr MARC, Sibilia (PPPL)

Session Classification: W.POS: Poster Session W

Track Classification: Divertors and high heat flux components