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Optimal Design of a High Voltage High Frequency Transformer and Power Drive System for Long Pulse Modulators

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The stacked multi-level (SML) klystron modulator topology has been suggested as an alternative to conventional pulse transformer based topologies in an attempt to improve output pulse performance and reduce system size for long pulse applications. In this topology, a power converter chain including a high frequency transformer generates the output pulse in a pulse modulation/demodulation scheme, effectively eliminating the direct size-pulse length dependency while allowing higher degree of freedom in design.

However, increased complexity necessitates careful consideration from a system perspective to ensure appropriate component selection and design. First, from the perspective of the semiconductor switches, the pulsed nature of the load must be taken into account. High modulator average and peak powers are combined into a power cycling problem where lifetime issues must be managed when selecting semiconductor technology and converter operating frequency. Simultaneously, these considerations are directly coupled to the design of the high voltage high frequency transformer, the largest component in the SML chain, key in reducing modulator footprint and volume. In addition, appropriate passive components must be chosen with respect to transformer leakage inductance, switching frequency and switch ratings to constrain voltage overshoot without deteriorating system efficiency.

In this paper, these integrated design considerations are combined with a catalog of IGBT switches available on the market to form an optimization algorithm set to minimize transformer volume, indicative of system oil tank volume, while ensuring high system efficiency and long semiconductor lifetime. The impact of required system lifetime as well as tradeoffs between system efficiency and volume are studied. Finally, the algorithm is used to outline the design procedure for a system rated for pulse amplitude 115 kV / 20 A, pulse length 3.5 ms, pulse repetition rate 14 Hz, efficiency>90%, lifetime>25 years. The derived design is validated in both circuit simulation and through finite element analysis.

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