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Improving Fast SiC MOSFET Switching Using an Inductive Gate Drive Approach

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The use of solid-state semiconductor switches in compact pulsed power systems requires high-voltage, high-current, and fast switching capabilities. The recent advancements in wide bandgap semiconductor switches have allowed for development of SiC MOSFETs with increased hold-off voltage (from 1's to 10's of kV) and low on-state resistance (10's of mΩ) that are suitable for many of these pulsed power applications; however, robust gate driving techniques are required to achieve fast risetimes on the order of 10-20 ns necessary for proper operation. Due to the high dI/dt , and subsequent inductive kickback, experienced by the switching elements under pulsed conditions, parasitic inductance drastically affects the performance of commercially available totem-pole gate drivers. In addition, traditionally packaged MOSFETs exhibit further degradation of switching characteristics due to the introduction of additional parasitics.

Previously, an inductive gate drive approach, utilizing a high-voltage inductive kick to rapidly charge the gate capacitance, was able to achieve high turn-on dI/dt up to 25 kA/μs and risetimes less than 20 ns. Due to the high turn-off dI/dt associated with the MOSFET source inductance, long fall times greater than 50 ns resulted. This effect was exacerbated for the traditional TO-247 package. This paper details further improvements to the inductive gate driving topology, including expansion of the gate driving methodology to improve the turn-off time of the switching element, utilizing a similar negative inductive kickback to rapidly discharge the gate capacitance. In more detail, the effects of inductor value, peak inductor current, and MOSFET parasitics are examined. Verification and optimization of the gate driving circuitry is performed using SPICE simulations

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