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Load Capacitance Effects on the Energy Mechanism and Severity of Series dc Arcs

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As the power demands increase for airplanes, heavy duty electric vehicles and data centers, their dc bus voltages are expected to increase. While this reduces cable weight and improves system efficiency, electric arcs become an increasingly dangerous fault condition. Arcs fall under two categories—in series or in parallel with a load. Parallel arcs release large amounts of energy as high and low voltage electrodes are almost shorted, whereas series arcs act as an inserted impedance. Both parallel and series arcs can cause electromagnetic interference, insulation damage and fires. Parallel arcs cause large load current surges, which can be detected and handled with overcurrent protection. Series arcs decrease the load current, making them more difficult to detect than their parallel arc counterpart. Various detection methods and series arc models have been studied in the past. Although some models reflect the underlying phenomena, few explain how the occurrence and severity of series arcs are linked with load and source impedance of the circuit. Based on a large group of test data with RC loads and a fixed loop inductance, this paper derives a generic waveform and formalizes a two-stage energy mechanism to describe transients of series dc arc. These provide analytical insights into the effects of load capacitance. It is found that load capacitance plays a major role in arc severity, limiting the rate at which arc voltage rises, which is a critical factor on whether a sustained arc can be formed. The findings in this paper can be extended to constant power loads and guide future designs of loads with series arc prevention in dc networks.

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