Test Results of a 7.5 kA Semi-Conductor Prototype Switch as Modular Switchgear in Energy Extraction Systems for the HL-LHC Magnet Test Facility

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***Abstract*— The superconducting magnets, intended for use in the LHC High Luminosity (HL-LHC) project at CERN are based on Nb_3Sn technology. Powering of prototypes of such magnets with up to tens of kilo-Amperes is required for detailed studies of the quench behavior as well as an evaluation of the associated magnet protection equipment. For this purpose an ultra-fast energy extraction system is needed in order to prevent any overheating of the magnet conductors during the quench process. No commercially available opening switch is capable of rupturing a DC current of 30 kA in a solely inductive circuit, within one millisecond and under development of up to 1 kV. This has been the incentive for undertaking the development of such a switch. The choice was to use high-current IGBT's as static switches. This paper presents the arguments for the different choices of topologies and component selections for the 7.5 kA basic module of which four units are composing the final 30 kA switch. Specific features related to the design, the compensation techniques and the thermal considerations are highlighted. In particular, this paper describes a detailed presentation and analysis of all test results from type testing of the first module, including a comparison with the design phase calculations and the simulation results.**

Keywords—Energy Extraction; Magnet Protection; DC breaker

I. INTRODUCTION

The final energy extraction system will be installed in a dedicated test stand in the CERN superconducting test facility which is currently being modified to house a 4.8 m long vertical cryostat operated at 1.9K. As two identical power supplies of 15 kA/16V are used, it was decided to split up the total circuit in two parallel, 15 kA branches, grouped only at the magnet level. Fig. 1 shows the principle schematic for 30 kA powering with two parallel Energy Extraction Systems each rated for 15 kA and consisting of semi-conductor elements used as fast acting DC switches. Each 15 kA branch is composed of two identical 7.5 kA basic modules. The modules with a maximum continuous DC current of 7.5 kA are designed to allow easy paralleling. In the near future CERN will need fast DC switches, not only for 30 kA powering, but also for 10 kA and 20 kA circuits. Therefore, no other development is needed to cover these demands.

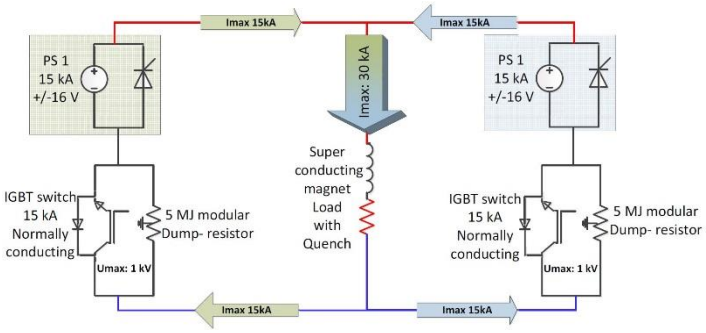

Fig. 1. Principle schematics for 30 kA powering

Fig. 2 is showing the two basic modules each composed of four high power IGBT elements.

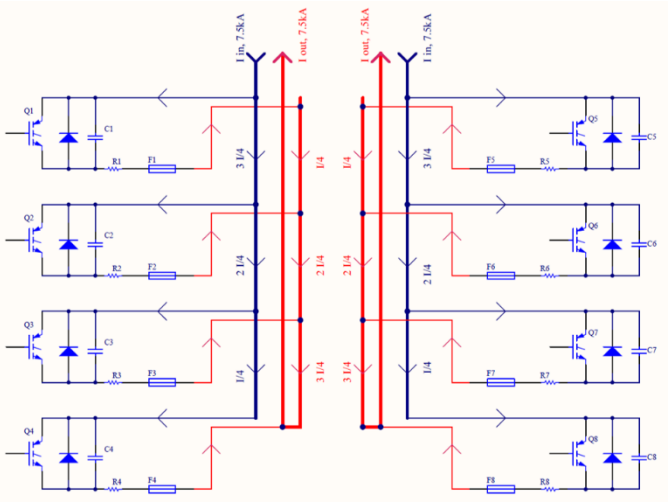

Fig. 2. Simplified presentation of a 15 kA switch system

The 7.5 kA main distribution bus-bars are mounted in a triplet configuration, with the main advantage of a full symmetrical design for each IGBT with identical resistance values for each branch. The overall compensation for stray fields

is respected since the sum of the vectorised currents is always zero, as shown in Fig. 3. The concept and design of the 30 kA Fast Opening Switch as Energy Extraction System, also focusing on the three levels of snubber capacitors as well shown in Fig. 4Fig. 3, is described in detail in the paper in press [1]. The current paper focusses on the test results for one 7.5 kA module, the various type tests performed and compares the measurement results with the simulation results.

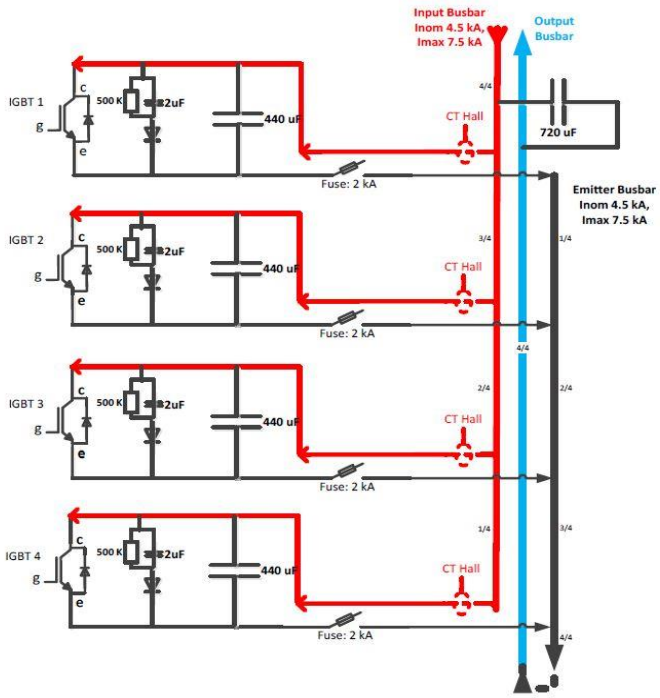

Fig. 3. Detailed schematics of a 7.5 kA module consisting of 4 parallel branches

II. Test Results

The goals of the performed tests are:

- Qualification of the functionality of the system.
- Proof the symmetrical design and the pursued current sharing within safe margins.
- Confirmation, during the opening process (transient mode) of the determined synchronisation of each IGBT and its repeatability.

A more detailed schematic is presented in Fig. 3, completed with three levels of snubber metallized film (MKP) capacitors and their total values. The first level, 720 µF, consist of two paralleled 360 µF MKP type power electronics capacitors. The second level, 440 µF, also MKP types but two 220 µF in parallel. Finally the third level consist of two paralleled MKP snubber capacitors of 1 µF each.

A. Individual Branch Tests

Each individual branch with its IGBT is tested separately in order to qualify the branch up to 2 kA for thermal validation as well as transients' evaluation to guarantee, during the commutation process, that the voltages and currents remain within safe margins.

B. Multiple branch tests

After successful testing of each individual branch the parallel branches were tested in different configurations. With two branches in parallel and later up to all four branches it was proven that:

- the current sharing up to the maximum values is under all circumstances within approximately ±2.5%
- During the opening process, the extraction curves as well as the transient curves are all identical. See Fig. 4 and Fig. 6.

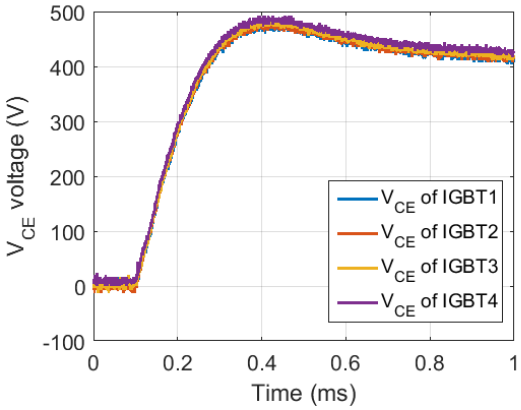

Fig. 4. Uce (driver level) - Four IGBTs in parallel extracting 7.5 kA on a 60 mΩ dump-resistor

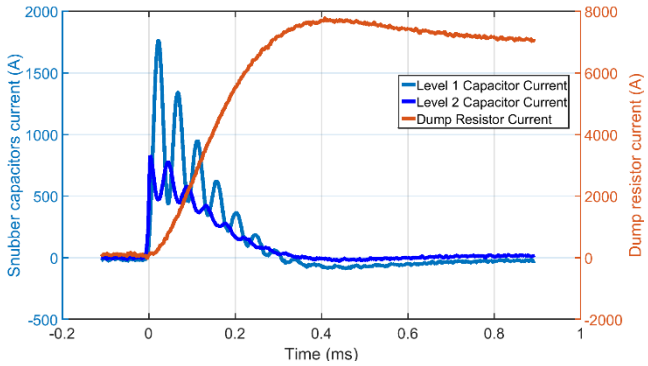

Fig. 5. 1st and 2nd level Capacitor and Dump-resistor currents during extraction 7.5 kA on a 60 mΩ dump-resistor

Fig. 4 shows the collector-emitter voltages of each IGBT measured at the driver level, meaning a high impedance path that remains unaffected by the potential rise due to the high current through the terminal resistances and other parasitical ohmic resistances.

Fig. 5 is showing the currents through the different elements. The current through the 1st and the 2nd level snubber capacitor is depicted alongside to the current towards the dump resistor. In absolute values each capacitor absorbs 50% of the total branch current of 1875A.

The conclusion of these tests is that all branches feature exactly the same impedances. Having the required synchronisation from the driver side, the opening process is fully identical for each branch without additional over-voltage over or over-current through the individual IGBTs or capacitors.

C. Snubber capacitor optimisation

The third level snubber circuit, responsible for reducing the fast transients generated by the IGBT switching, is optimised for a single switching-off process. Several different snubber solutions, like C, RCD and CRCD, were tested before deciding on the final configuration. The challenge is to optimize the snubber topology, as each additional element has its own stray inductance (of a few nano-Henry), which is reducing the overall efficiency. The overall snubber circuitry, including the PCB, should be designed in such a way so to reduce the stray inductance to a minimum. Theoretically, for off-switching the best snubber circuit from a stray inductance point of view is a capacitor in parallel to the IGBT. In this way the snubber circuit itself can be very compact and the connection leads as short as possible, e.g. one can install the MKP capacitor directly onto the IGBT's terminals. But, in combination with the other levels of snubbers (capacitors to compensate the stray inductances of the distribution bus-bars) and with the stray inductance between these two types of the snubbers, a resonance loop is created with a ringing frequency of approximately 0.5 MHz. A peak voltage of approximately 60 V is generated and damped within a few periods as shown in Fig. 6.

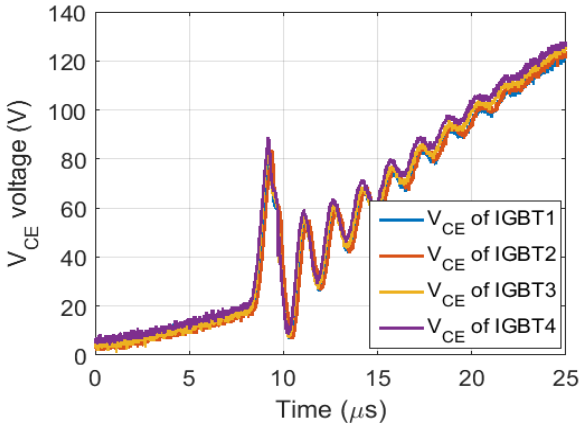

Fig. 6. Fast transients with CRCD snubber at 7.5 kA extraction and Master-Slave configuration

To minimize this peak voltage and to increase the damping, a diode was installed in series with the capacitor. Because of the diode's relatively high internal inductance, it is not possible to reduce the spike completely. Also a combination of such a DC-snubber with another parallel capacitor was tested but in all cases the diode's inductance is dominant. Nevertheless a reduction of the peak voltage by approximately 50% was obtained. A RCD snubber circuit, with optimized connection layout (minimised parasitical inductance) was implemented as final solution and using this configuration only a 30V spike is present but, because of the diode influence, without ringing as shown in Fig. 7.

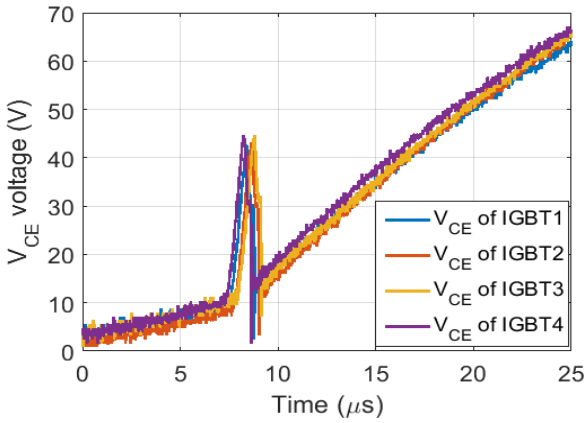

Fig. 7. Fast transients with RCD snubber at 7.5 kA extraction having a Four Masters configuration

For further reducing the fast transients that occur at the initial stage of off-switching, it was chosen to increase the turn-off gate resistor from 4 Ω to 15 Ω. Therefore, the energy stored in the stray inductance of the branch bus-bars will partially be dissipated inside the IGBT, additionally damping the voltage spikes. The switching time increased approximately from 1 to 10 µs. The configuration with all 4 branches identically delayed by 10 µs was tested as well and confirmed the increased damping.

Taking into account the total snubber capacitance of approximately 2.48mF per 7.5 kA module, the duration of the total "opening" process lays between 0.5 and 1 ms, depending on the dump resistor value which varies from 240 mΩ down to 6.6 mΩ. All fast transients occur at the very beginning of the voltage rising, i.e. just above zero volt level. If the dump-resistor is configured for lower values than 60 mΩ, a slower voltage overshoot (see Fig. 4, Fig. 13 and Fig. 14) appears across the dump resistor (related to the total energy extraction system C and R-values). This has no influence on the total circuit current decay (L/R) and therefore neither on the protection of the superconducting magnet (see also chapter IV).

D. Heat run

1) Component temperatures

The temperatures of the various parts of the complete system and more specifically of the IGBTs are important parameters of the switch and their evolution in time has to be observed continuously during operation. This is due to a plethora of reasons. The absolute maximum temperature but also the temperature swing affects the lifetime of the IGBT. Therefore, in order to maximize the lifetime, the base plate temperature is kept around 40°C and will be monitored to assure that the temperature remains around the specified value, regardless of the duration of the operation.

2) Current sharing

Additionally, a positive coefficient correlates the on-state losses of the IGBT to the temperature. This creates a feedback loop that improves the current sharing among the four IGBTs. The observation of the current sharing evolution in time is the second reason for performing a long time continuous run.

3) Shunt resistor

Originally, a shunt resistor of 25 μΩ was connected in each IGBT branch, intended for measuring the branch current but also increasing the current sharing mechanism. Its removal was decided for the following three reasons. Firstly, the obtained voltage signal correlated to the branch current was small and therefore the signal/noise ratio as well, leading to a less accurate measurement. Secondly, the appearance of stray elements has inherent time delays, thus a high bandwidth signal acquisition requires complicated compensation methods. Finally, the existence of this resistor increased substantially the temperature on the elements connected to it or placed above them.

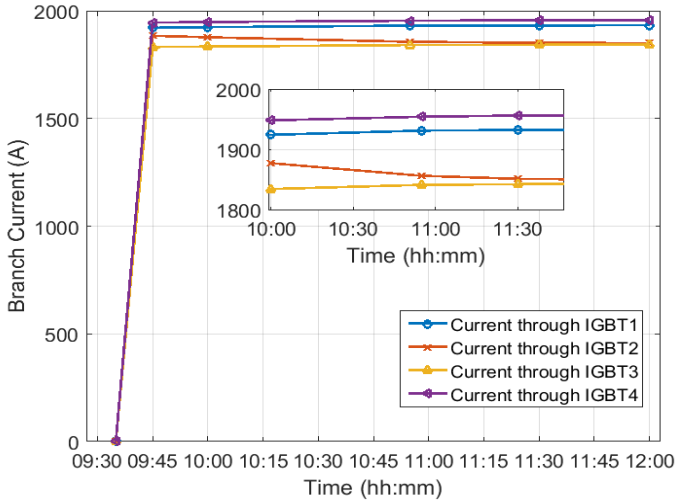

Fig. 8. Branch currents and current sharing over time

4) Heat Run Results

The heat run presented here was performed without shunt resistors and the current sharing rests exclusively on the thermal coefficient of the IGBTs and its internal connection resistances. It was important to observe whether this is sufficient or not.

With the shunt resistor removed, the current through the IGBTs was measured using DC current transducer sensors, and the measurement of those in time, depicting the current sharing is presented in Fig. 8.

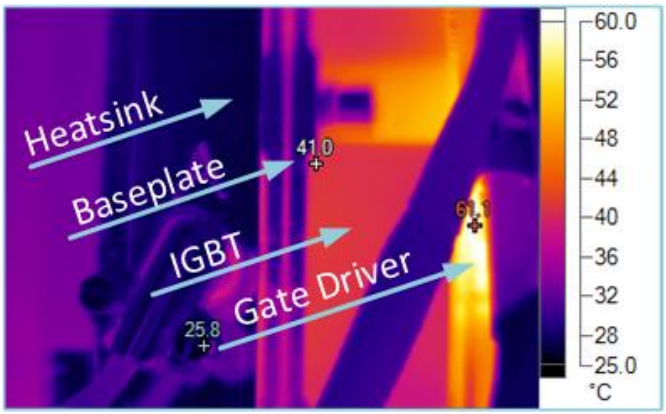

Fig. 9. Base plate and heatsink temperature after 8 hours of heat run

For the temperature recording a Fluke Ti400 IR camera was used and the results can be seen in the figures 9 and 10. In Fig. 9 the temperature of both the IGBT baseplate and the water-cooled heatsink are depicted. It can be noted that between the initial stages of the heat run and at the final stages, the baseplate temperature appears stable and close to the designed temperature of 40 ºC.

Additionally, the temperatures of the connection points at the collector and emitter terminals to the branch bus-bars have been recorded.

The temperature of these points at the end of the heat run can be observed in Fig. 10 alongside with the temperature across the branch bus-bars which does not exceed the design temperature of 40 ˚C.

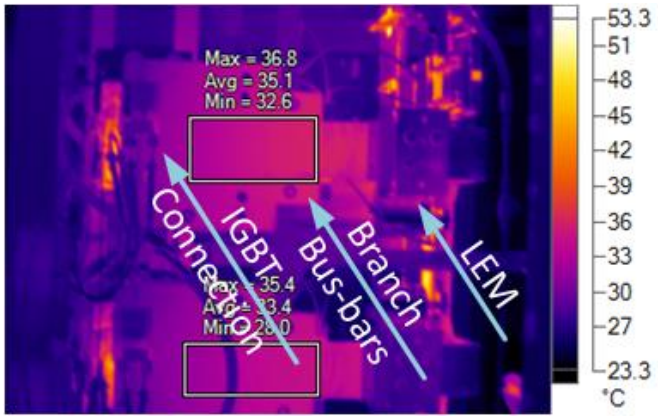

Fig. 10. Temperature at connection points and busbars

E. Electronics and Controls System

The command and controls system are kept as simple as possible but taken in account the extreme importance of the switch functionality, having to open in case a quench is detected, the system has to be extremely reliable. A careful selection of the components involved are at the base of this objective in conjunction with the redundancy of the critical functions, e.g. the hardware current loop opening switch. Many temperatures, currents and voltages are processed primarily by off-the shelf hardware, a CompactRIO platform from National Instruments ™. Those parameters are monitored by the firmware and when passing pre-set thresh-holds the compact-RIO system will interact with the purposely developed hardware part of the command and controls system. All the switch parameters and actions can be remotely controlled and observed via an Ethernet connection. The command and controls system developed for the 7.5 kA module will be described in more detail in a future publication.

III. FAULT SCENARIOS

The principle of energy extraction using DC switches in circuits powering superconducting magnets eliminates a certain number of fault scenarios. Firstly, in monopolar powered circuits, no reverse voltage will ever occur. Secondly, from a load and powering point of view, no short circuit currents can be generated. However, when using larger numbers of IGBTs in parallel, several fault scenarios could lead to severe damage of superconducting parts of the circuit in case of quenches or to the energy extraction system itself, namely a short circuit of one or

more branches during the commutation process and unsynchronised switching of the IGBTs.

The short circuit issue for the particular IGBT is not yet tested knowing that the probability of such a failure is extremely low, especially taking into account the maximum current, maximum voltage and temperatures of the IGBTs wafers, which all have a huge margin with respect to the maxima mentioned in the datasheet. Temperatures, water flow, collector-emitter voltages and branch currents are all monitored and stored in logging databases. The controls system will prevent operation under any conditions out of specification. A R&D program treating short circuit situations is planned for early 2017. A back-up solution in form of a triggered fuse in series with each IGBT is considered and still under investigation. For more details see [1].

An IGBT switching off later than all others will lead to overcurrent in the related branch. According to simulations a delay up to 10 µs, between the different branches within one module of 4 IGBTs, will not lead to transient currents and voltages out of the Safe Operating Area (SOA). However, these transients are not the ideal switching scenario, might cause differences in the current in and voltage over the branches, affecting the IGBTs and snubber capacitors' lifetime.

A. *Artificial switch delay of one gate driver*

For observing the effect of a delayed gate driver, one out of the four drivers was modified by increasing the gate resistance, to obtain a switch delay of approximately 10 µs. Such a delay does not represent a realistic delay that might occur in any stage between the electronics and the gate driver, but was chosen in order to observe the behaviour of the switch, when the upper limits of the SOA are reached due to such a fault. The delay only caused higher currents through the snubber capacitors of the 2nd level but all numbers stayed within the maximum allowed values. Delaying further wasn't experimented since simulations show that more than 10 µs delay leads to higher than nominal rated DC current through the delayed IGBT.

B. *Four Masters Configuration*

For performing verification tests on each individual branch an independent control of each gate driver is required. Such a control cannot be achieved with the preferred Master/Slave configuration. For this reason, four independent Master drivers were chosen and the possibility of controlling the IGBTs independently was investigated. Such a topology would not only allow for flexibility at R&D level, but also for remote re-calibration of the measurement devices, such as Uce and branch current transformers.

After this configuration was implemented, the fault scenario that was discussed in the previous subchapter emerged. Due to the time spread of the optical transmitters and receivers needed in each Master channel, a Δt of approximately 500 ns was observed (see Fig. 11) whereas the Master/Slave configuration lead to a spread of 20ns. As a result, the collector-emitter voltages were also shifted in time with about 0.5 µs total spread (see Fig. 12). The appearance of this spread verifies that the scenario of the delay is realistic as well as that the upper limit of 10 µs provides sufficient margin for the delay that could appear between the gate voltages.

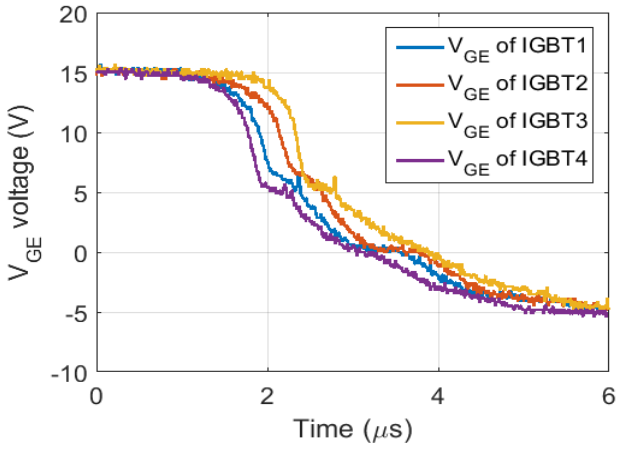

Fig. 11. Four Masters Configuration, 0.5us delay on the level of the gate signals

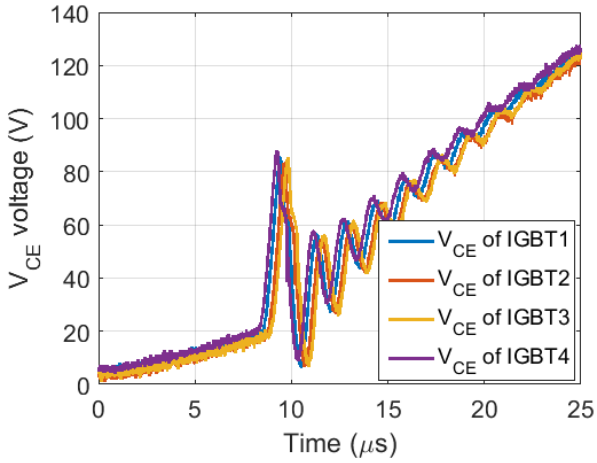

Fig. 12. Four Masters Configuration, CRCD snubber, 0.5us delay on the level of Vce signals

The result from the tests with different snubber- and drivers configurations shows that the optimum behaviour is achieved using the combination RCD-snubber and Master-Slave configuration for the drivers. In this way all transients for the branches are kept as low as possible and identical. In terms of maximum voltage and current spikes and the related energy as well as high frequency oscillations the margin is very comfortable and leaves room for fault scenarios such as late off-switching to up to more than 10 µs.

IV. Transient Response and Simulations

It was shown in Fig. 4 and Fig. 5 that during the switching operation of the opening process, a slow transient behavior appears within the time scale of a few milliseconds. This transient behavior was studied for different dump resistor values and the only components responsible for this are the total snubber capacitance, the stray inductances and the resistance of the dump resistor. The resulting oscillation frequency, more visible in Fig. 13 which represents the Uce voltage, is approximately 1.6 kHz. By assuming a simple RLC circuit and a capacitance of C = 2.48mF, for this frequency an inductance

of L ≈ 4 μH is calculated. Such a stray inductance value has been previously associated with the stray inductance of the dump resistor, the corresponding cable and power connections. This observation proves that the transient behaviour of the switch is independent of the inductance of the magnet under test.

Based on these measurements, a model of the switch which incorporates the stray elements was developed, such that it can approximate with a high accuracy these transients. It can be seen in both Fig. 13 and Fig. 14 that an excellent match has been achieved to the experimental measurements, with emphasis to correct prediction of the initial overshoots. The development of this model will allow for investigation of the effect on the various stray elements to the operation of the single switch as well as the complete 30 kA system as displayed in Fig. 1.

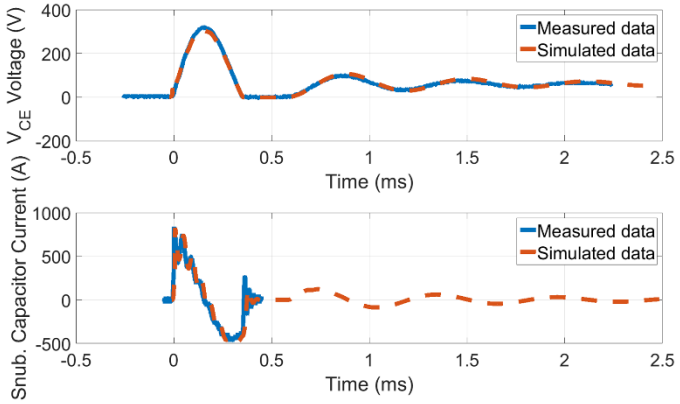

Fig. 13. Transient behavior during switching of the Uce as well as the 2nd level capacitor current for a dump resistor of 6.67 mΩ

By observing Fig. 13, it can be seen that the Uce oscillations are not allowed in the case of 6.67 mΩ dump resistor to take negative values. This is due to the freewheeling diode, integrated to each of the IGBT modules, becoming forward biased when the IGBT voltage becomes negative. For this reason, the Uce voltage gets clamped at zero volts for the duration that it would normally oscillate negatively.

The aim of the simulation model is to successfully predict the effect that stray elements and inherent asymmetries to element values will have to the current sharing during normal operation, as well as to the transient behaviour during the switching phase. Lastly, this simulation model is critical for performing an in-depth investigation of the possible faults that can occur and the results will provide aid to mitigate the effect of these faults.

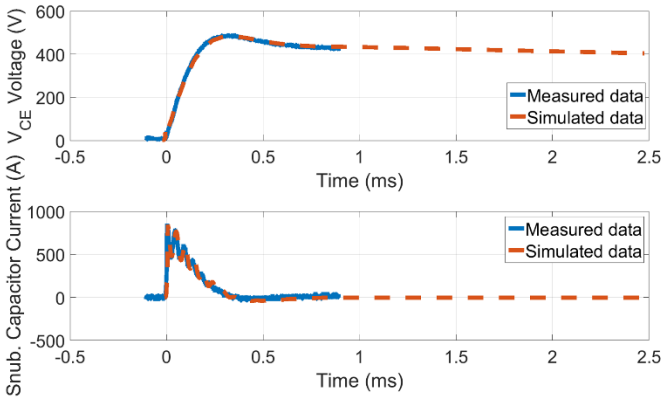

Fig. 14. Transient behavior during switching of the Uce as well as the 2nd level capacitor current for a dump resistor of 60 mΩ

V. Conclusions

An improved design for housing the IGBT Switch from the one presented in [1] was developed. The transient behaviour of the switching process was fully analysed and the conditions that optimize it have been investigated and discussed above. The system successfully operated continuously for up to 8 hours proving its operational and thermal stability. All the above allow for proceeding to the next important stages of the project; paralleling initially 2 and later 4 such systems, for implementing a 15kA and ultimately a 30 kA energy extraction system.

This development is a premiere for energy extraction systems at CERN and the accomplishment of an important milestone within the recently approved High-Luminosity LHC project.

Acknowledgment

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References

[1] K. Dahlerup-Petersen, G. J. Coelingh, A. Dinius, A. Erokhin and F. Rodriguez Mateos, A High-current, IGBT-based Static Switch for Energy Extraction in Superconducting Power Circuits - Concept, Design and Production of a 30 kA Fast Opening Switch, July 2016 [2016 IEEE International Power Modulator and High Voltage Conference, San Francisco, California]