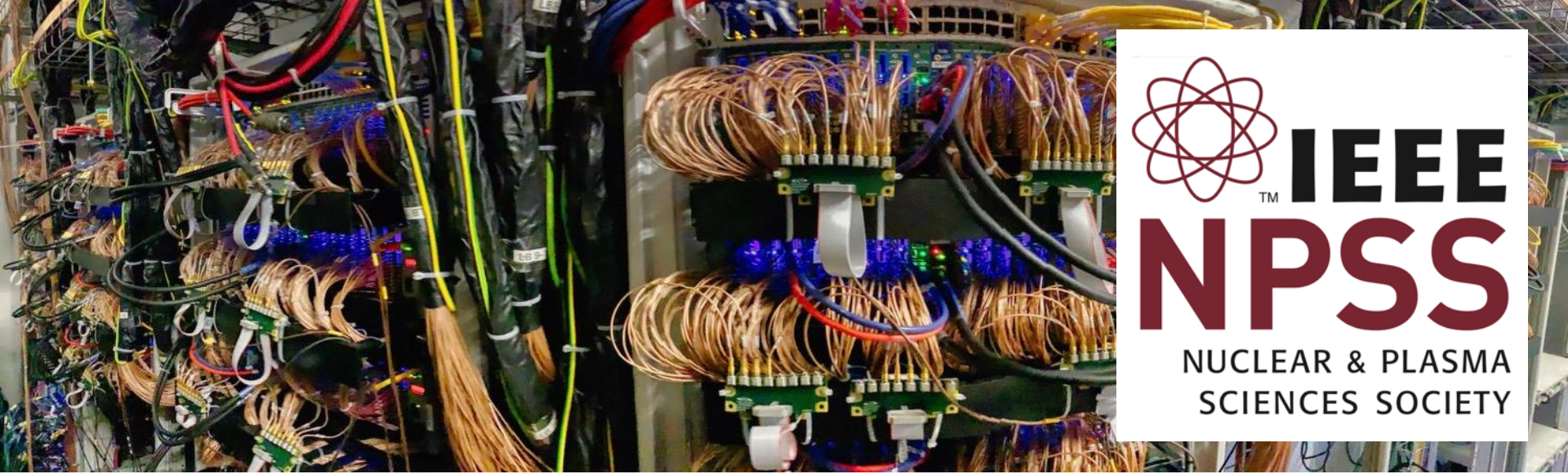


Measuring Picoseconds and GHz

Stefan Ritt, Paul Scherrer Institute, Switzerland

IEEE NPSS Prague EduCom International Summer School

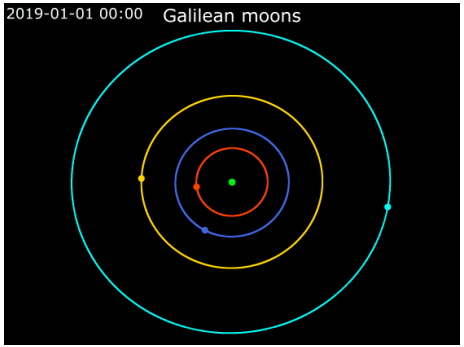
June 30th, 2025, Prague, Czech Republic

Stefan Ritt

- Studied in Karlsruhe, Germany
- Postdoc Univ. of Virginia, USA
- Head of muon physics group at PSI, Switzerland
  - Developer of MIDAS DAQ system https://midas.triumf.ca
  - Developer of DRS4 chip https://www.psi.ch/drs
  - Developer of ELOG electronic logbook https://elog.psi.ch/elog/
  - Co-spokesperson of Mu3e Experiment https://www.psi.ch/mu3e
  - Fellow of IEEE NPSS society https://ieee-npss.org
- Hobbies: Biking, Scuba diving, Drone flying, 3D printing

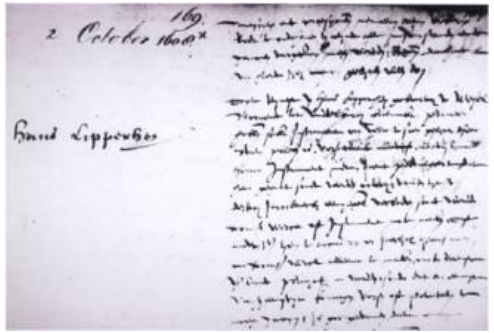
Discovery and Instrumentation

In 1610
Galileo Galilei
discovered four
Jupiter moons



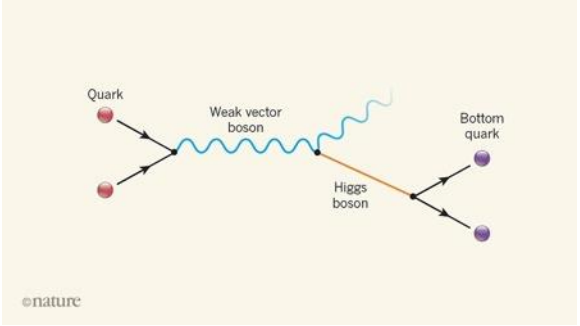
Jean-Leon Huens, National Geographic

In 1608
Hans Lippershey
filed a patent for
a telescope



← what was more important? →

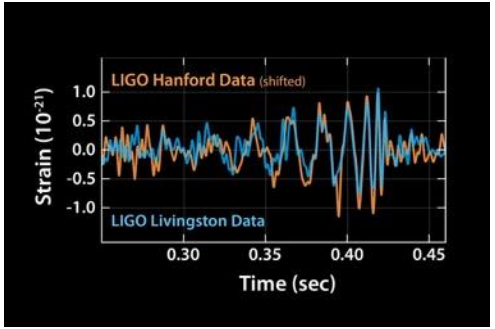
Recent discoveries



Higgs Boson

2013

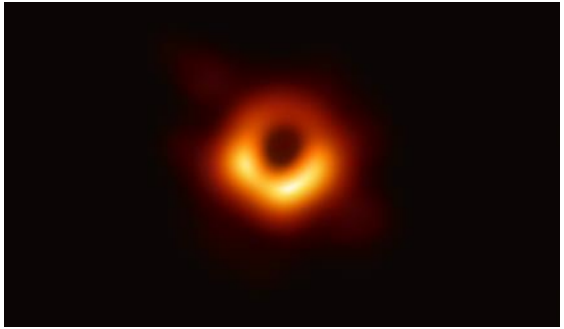
LHC Detector



Gravitational Wave

2017

Ligo Detector



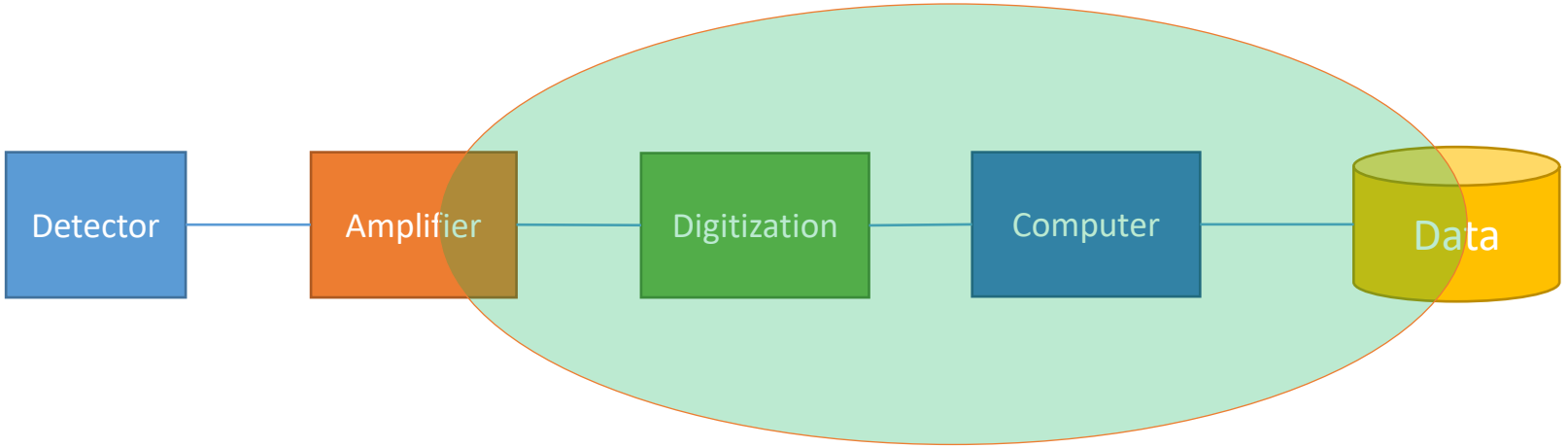
Black Hole

Event Horizon Detector Network

Importance of Instrumentation

- Behind most discoveries lies an essential development in instrumentation

From Detectors to Data

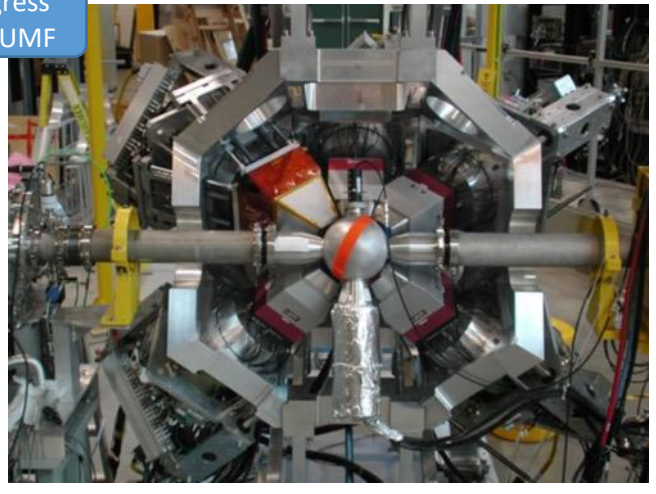


This Talk

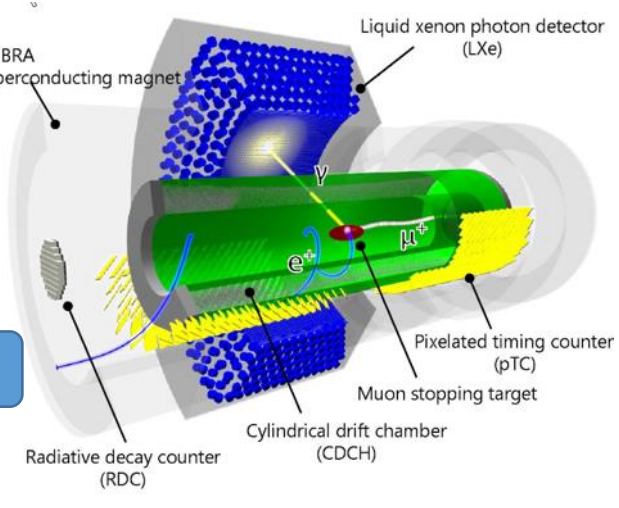
Measured quantities in Particle Physics

- **Position** → position sensitive detectors
- **Time** → resolutions down to ps
- **Energy** → calorimeter
- **Momentum**, **Charge** → curvature in B-field

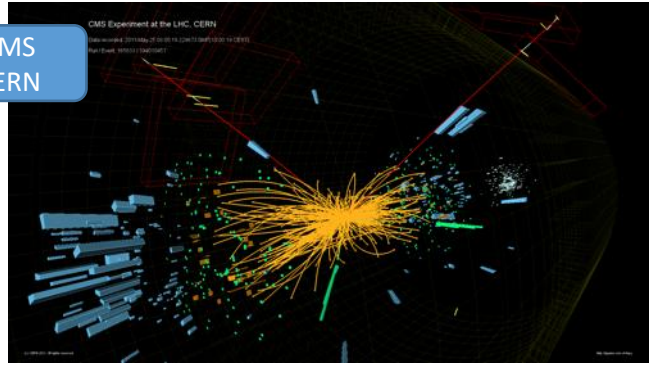
Tigress
TRIUMF



MEG
PSI



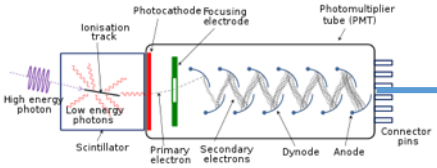
CMS
CERN



Particle Detection

- Old days: Looking **by eye** at scintillators

- Today: Converting detector signal into **electronic signals**



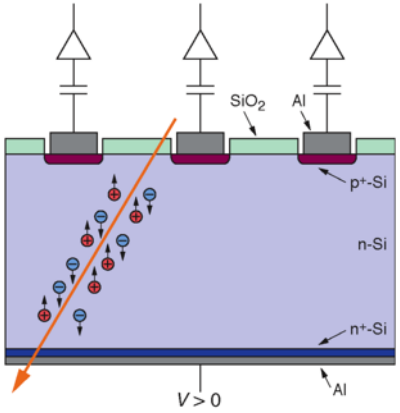
Digitization

Computer

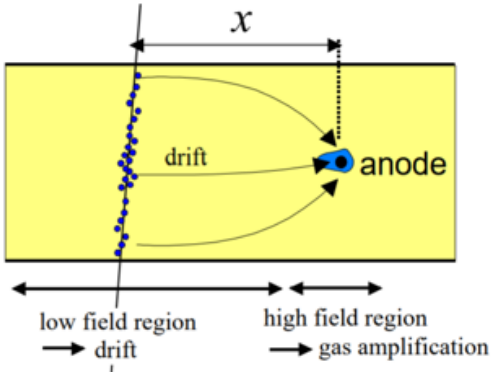
2 Principles of Detection of Ionizing Radiation

1. Detectors convert **property** to be measured directly into **electrical signal** → **position, time**
2. **Indirect** via light generation in scintillator → **energy, time**

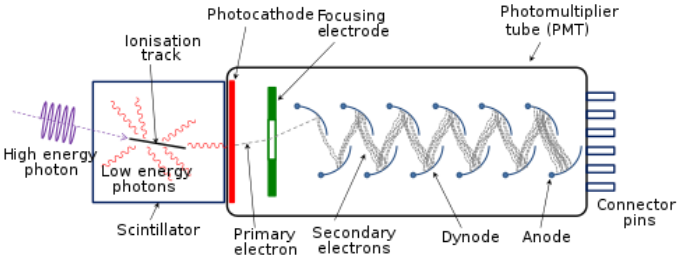
→ See other Lectures



Silicon detector



Wire chamber



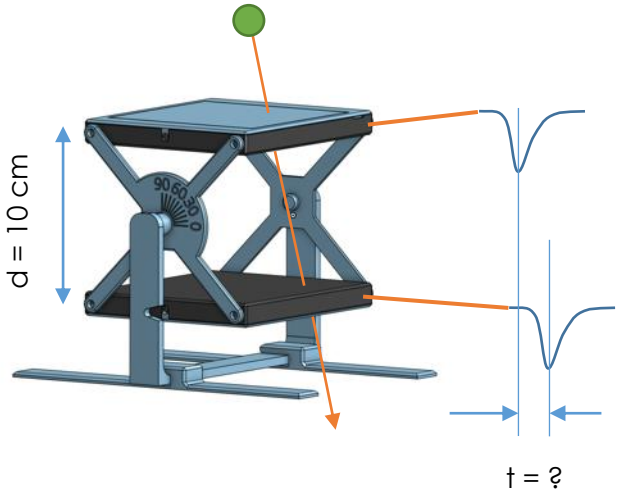
Photomultiplier

Signals and Electronics

How we process the information from detectors

Signals are fast!

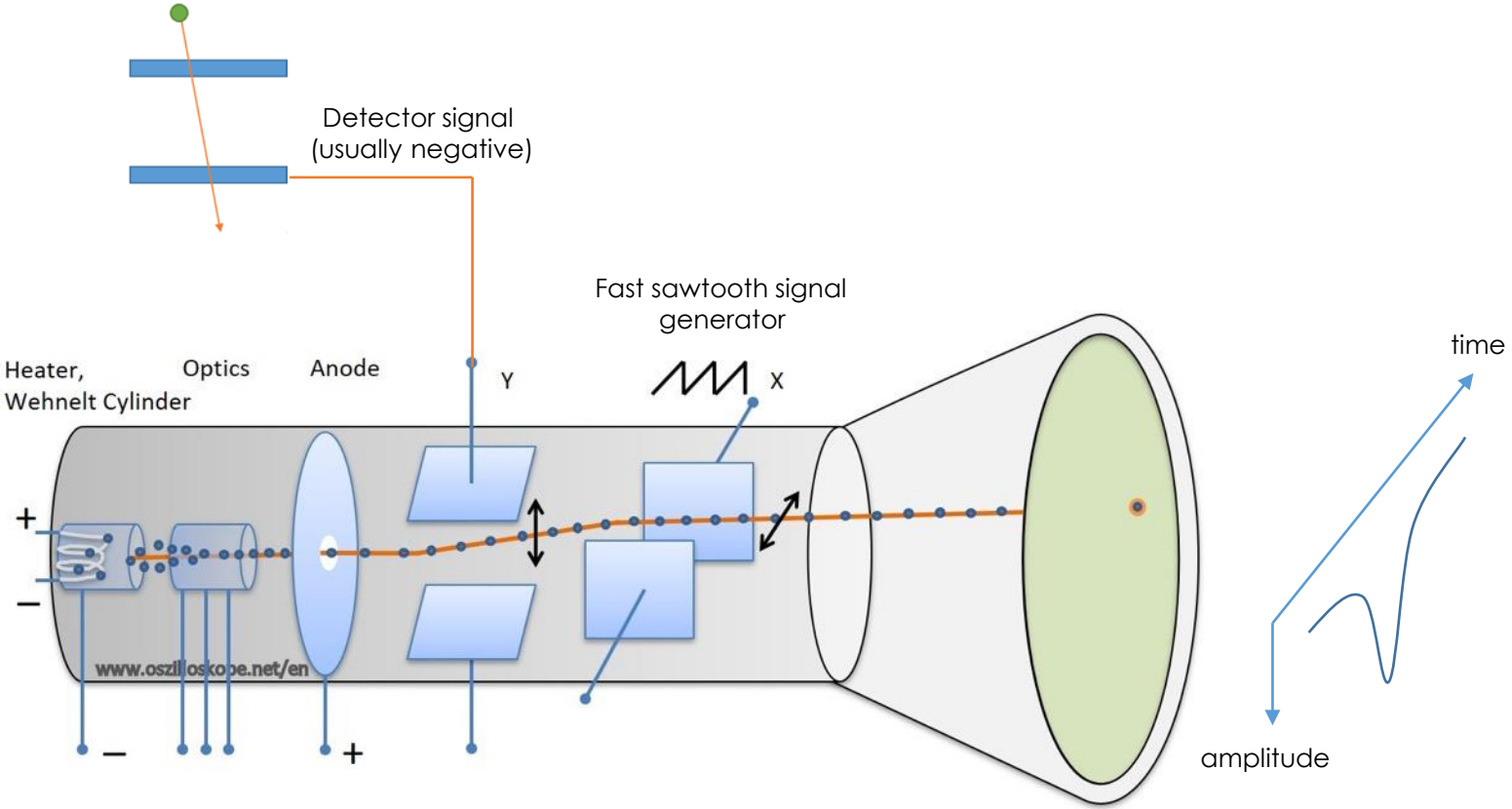
- Cosmic Muon with 90% speed of light hits two detectors 10 cm apart
- What is the time difference between the two signals?



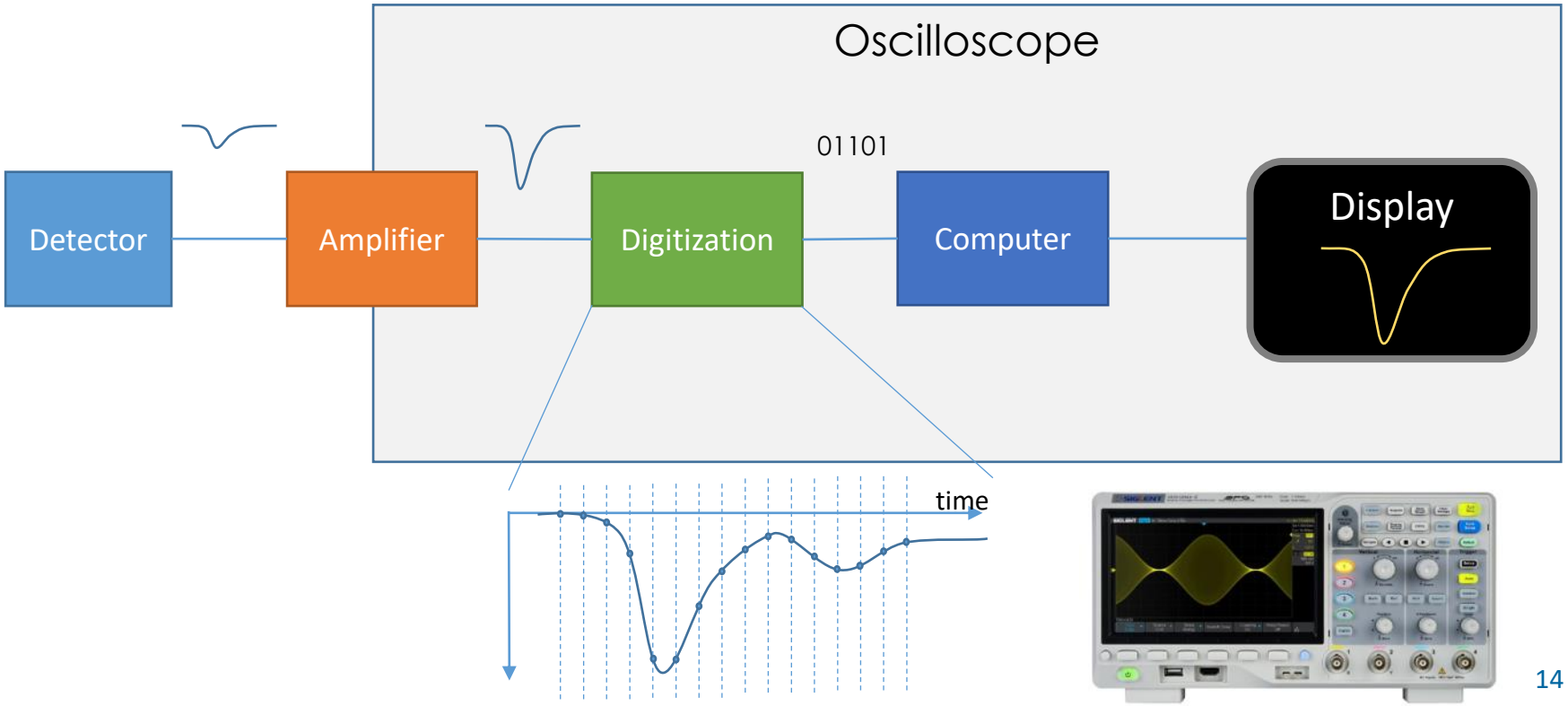
$t = d / v = 0.1\ m / (0.9 * 3*10^8\ m/s) = 0.0000000004\ s = 0.4\ ns$

You need a fast clock!

Principle of an oscilloscope

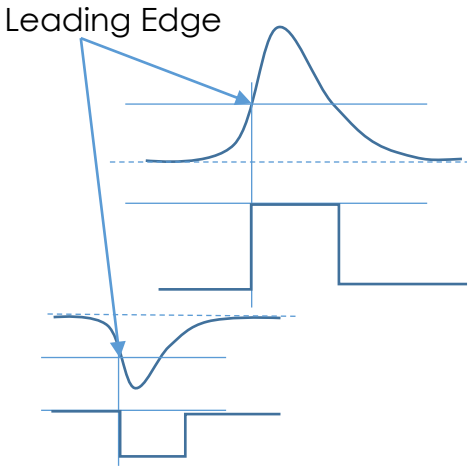


Modern Digital Oscilloscopes

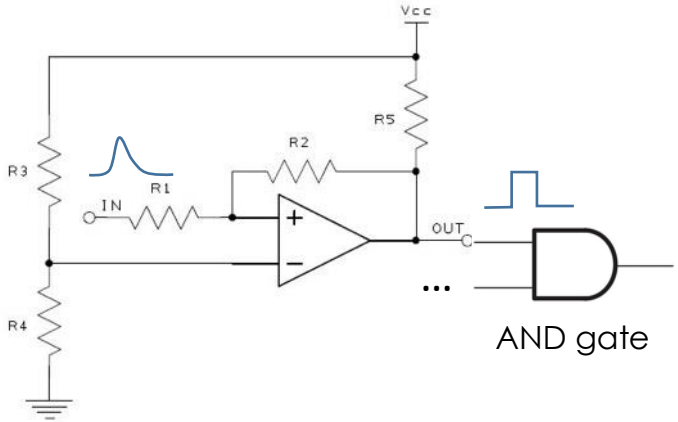


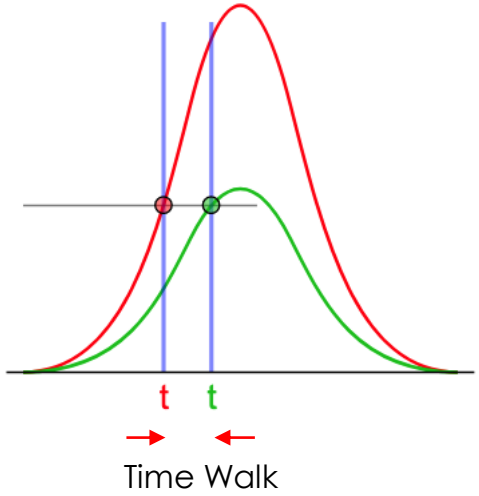
Signal Discrimination

- Convert **analog** detector signal to **digital** signal
  - **Digital** signal can be processed in **logic** and **computers** ("0"/"1")
  - Good for **detection** and timing
  - Problem: "**Time-walk**" effect



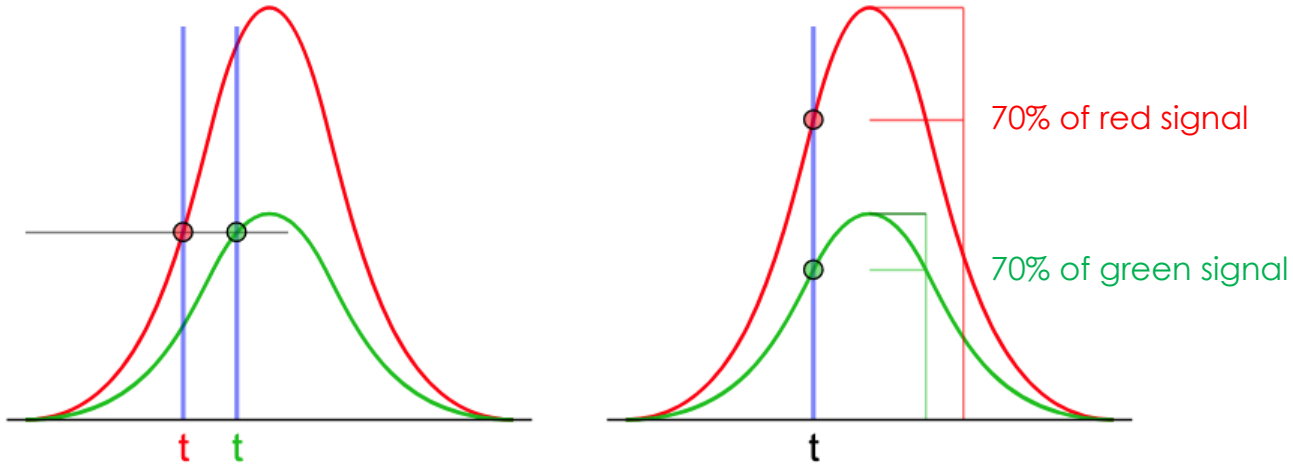
Comparator



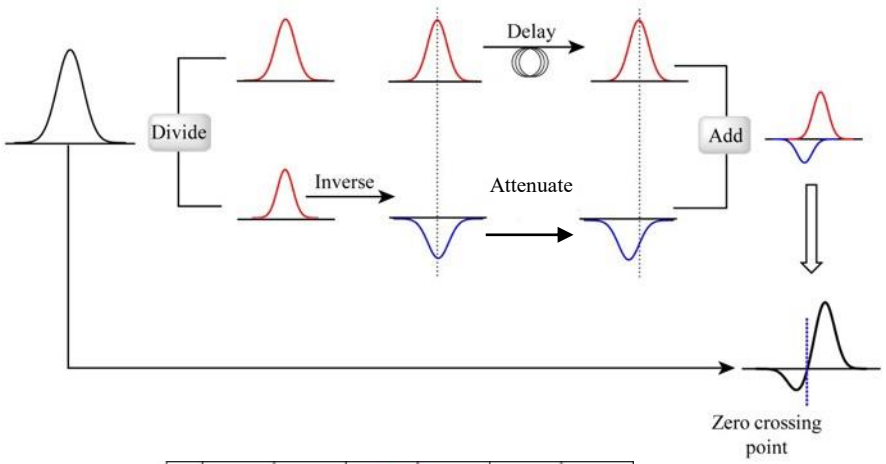


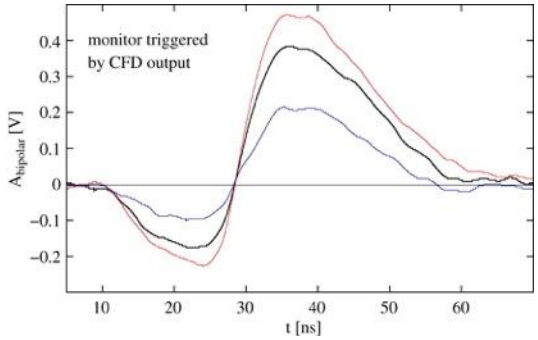
Signal Discrimination

- **Constant Fraction** Discriminator (CFD) triggers **independent** of signal amplitude
- Trick: do not trigger at constant threshold, but at **constant fraction** of signal amplitude

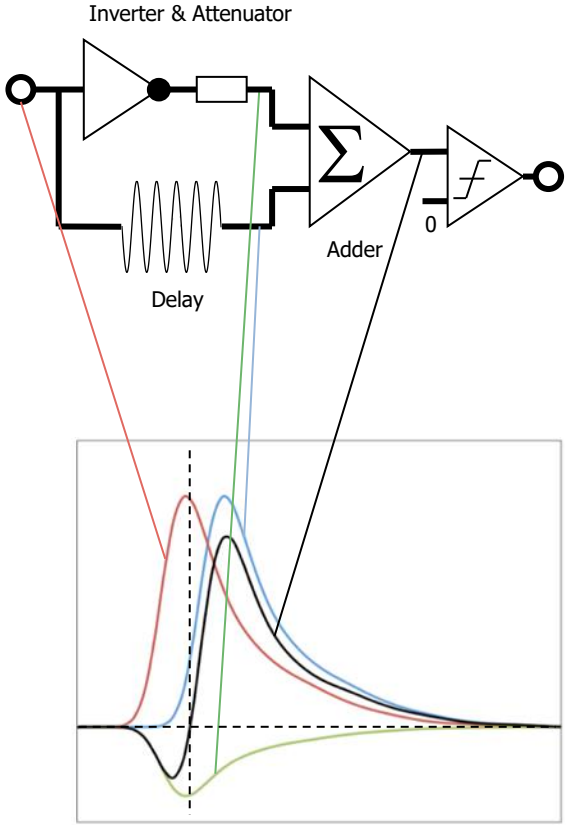


Implementation of a CFD





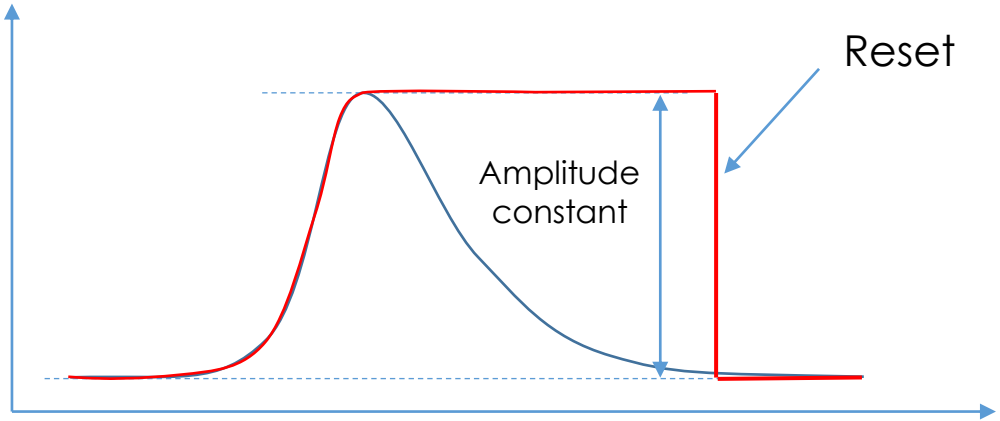
https://doi.org/10.1016/j.nima.2012.04.088



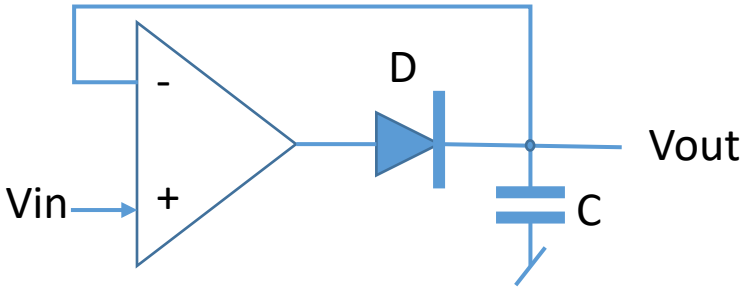
Analog-to-Digital Conversion

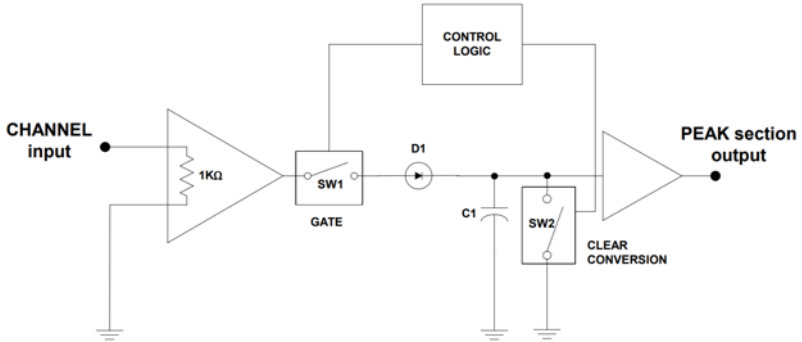
ADCs and More

Digitization: Peak-sensing ADC

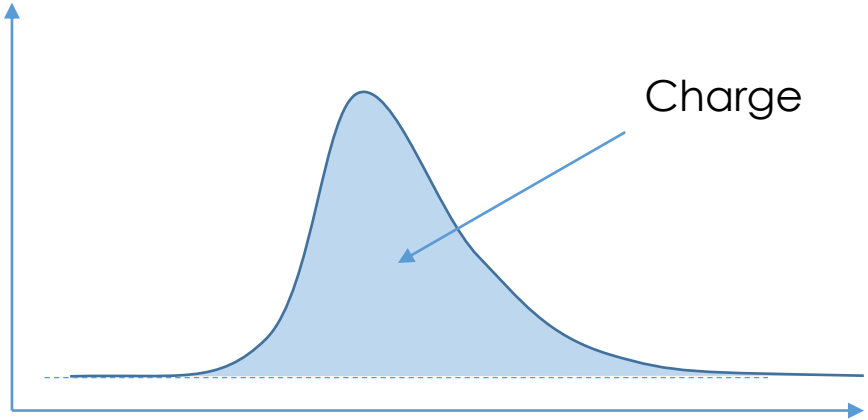


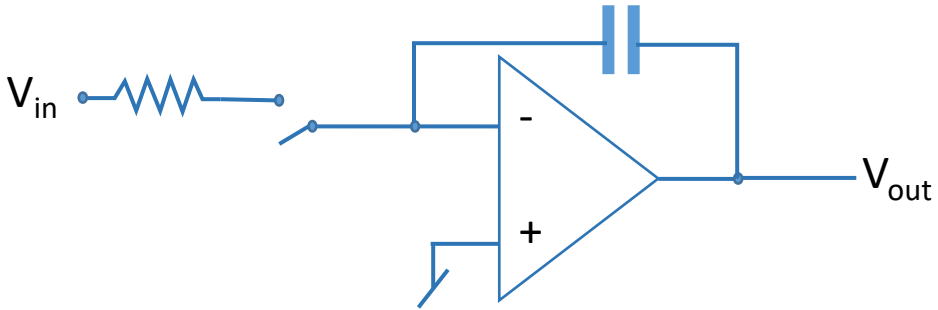
- Technique to digitize **fast** signals with **slow** ADCs
- Needs **reset** after each signal
- Mainly **historical**



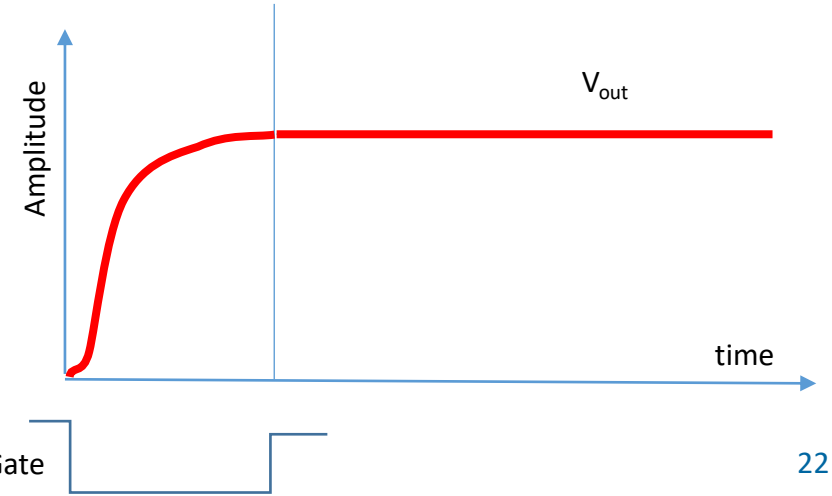


Digitization: Charge integration



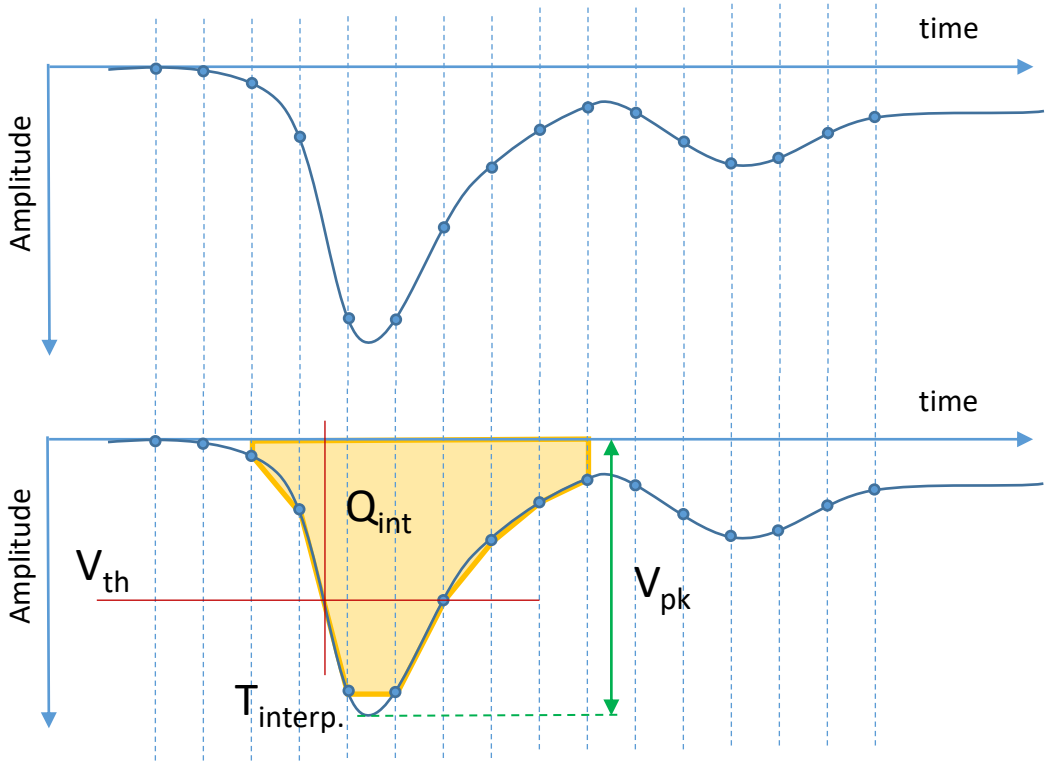


- Many detectors have a **proportionality** between **charge** and particle **energy**
- Noise **immunity**



Digitization: Waveform sampling

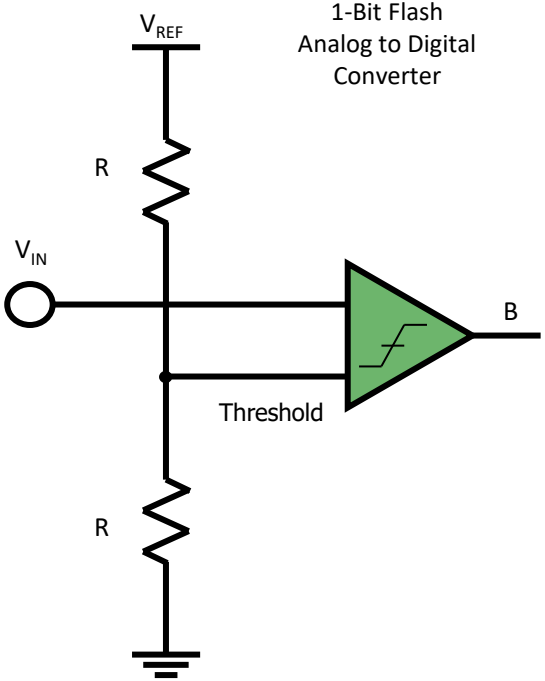
Sample waveform at discrete points (sampling rate) and extract features in digital world

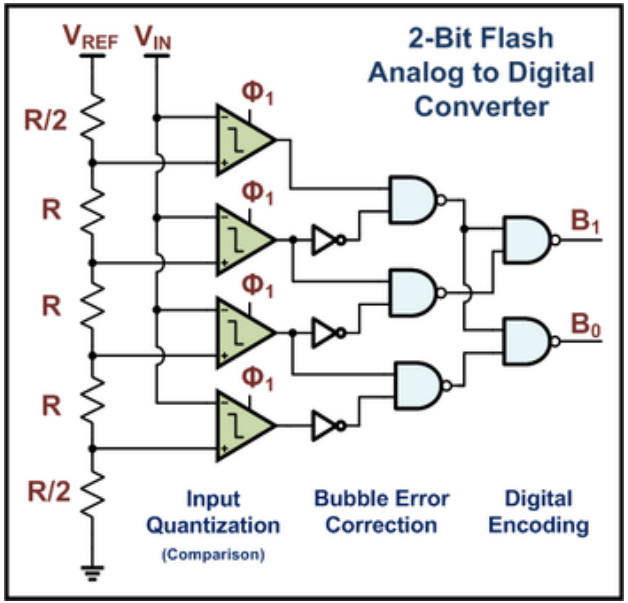


ADC Type	Resolution (bits)	Conversion rate
Dual Slope	12-20	100 sample/s
Successive approximation	8-18	10 Msample/s
Flash	4-12	10 Gsample/s
Pipeline	8-16	1 Gsample/s
Delta-sigma	8-32	1 Msample/s

Digitization: Flash ADC 1-bit and 2-bit

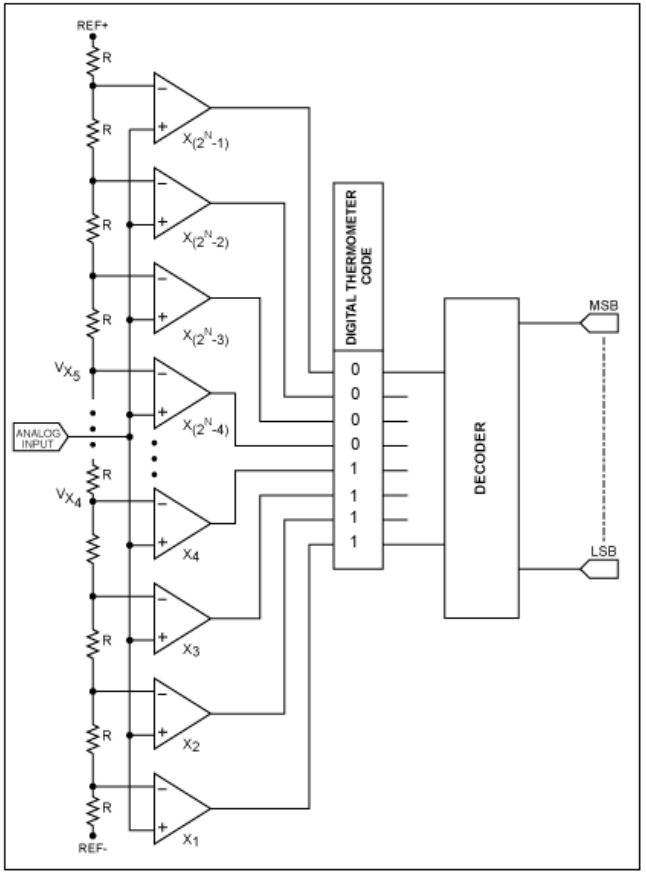
A voltage cannot be measured directly; you can only compare it with another one



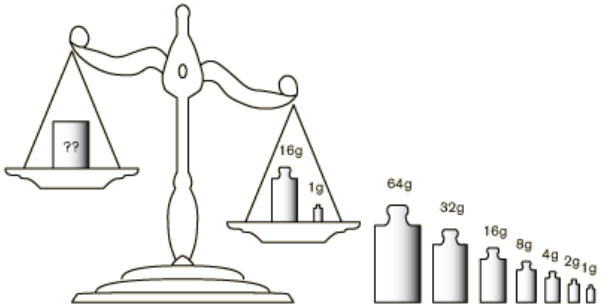


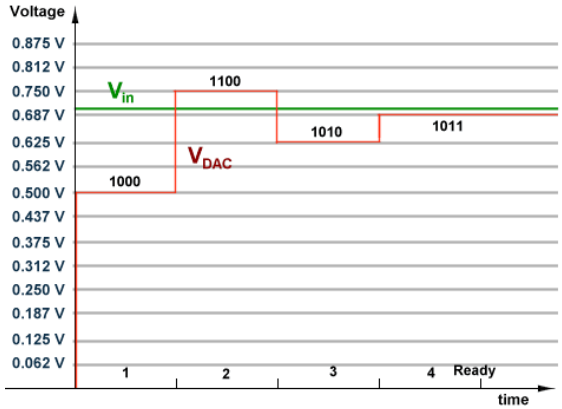
Digitization: Flash ADC n-bit

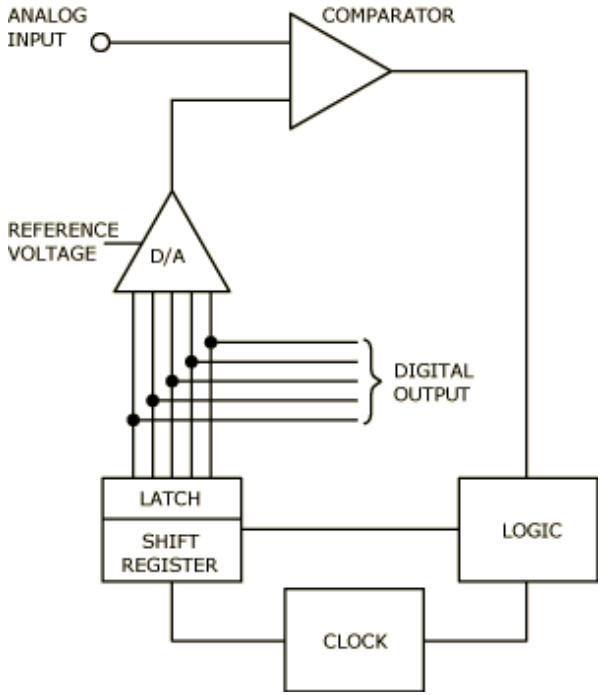
- Flash ADC very **fast**
- Requires **2^n** comparators
- Typically **<=8 bit** resolution



Digitization: Successive approximation ADC

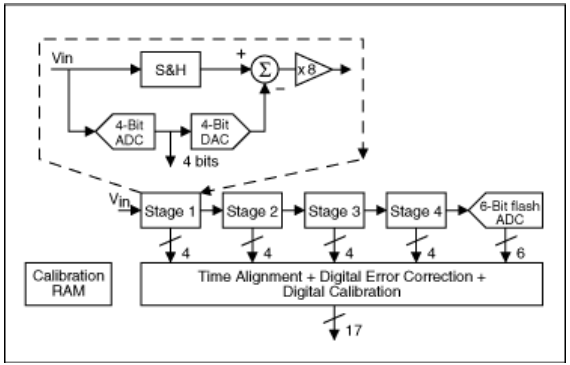


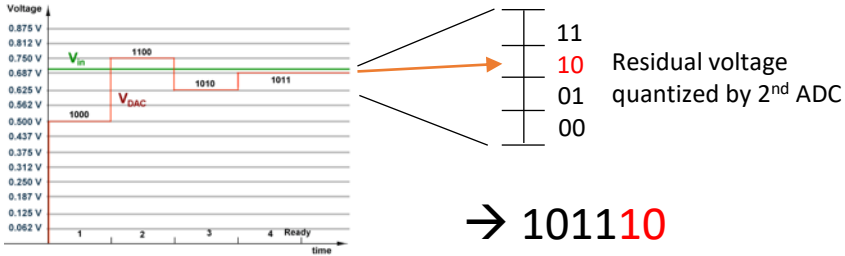




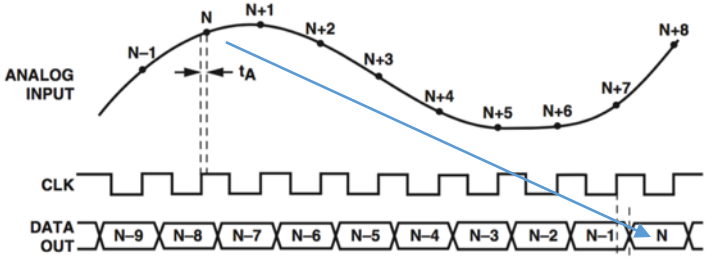
Digitization: Pipeline ADC

- Combine **several flash ADCs** with successive approximation logic
- Only requires **4-Bit** flash ADC
- Can convert **one sample** in each **clock cycle**
- Has a **latency** depending on the number of pipeline stages
- Most common technology for fast ADCs b)

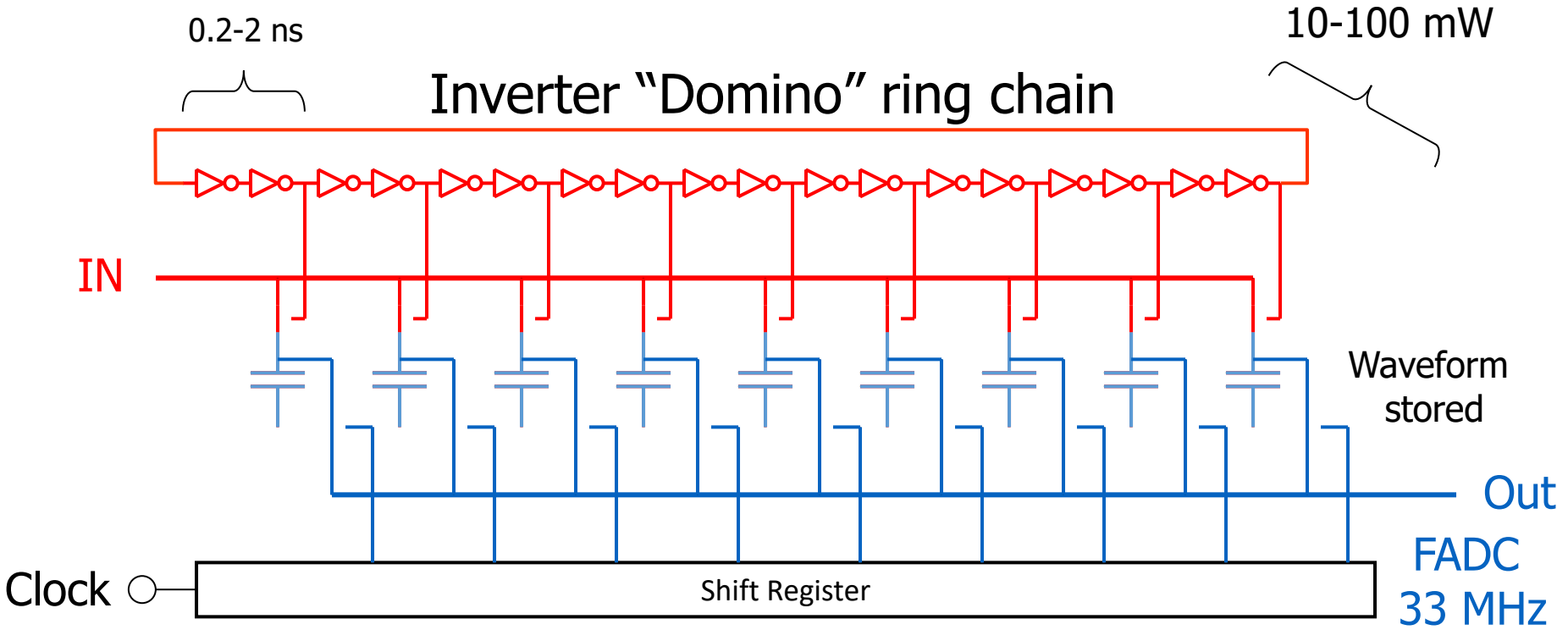




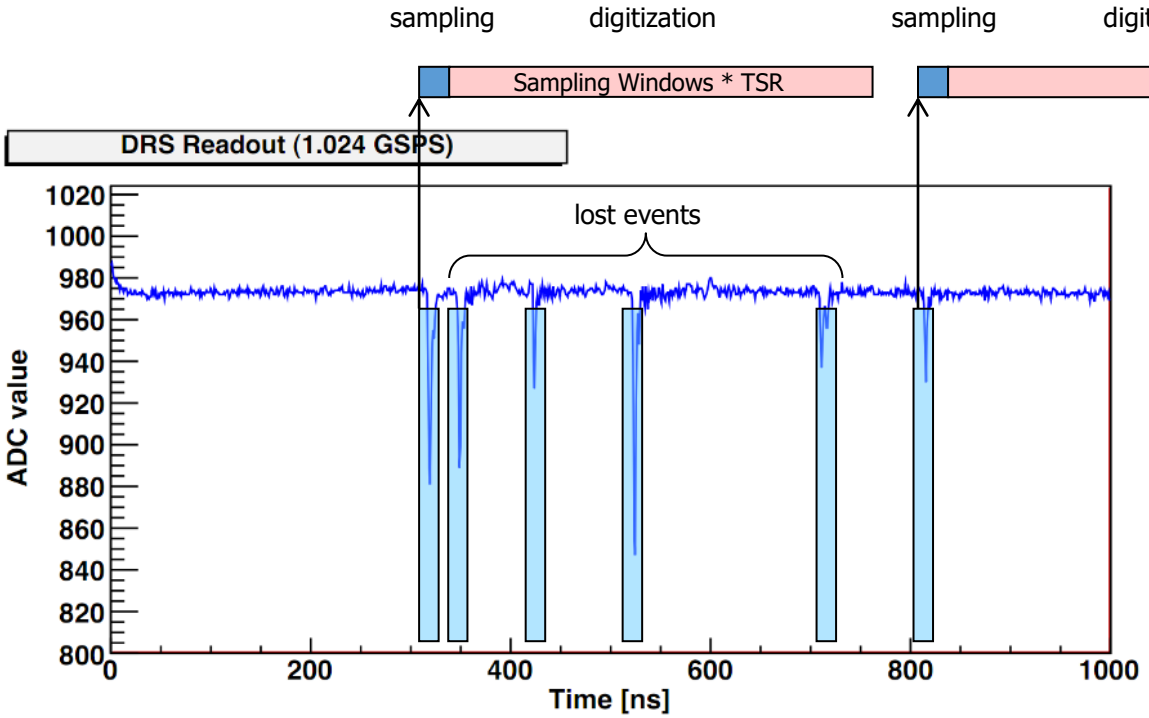
→ 101110



Digitization: Application Specific Integrated Circuit (ASIC) for Waveform Sampling: Switched Capacity Arrays (SCA)

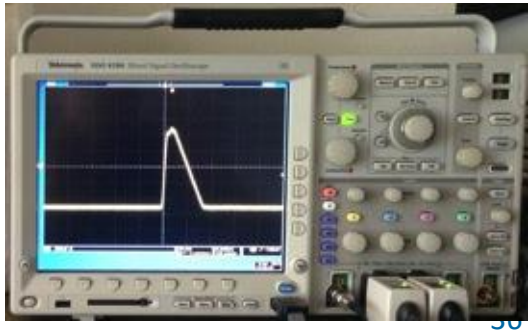


Triggered Operation



Dead time =
Sampling Window · *TSR*

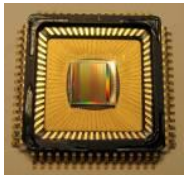
(e.g. 100 ns · 60 = 6 μs)



Chips usually cannot sample during readout ⇒ "**Dead Time**"
Technique only works for "**events**" and "**triggers**"

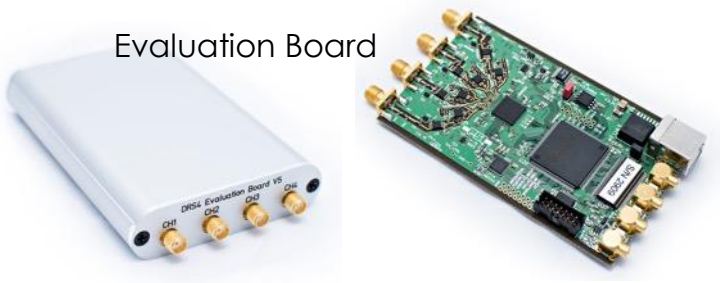
DRS4 Chip

- Developed at PSI in **2008** together with R. Dinapoli
- **5 Gsamples/s**, 12 bits resolution, 8+1 channels, 17.5 mW/channel
- Time measurements down to **10 ps**



DRS4 Chip

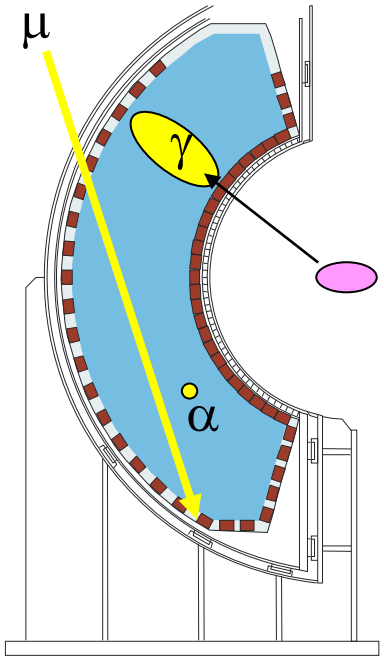
Evaluation Board



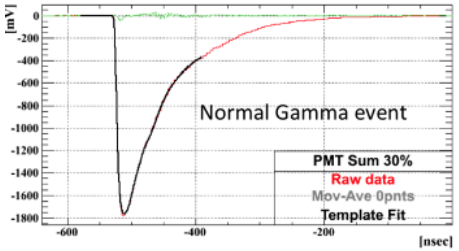
9000+ channels of MEG II, PSI

WaveDREAM Board

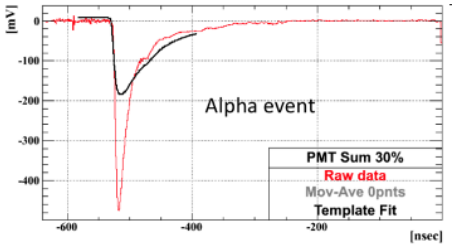
Pulse shape discrimination



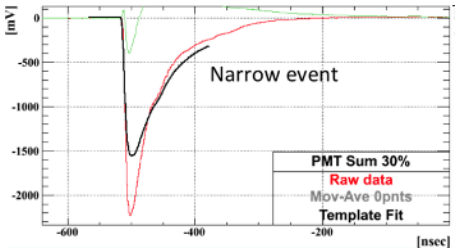
γ



α



μ



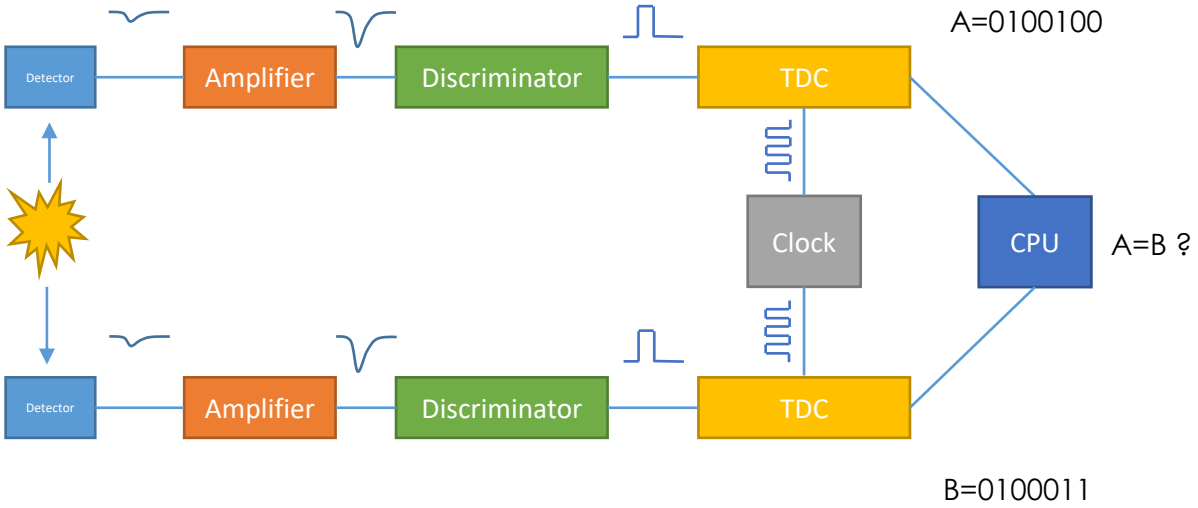
Events found and correctly processed
2 years (!) after the data has been taken

Time-To-Digital Conversion

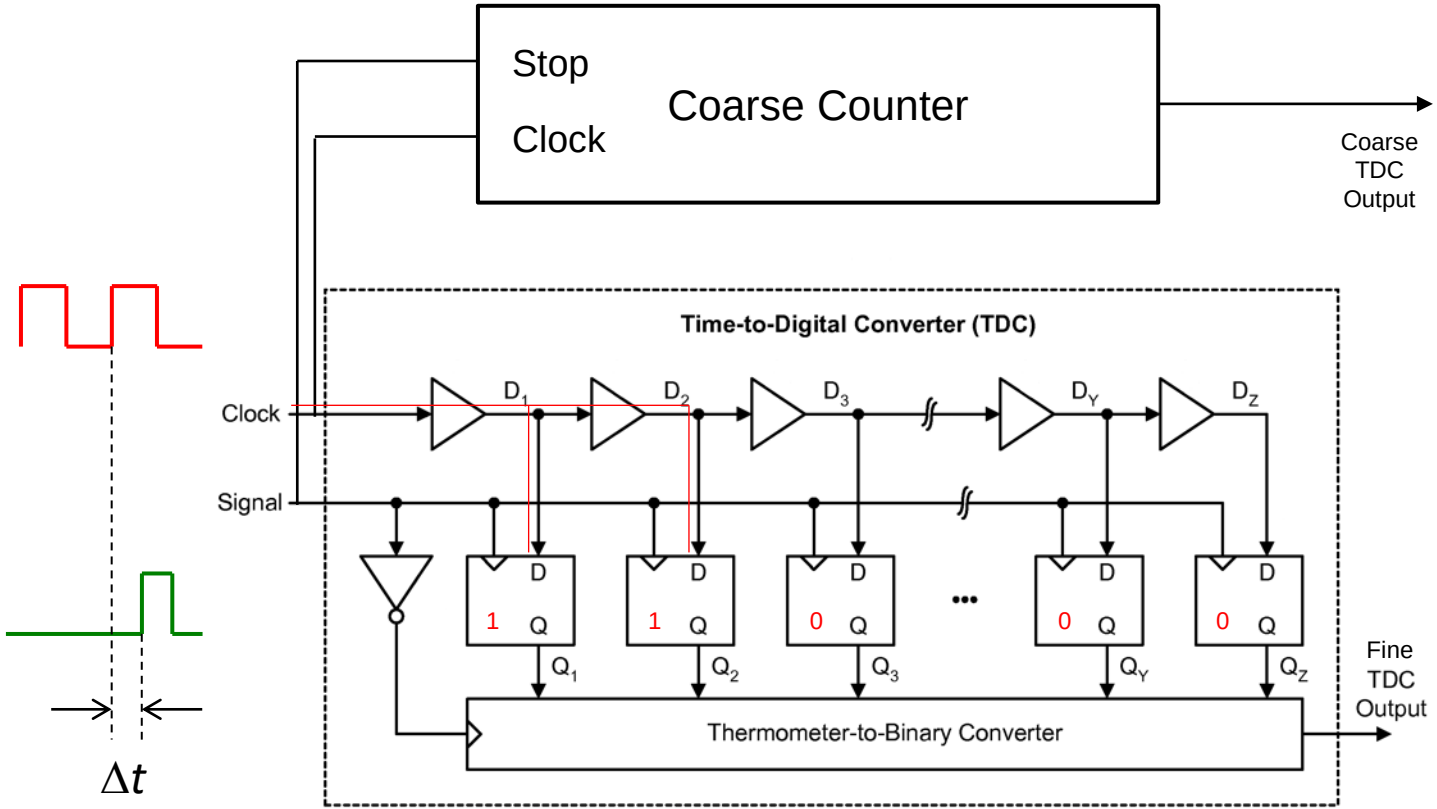
TDCs

TDCs

- Often it is enough to know **time** of event
- **Time-to-digital** converter to measure relative time



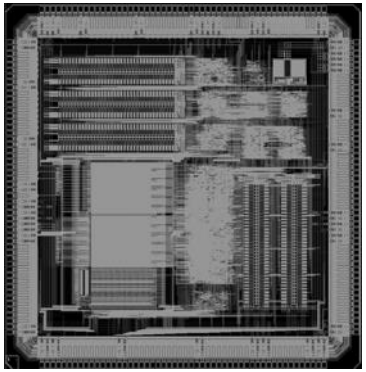
Digitization: Time-to-digital Converter

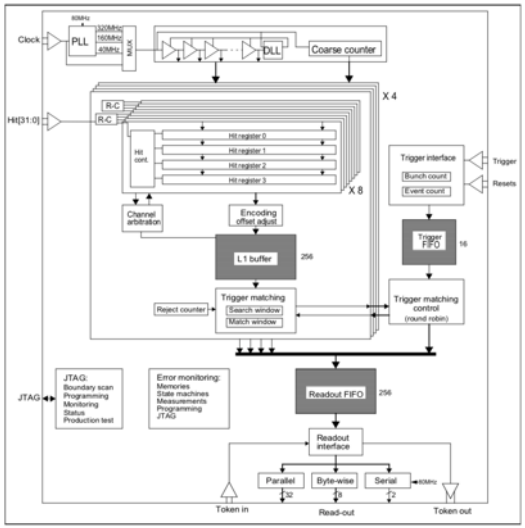


Examples of TDCs

HPTDC (CERN)

32 channels, 17 ps resolution

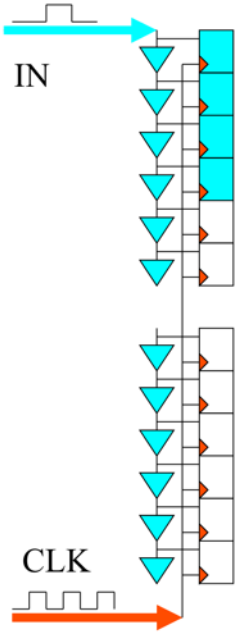


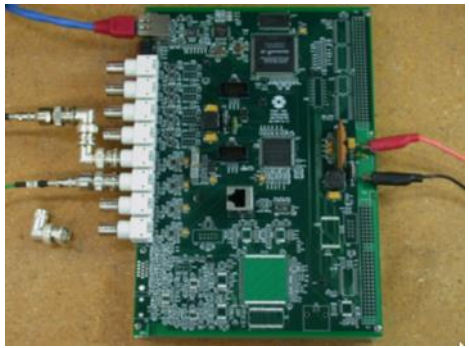


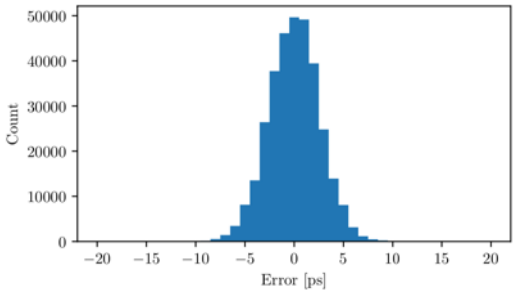
FPGA TDC

Jinyuan Wu (Fermilab): 32 channels, 10 ps resolution

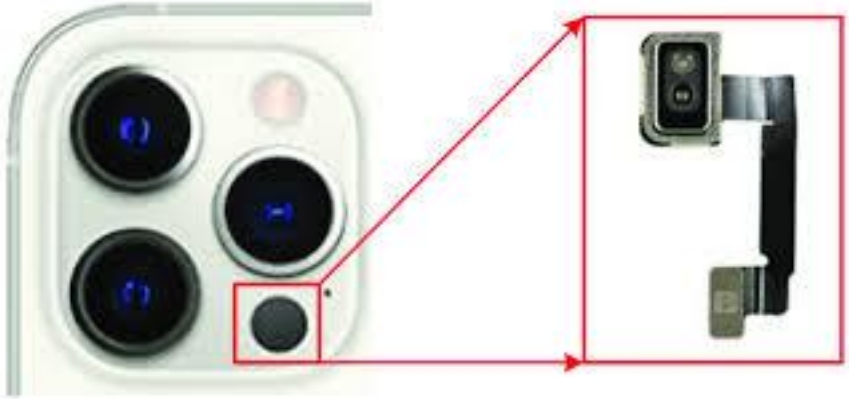
Sven Engström (Linköping Univ.): 1.8 ps resolution

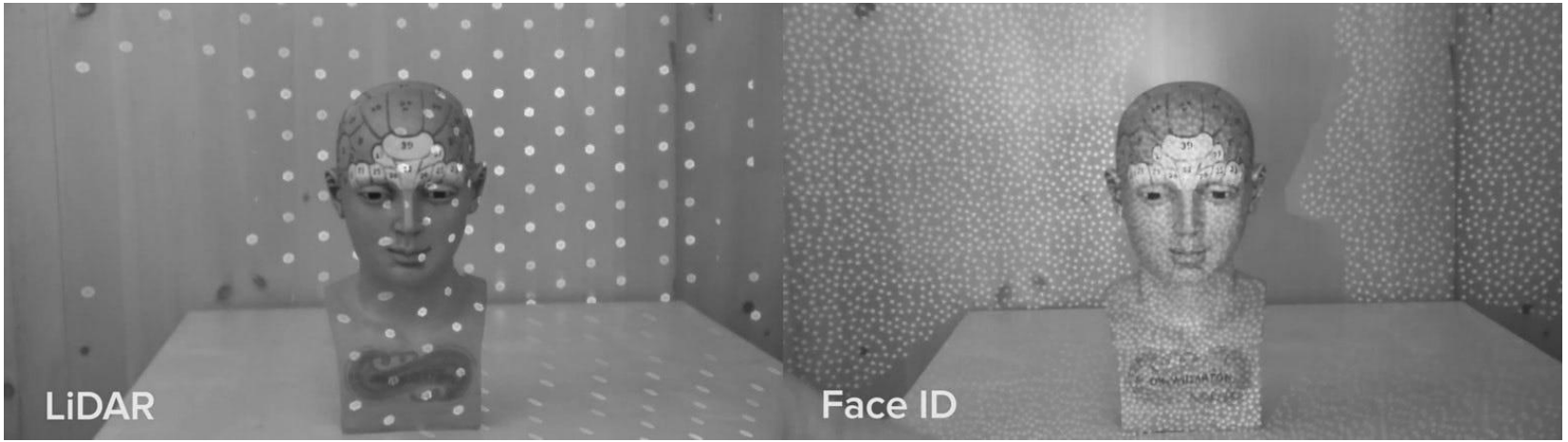






Lidar



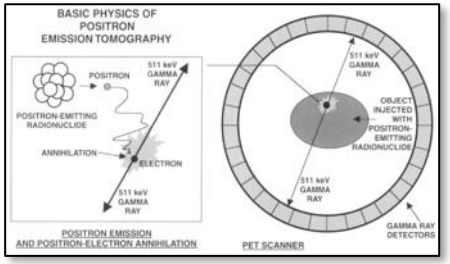


Triggering

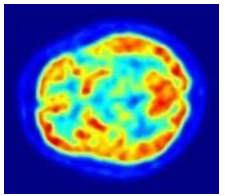
How to reduce your data to be recorded

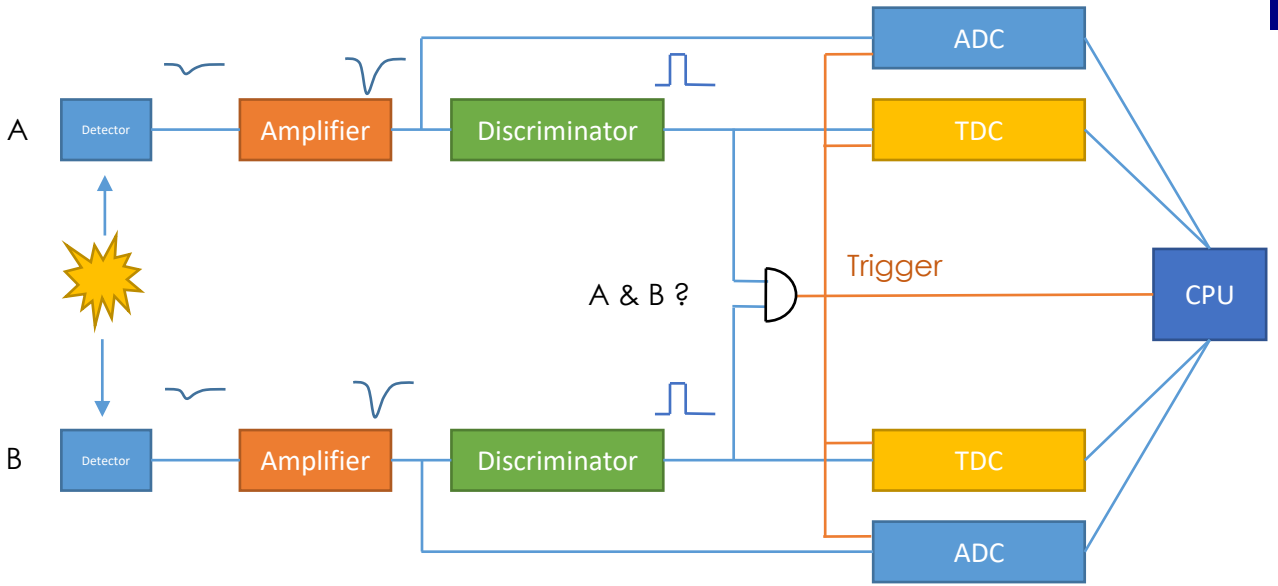
Triggering

- Detectors produce **continuous** electrical signal
- You might only be interested in "**events**"
- **Trigger** your readout electronic only if something "**happens**"
- Can **reduce** your **data rate** enormously



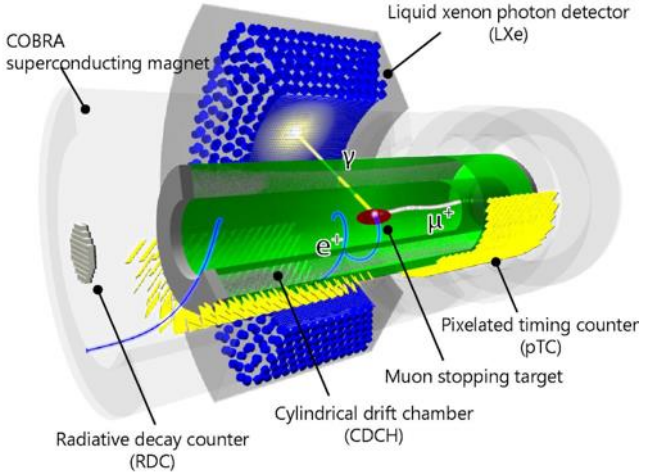
PET image of human brain

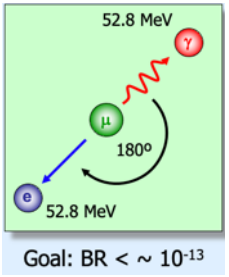


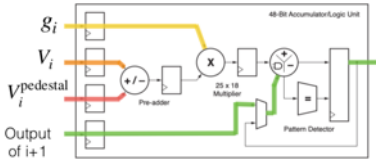


Trigger of MEG Experiment

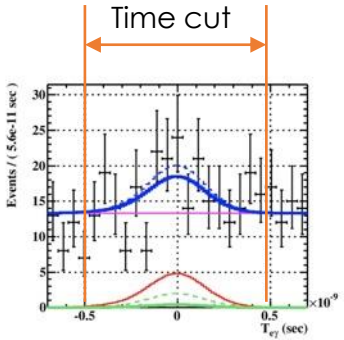
- Event size: 3 MB
- Muon stop rate: **10^8** Hz
- LXe rate: **10^5** Hz
  → 300 GB/s
- Energy sum trigger → **10^3** Hz
- Time trigger → **10^2** Hz
- Direction match → **10** Hz
  → Data rate **30 MB/s**

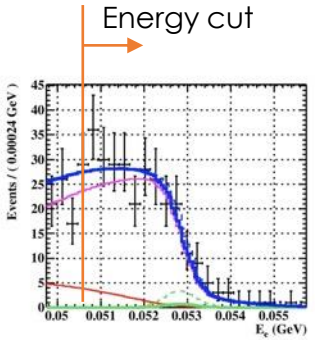






DSP Block in FPGA
to add weighted sum

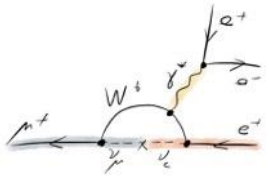


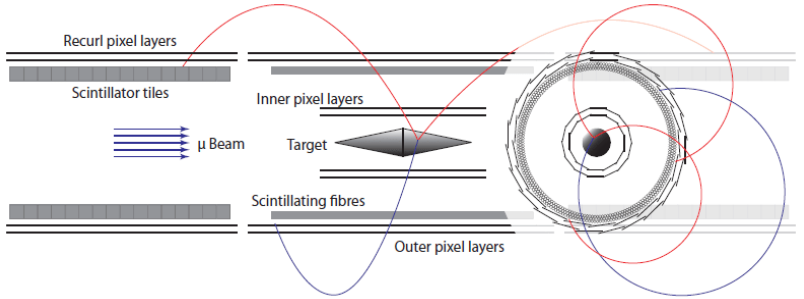


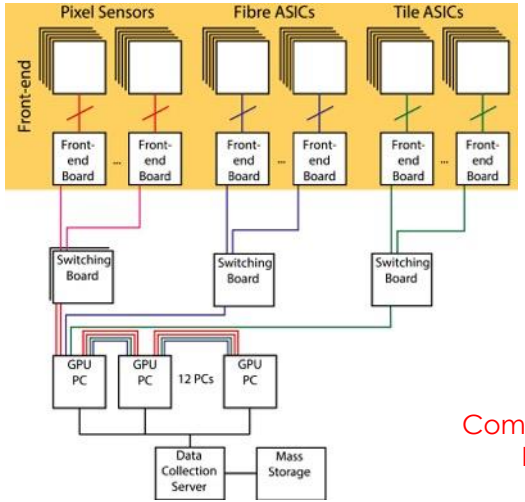
Trigger-less DAQ

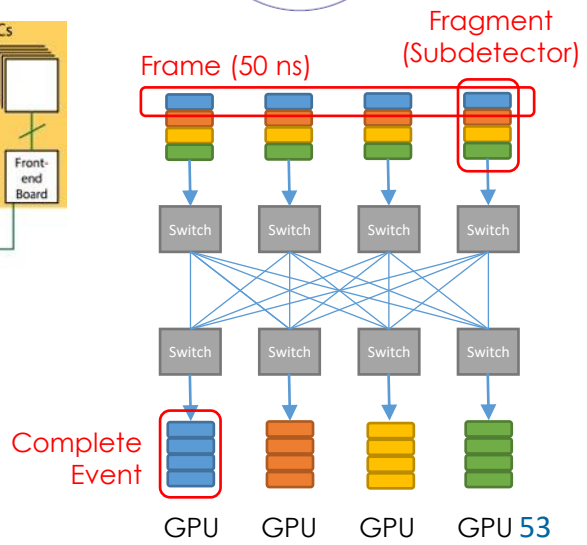
- **Mu3e** experiment at PSI searches for decay $\mu \rightarrow e^+e^-e^+$
- **200 M pixels** are very hard to trigger on
- **Trigger-less** DAQ:
  - **each** particle hit is sent out
  - **~100 GB/s**
    → 100's of high-speed optical links
  - Switching boards for "**event building**"
  - Send full events in 50 ns "**frames**" to 12 GPUs
  - GPUs do full event reconstructing and can **reject 99.9%** of background

    → **100 MB/s** data rate





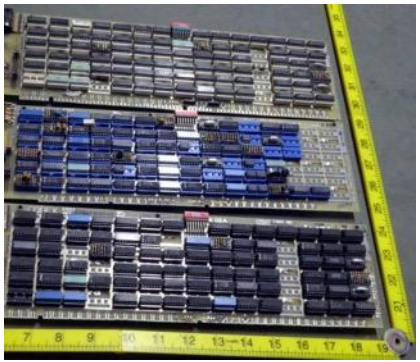


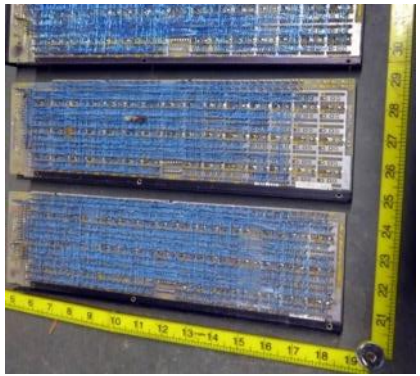


File Programmable Gate Arrays

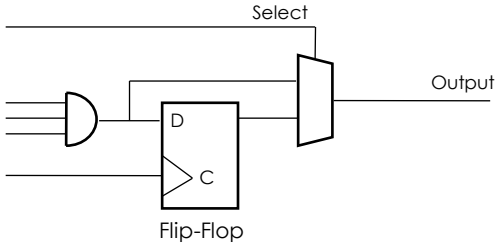
How to process digital data

Field Programmable Gate Array (FPGA)

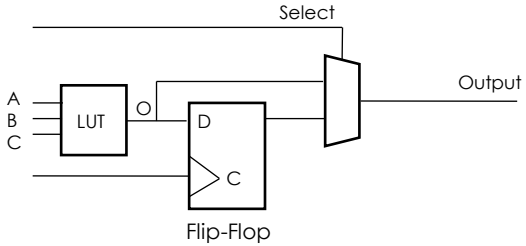




Basic Logic Block



Programmable Logic Block with LUT

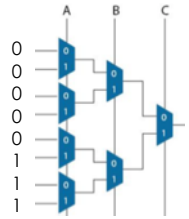


Memory Content

Memory Address

A	B	C	O
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	**1**	**1**	**1**

O = A and B and C

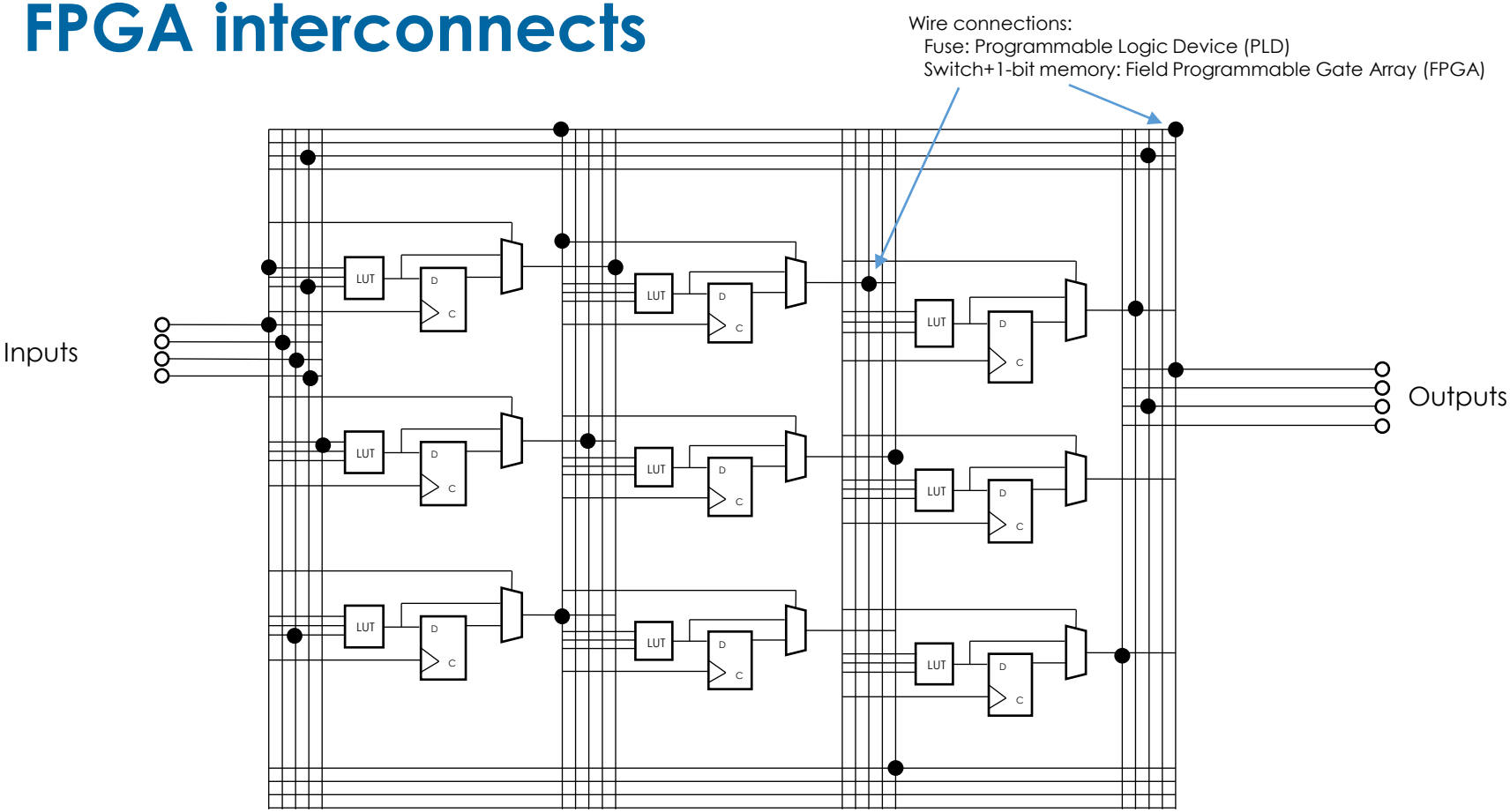


A	B	C	O
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	**1**	**1**
0	**1**	**1**	**1**
1	**1**	**1**	**1**

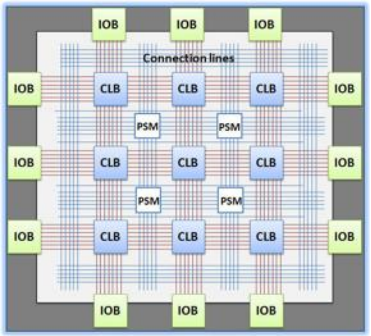
O = (A or B) and C

Wire-wrap technique 1960- (Apollo 11)

FPGA interconnects



Modern FPGA



IOB
Input-Output Block

CLB
Configurable Logic Block

PSM
Programmable Switch Matrix

XILINX. Spartan-6 Family Overview

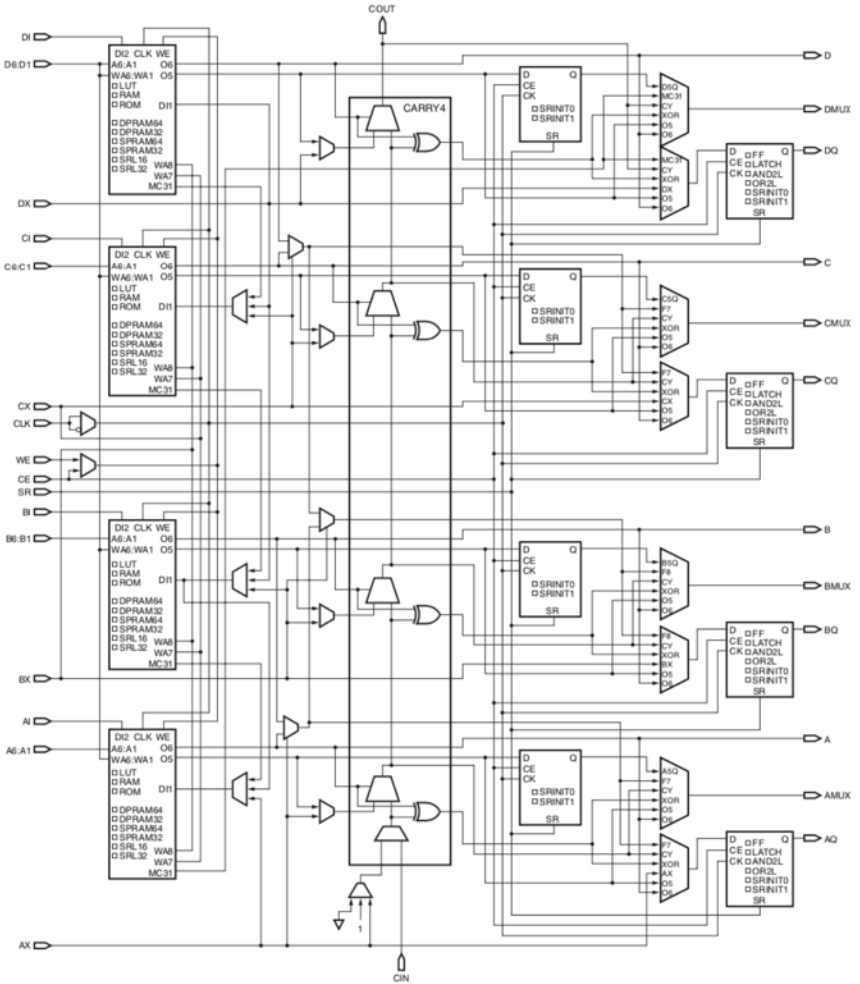
Spartan-6 FPGA Feature Summary

Table 1: **Spartan-6 FPGA Feature Summary by Device**

Device	Logic Cells[1]	Configurable Logic Blocks (CLBs)			DSP48A1 Slices[3]	Block RAM Blocks		CMTs[4]	Memory Controller Blocks	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices[2]	Flip-Flops	Max Distributed RAM (Kb)		18 Kb[4]	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	120
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,750	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	400
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	570
XC6SLX25T	24,051	3,750	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	320
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	490
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	530

Notes:

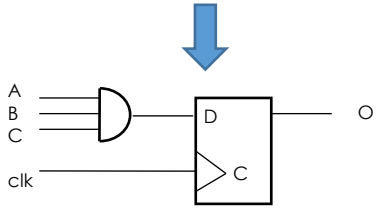
1. Spartan-6 FPGA logic cell ratings reflect the increased logic cell capability offered by the new 6-input LUT architecture.
2. Each Spartan-6 FPGA slice contains four LUTs and eight flip-flops.
3. Each DSP48A1 slice contains an 18 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.
5. Each CMT contains two DCMs and one PLL.



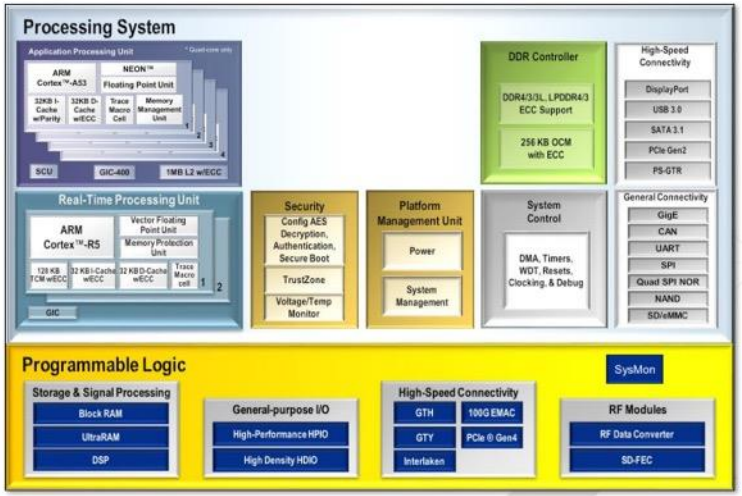
Xilinx Spartan 6 Configurable Logic Block

FPGA features

```
if rising_edge(clk) then
  O <= A & B & C;
end if
```



- Today almost all logic is done with FPGAs in particle physics
  - Programming via Hardware Definition Languages (**VHDL**, Verilog)
  - **Re-programmable even after installation**
  - High cost of FPAG ($10-$1000) not so important
- Modern FPGA (Xilinx, Altera, Lattice, …) have many features:
  - Digital Signal Processing Blocks (**DSP**)
  - Block **RAM**
  - Gigabit **serial links**
  - Connectivity (USB, Ethernet, …)
  - Soft/Hard-core **CPUs**
- Particle physics:
  - **Read** ADC/TDC
  - **Pre-process** data
  - **Send** data via high-speed serial links



Xilinx Zync Ultrascale+

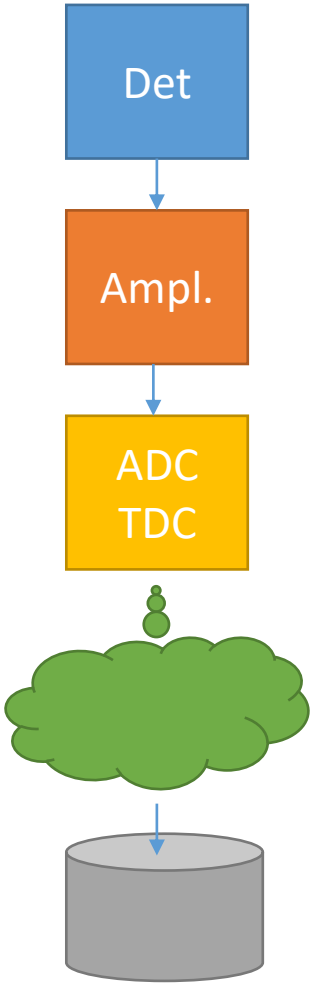
Data Acquisition Systems

Software Part between Digitizers and Storage

Data Acquisition (DAQ)

- We have
  - **Detectors** producing electrical signal
  - Analog **electronics** to condition/shape the signal
  - **Digitizers** for amplitude, charge, time

- We want
  - Define an "**event**" as a collection of data belonging to one physics process (e.g. particle decay)
  - **Read** digitized data from hardware
  - **Combine** data from several detectors
  - **Store** data on permanent medium (disk, tape)



Requirements for a DAQ system

- Experiment **independent**, read all types of hardware
- Typically **10-10,000** channels (will not cover LHC)
- Highly **configurable**
- **"Run concept":** Data collected during defined experiment conditions
- **Robust**
- Should **not rely** on "trendy" hard- and software
  (will it run in 10 years?)
- Efficient and **performant**, typically 100-1000 MB/s
- Include "**slow control**" (temperatures, pressures, …) with plots over time ("History")
- **Good features**: Central configuration, Alarms, Data monitoring,
  Single Event Display, Communication between shifters
- **Remote** (web) controllable

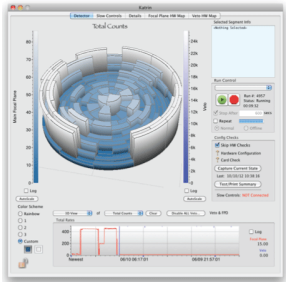
Writing **DAQ** software is orders of magnitude more **complicated** than writing simulation or analysis code

DAQ programming is the "**master discipline**" of coding

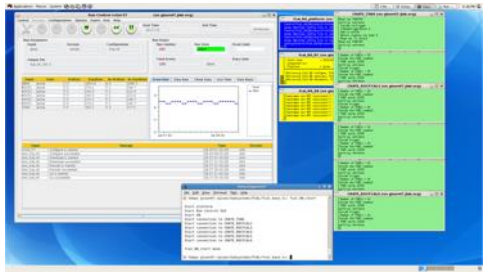
Overview of DAQ systems

- Most physics lab have their own DAQ system and experts
- **Labview**
  - Commercial system from National Instruments Corp.
  - Works well for small setups
  - Drivers for many devices, NI hardware
  - Writing own drivers can be tricky
- **ORCA**
  - Developed at Univ. North Carolina
  - Runs only on MacOS
  - Experiments: KATRIN, MAJORANA, SNO+
- **Artdaq**
  - Developed by Fermilab
  - Based on art offline framework (originally form CMS)
  - Experiments: LARiAT, Darkside-50, Mu2e
- **Midas-UK**: Multi Instance Data Acquisition System (Rutherford – STFC)
- **CODA**
  - Developed at Jefferson Lab and used for experiments there
  - Relies on special readout controller
- And many more…

Labview



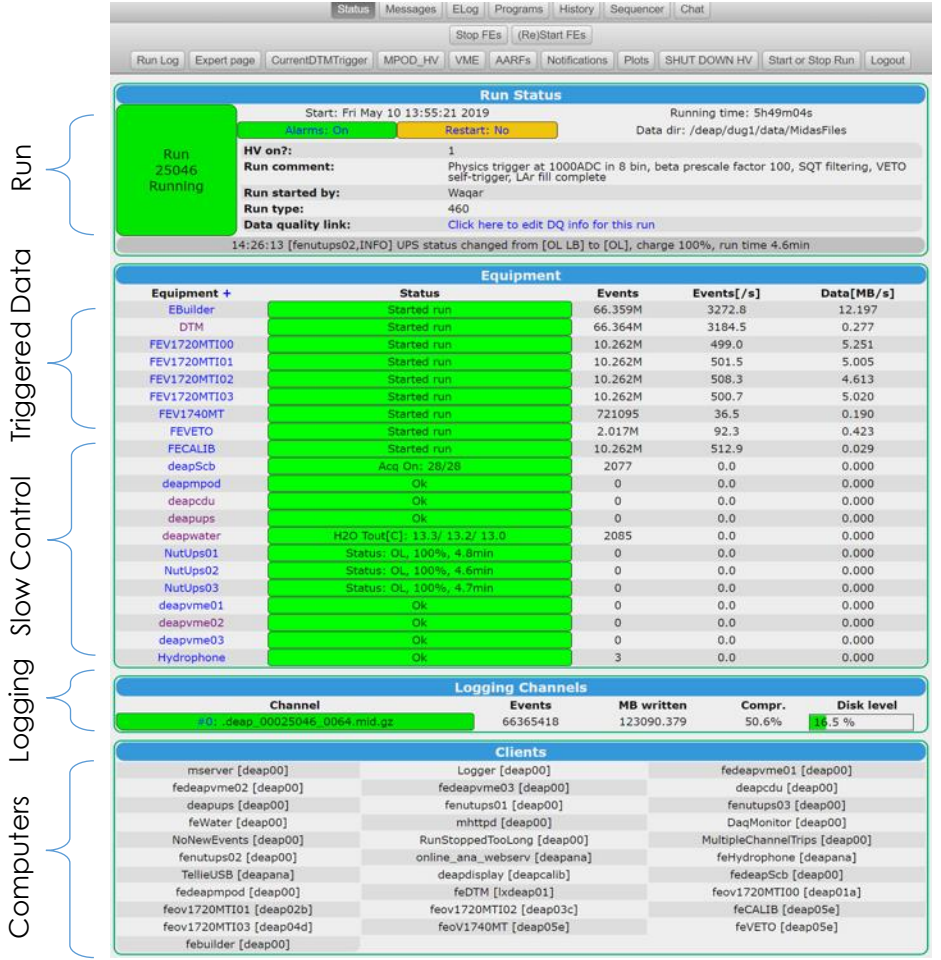
ORCA



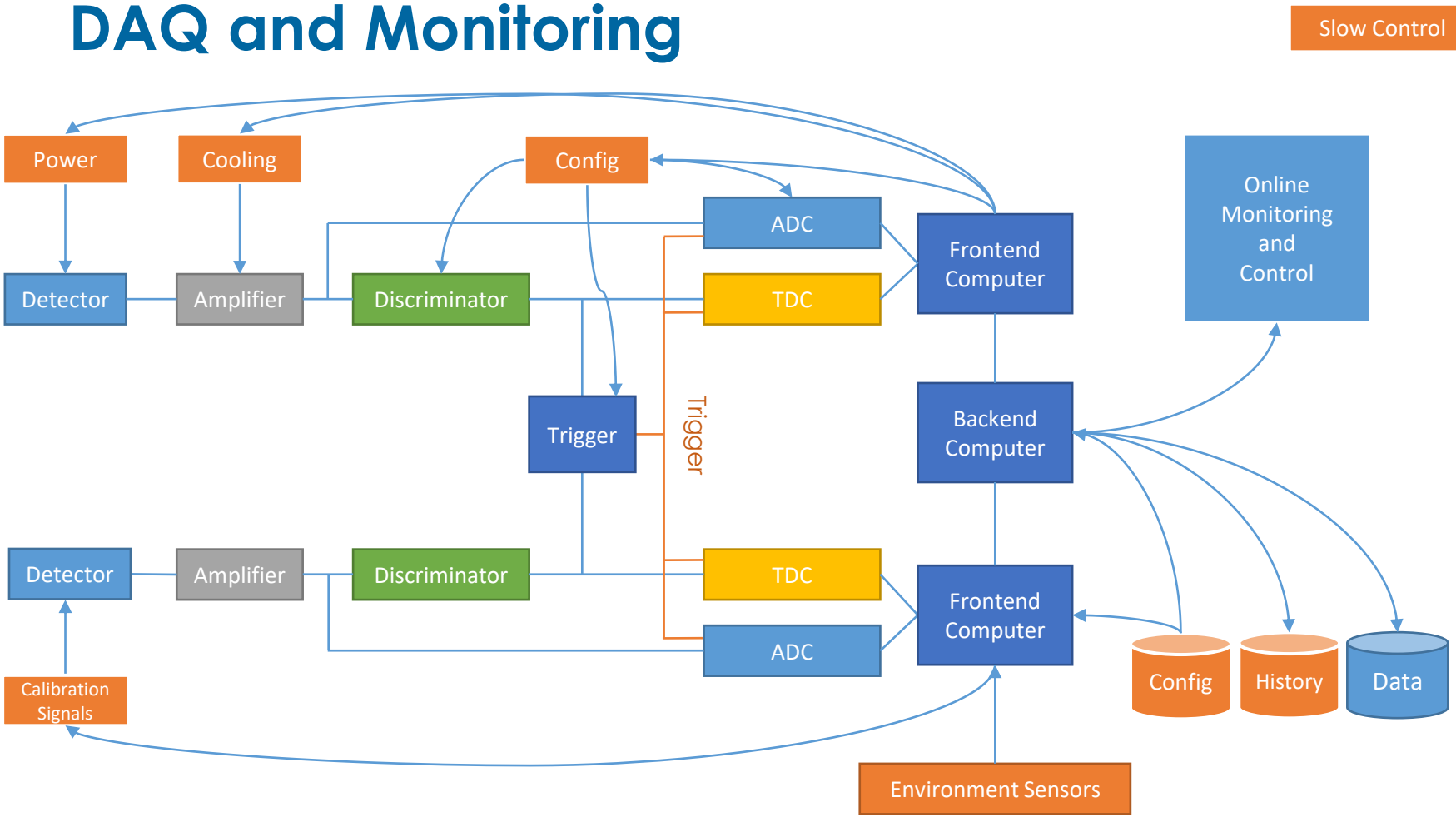
CODA

MIDAS system

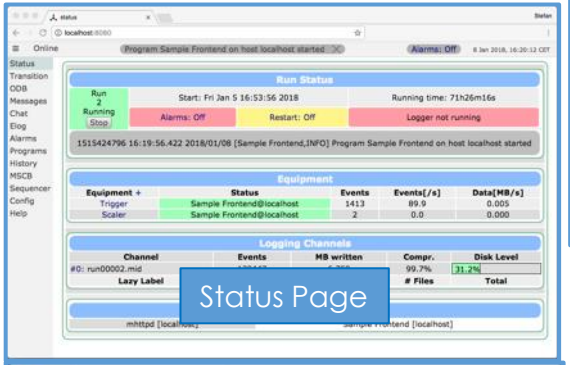
- Development started in **1993** at **PSI**, Switzerland joined by **TRIUMF**, CA in **1996**
- Today used at **PSI** and **TRIUMF** as the standard system, plus **CERN** (Alpha-g), **KEK** (T2K), **Fermilab** (g-2), …
- Maximum Integrated Data Acquisition System
  - Written in C++, JavaScript
  - Integrated **Slow Control**
  - Operating system / hardware **independent**
  - Quick installation
  - Easy customization
  - **Free** (GPL)
  - Good for 1-50 DAQ computers and **~1 GB/s** data rate
- https://midas.triumf.ca

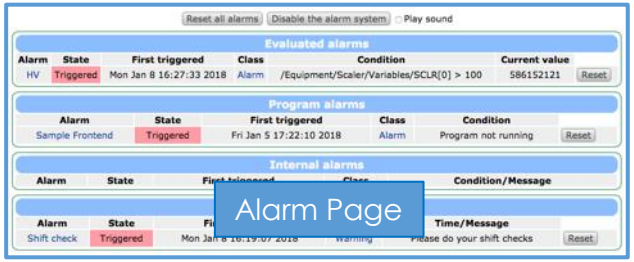


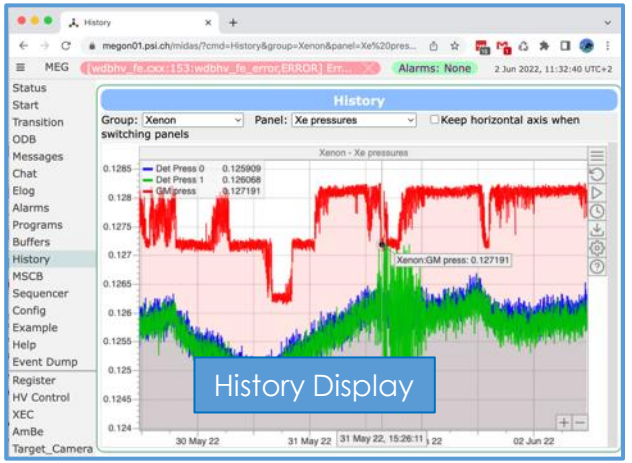
DAQ and Monitoring

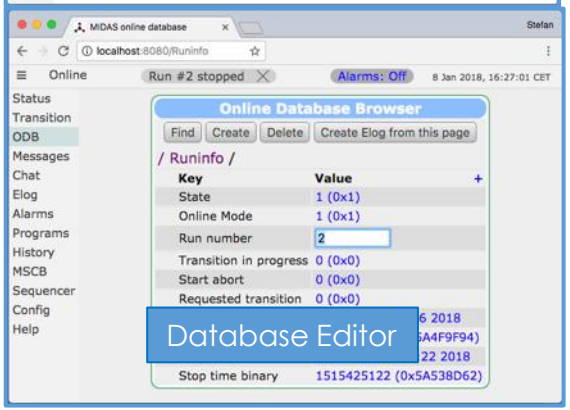


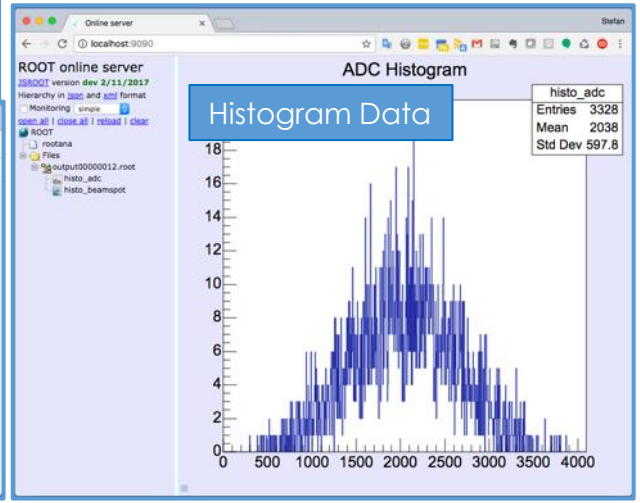
MIDAS in a nutshell





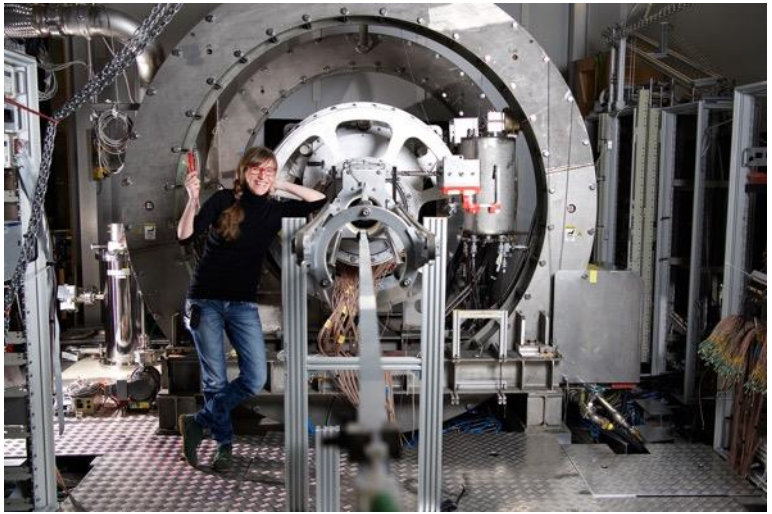


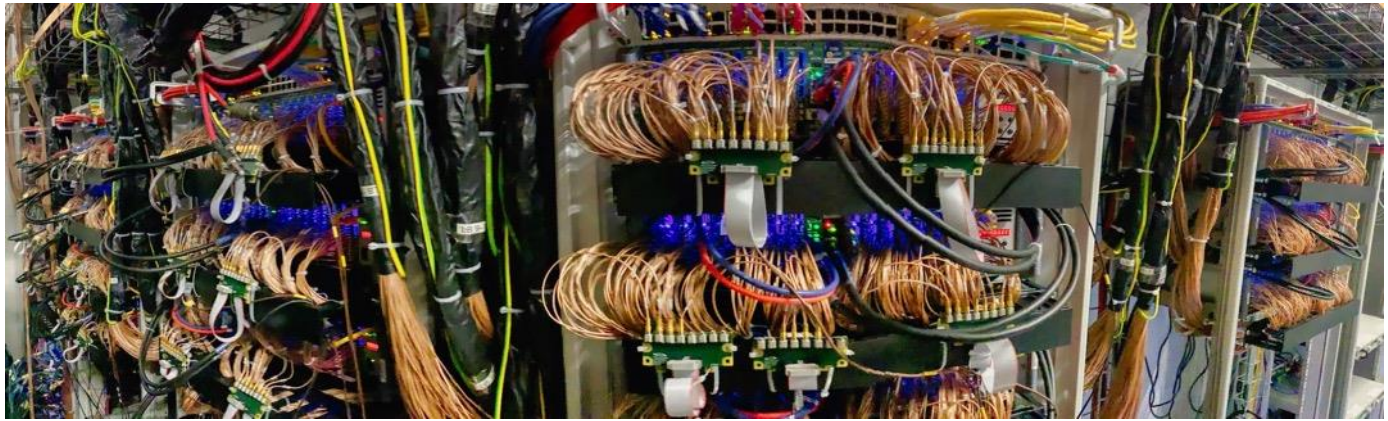


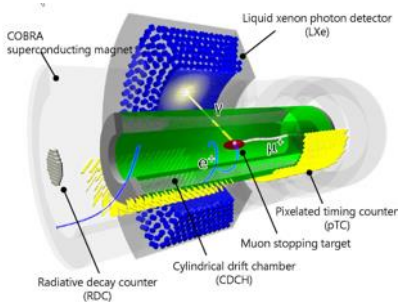


MEG II Experiment, PSI

- Period: **2008 -**
- Channel Count: ~9000
- DAQ Hardware: Custom **WaveDAQ crate** with DRS4 chip (5 GS/s, 12 bit)
- Sophisticated FPGA trigger
- Computer: FPGA Frontend (Xilinx Zynq), **40-core backend PC**
- Rates: 30 events/s, 3 MB events, ~100 MB/s
- Software: MIDAS, ROOT
- Storage: Local SDD (4TB), PSI cluster (1.5 PB)







PAUL SCHERRER INSTITUT

PSI

- Electronics and DAQ are **essential** to make new **discoveries**
- To work on DAQ, a **broad** set of evolving **skills** is necessary
  - Detector Technology
  - Analog and Digital Electronics
  - FPGA programming
  - Serial Links, Networking
  - Multi-thread programming
  - Cluster computing
  - User Interfaces
  - …
- Skills can only be obtained in **hands-on environments**
- **Many thanks to**
  - Pierre-André Amaudruz for some slides
  - IEEE Nuclear and Plasma Sciences Society for sponsoring this lecture