Signal levels and bus standards Present and future

中国科学院高能物理研究所
Institute of High Energy Physics Chinese Academy of Sciences

Zhen-An LIU

IEEE/NPSS SM, Prof. of IHEP/Chinese Academy of Sciences, Beijing, China (Liuza@ihep.ac.cn)

IEEE NPSS School of Application of Radiation Instrumentation

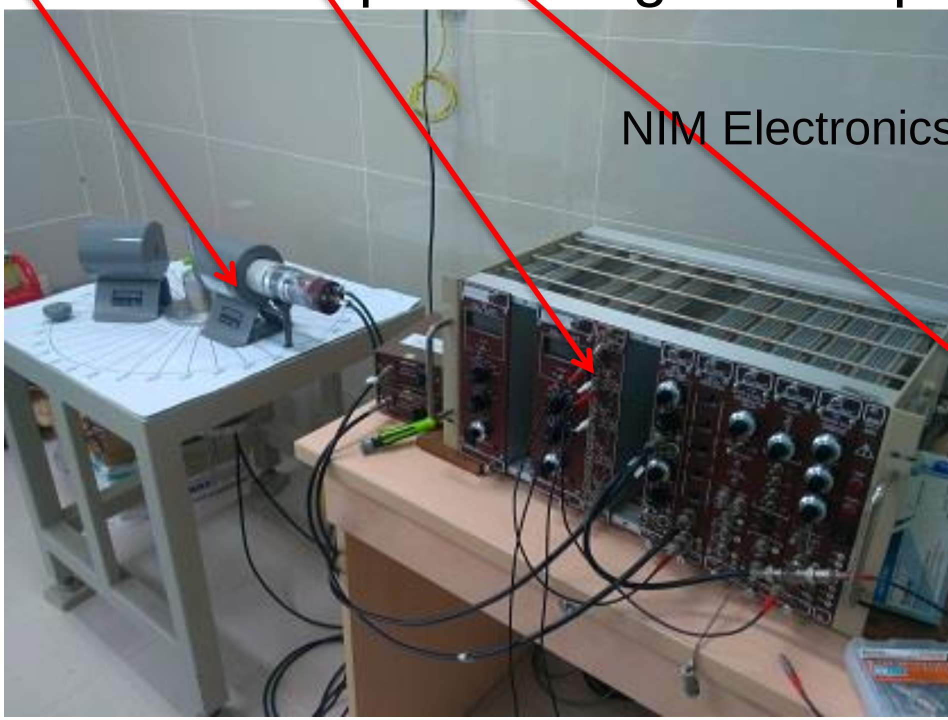
14-26 Nov. 2022, Dakar, Senegal

Outline

- Overview in a physics experiment
  - Why standardization is a must
- Signal standard in instrumentation
  - Levels
  - Level shifting
- BUS Standard in instrumentation
  - Old NIM,CAMAC,VME
  - Present and future standard
    - VPX
    - xTCA for Physics: AMC, ATCA, MTCA
  - Some examples
- Summary

Overview in a physics experiment

- Physics Experiment/Instrumentation
  - Detector: for signal detection
  - Electronics: signal processing
  - Processor: data processing and display

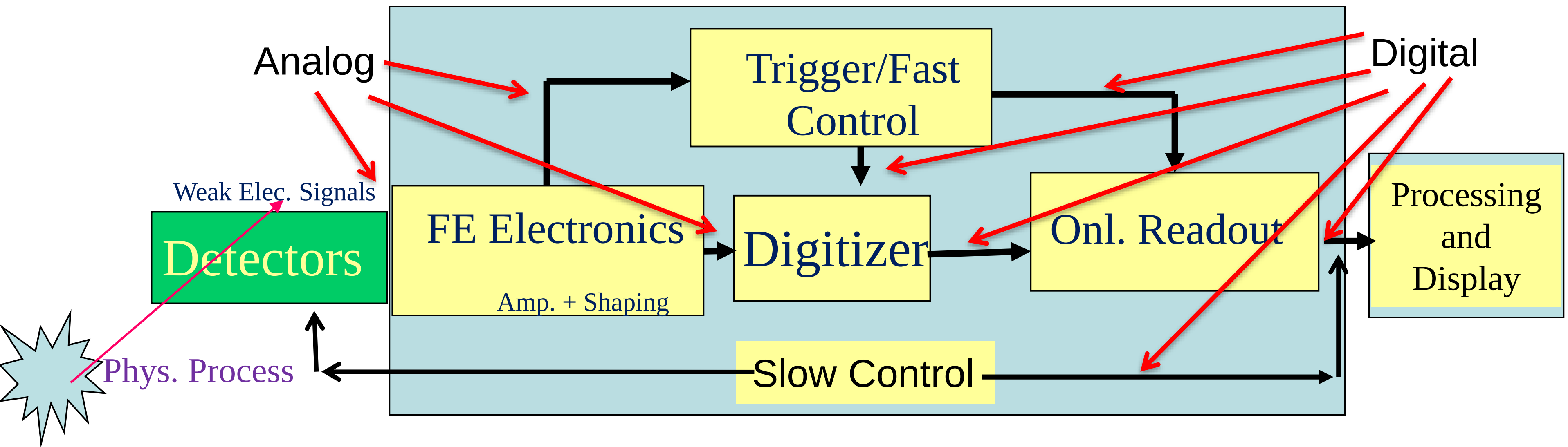


MCA

Compton Scattering Setup in NTLab VNU-HCMUS, School on RT System 2016

Signal Processing and Control

- Analog/Digital signal processing

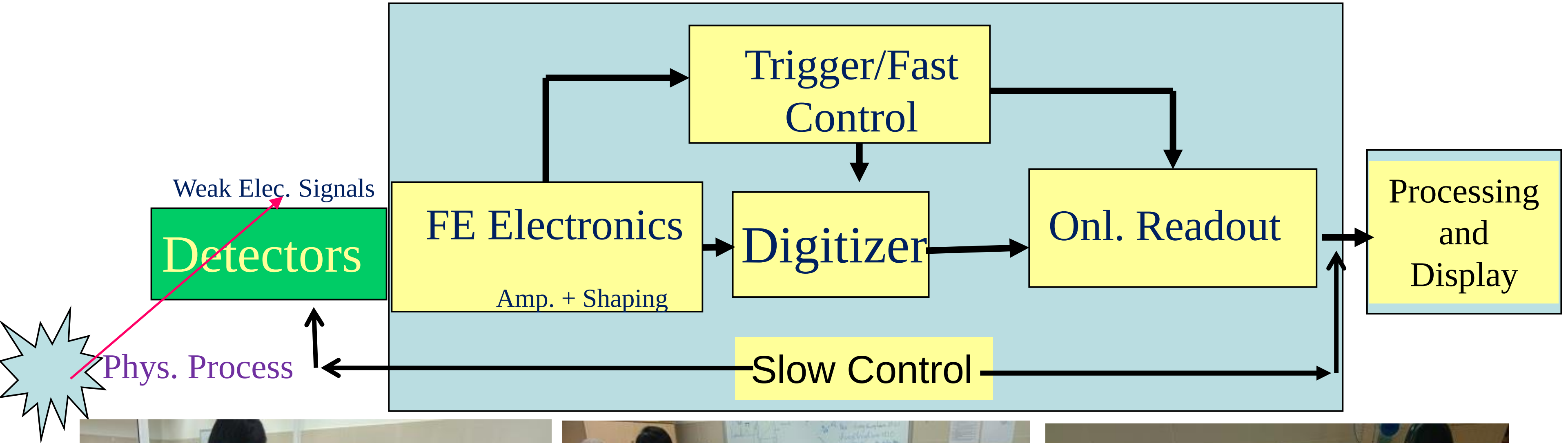


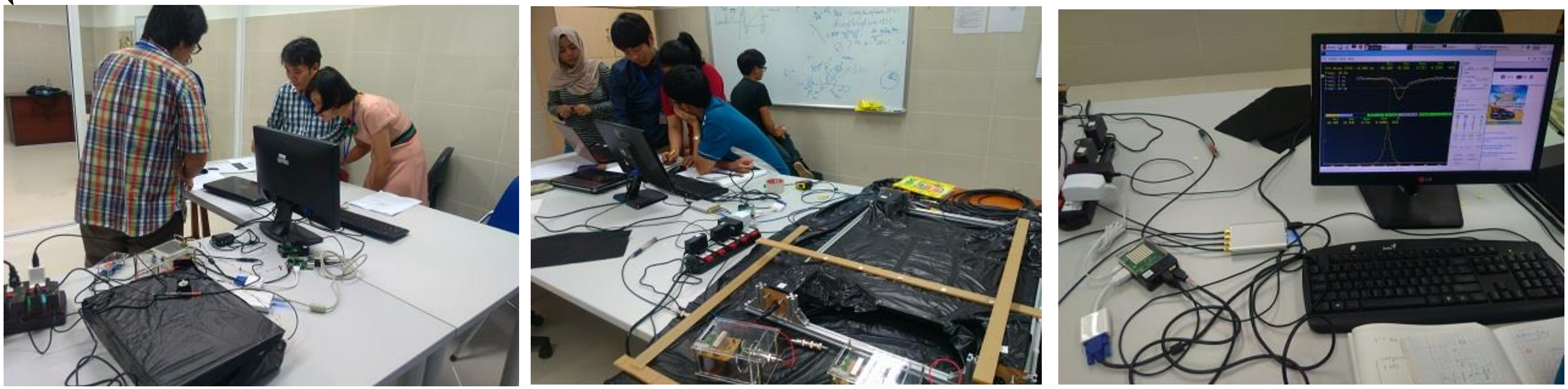
  - Pre-Amplifier: amplify weak signal
  - Main Amplifier: amplify small signal
  - Digitizer: convert analog to digital
  - Readout: collect data
  - Processor: data analysis and display

Digital signal standardization

Trend direction 1: Instrumentations minimization: Lower signal level and Faster data link

- Full system into small box



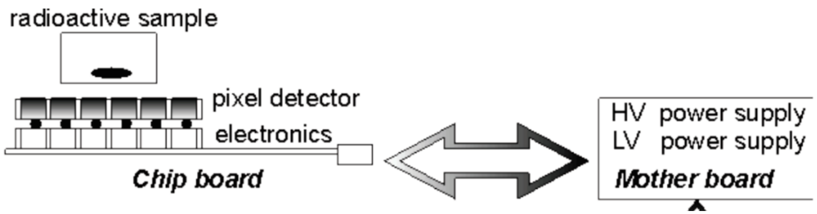


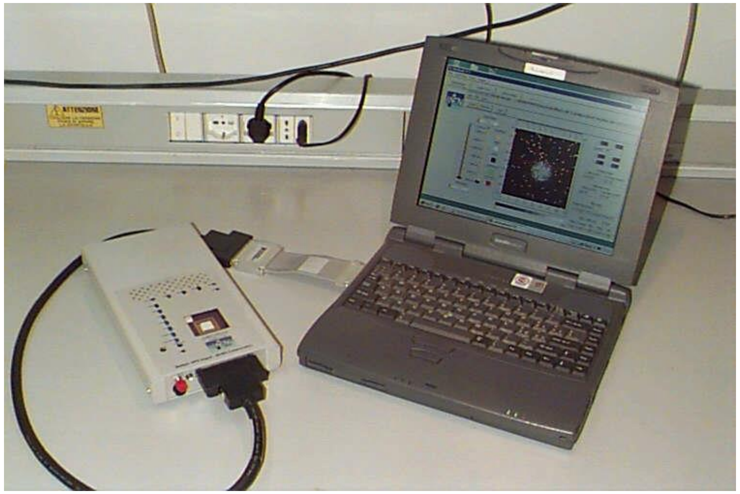
PMT(left),TOF(middle, right) exercise setup for RT School 2016

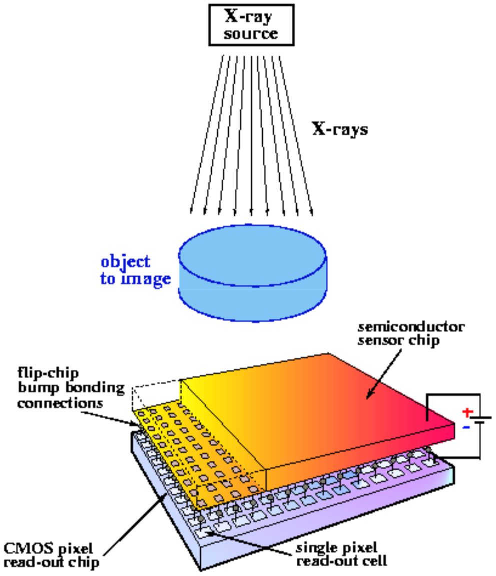
Trend direction 1: Compact Instrumentations: Lower signal level and Faster data link

- Or even handy meters
  - ASICs: Application Specific Integrate Circuits
  - FPGA:Field Programmable Gate Array
  - System on Chip
  - Experiment on Chip

Medipix1 block







Question

- Can you connect your Mobile Phone to your notebook or desktop computer?

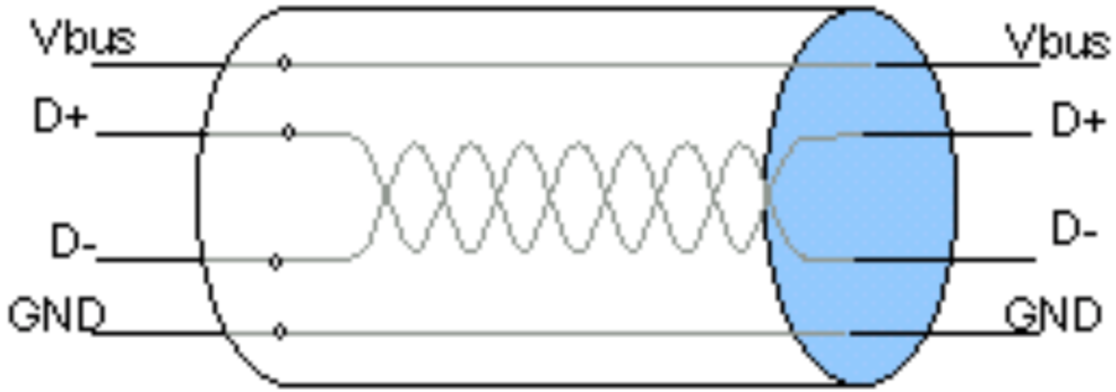
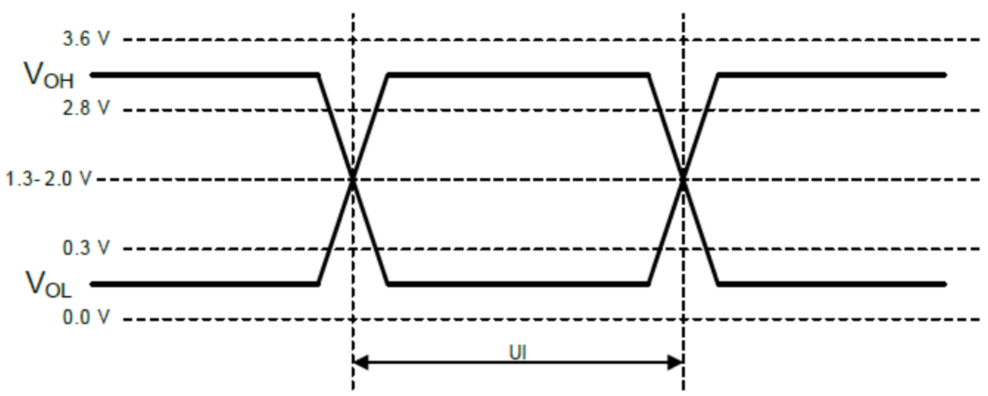


Figure 4.1. USB Full-speed/low-speed Signal Levels



The Answer is YES! As we have USB cable to connect them with compatible Levels and form factor.
Thanks to standards!

USB standard

- Why you can borrow a USB line to connect your Mobile Phone to your notebook?

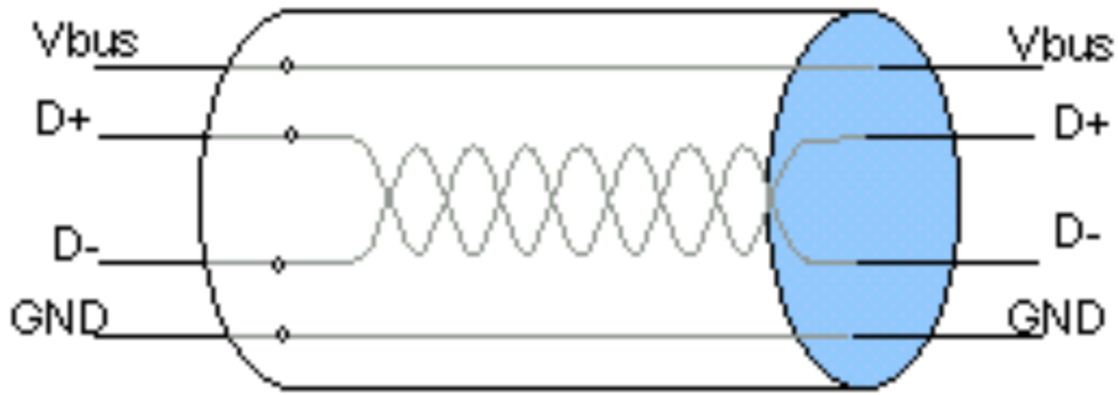
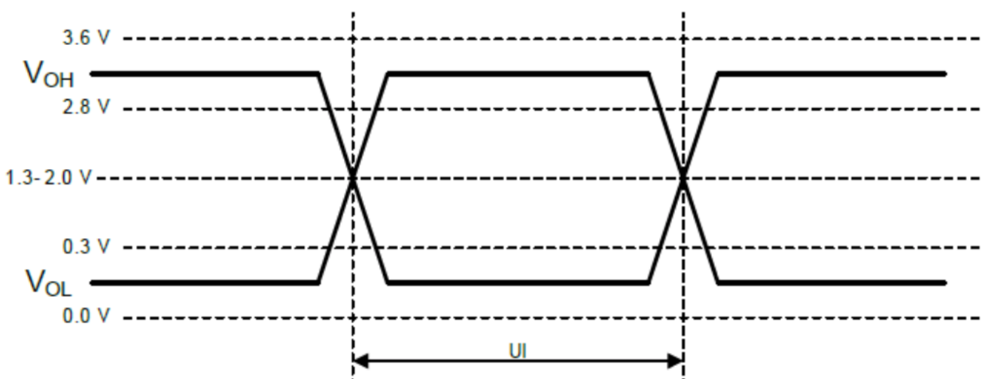


Figure 4.1. USB Full-speed/low-speed Sig

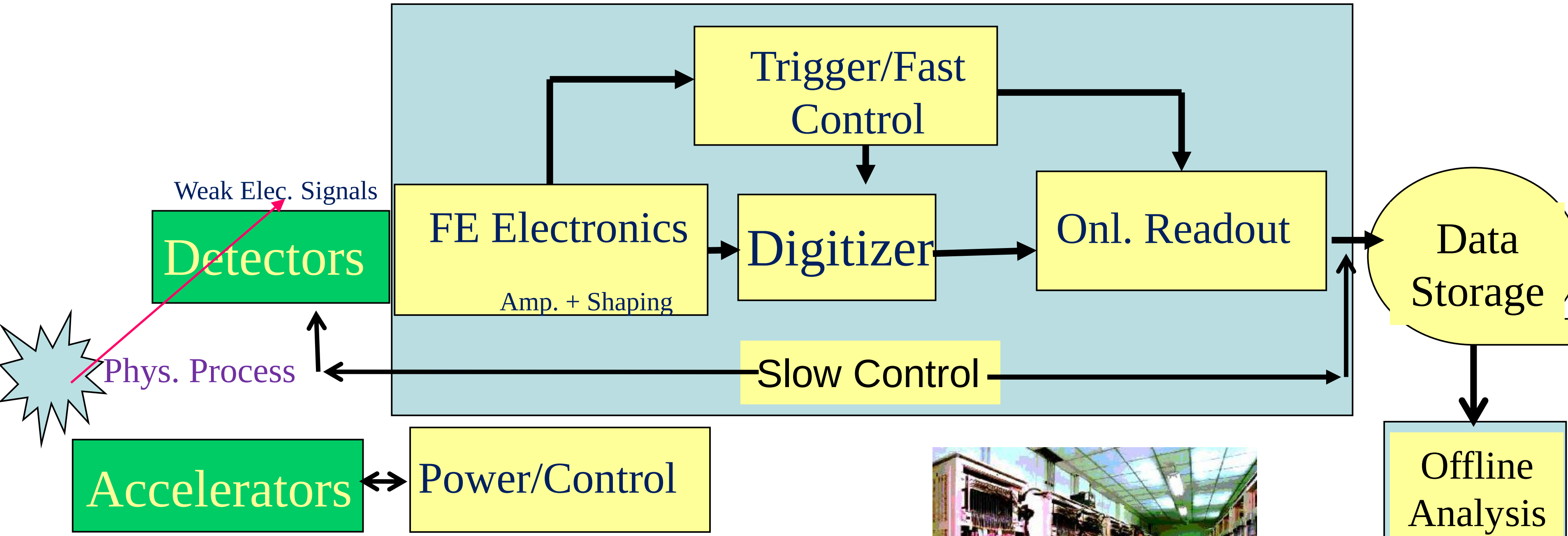


Do you still see a problem with USB?

- USB
- Mini-USB
- Micro-USB
- Apple lightning
- Type C-USB

Trend direction 2: Experiment needs Instrumentations for Signal Processing and Control in Larger scale

- Huge amount of different instruments




Electronics


Accelerators


Detectors

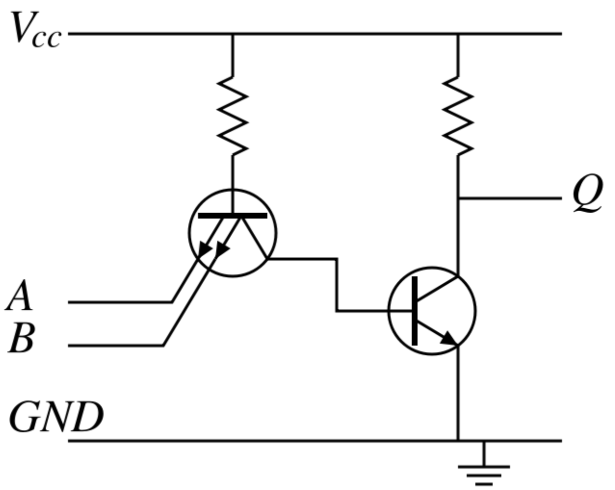
- Control and Data Readout
  - Standardized Signal levels
  - Standardized Crates
  - Standardized Modules

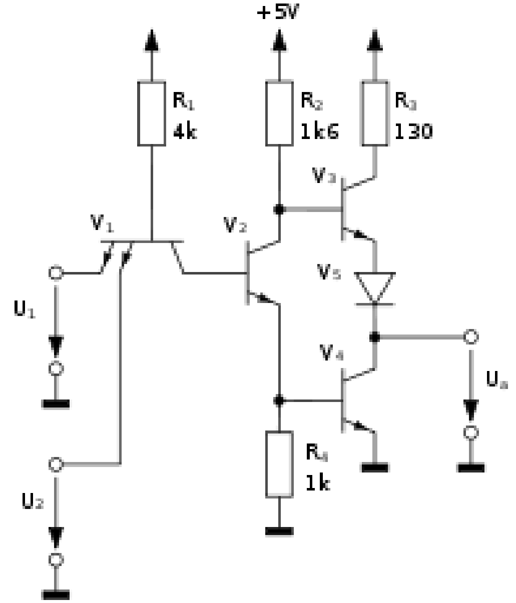
Questions

- In digital world, what is the logic 1? And Logic 0?
- What are the names representing different digital levels? Their voltages of level 1? And level 0?
- You know USB line already, what else?
  – Can-BUS, one-wire BUS
  – Boundary Scan/JTAG
  – ……

TTL Logic

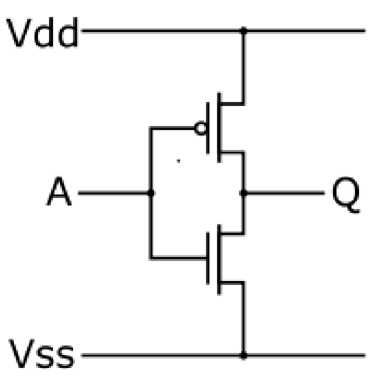
- TTL: Transistor-Transistor Logic
  - invented in 1961 by James L. Buie of TRW Company
  - Logic 1(high): >2V
  - Logic 0(low): < 0.8V

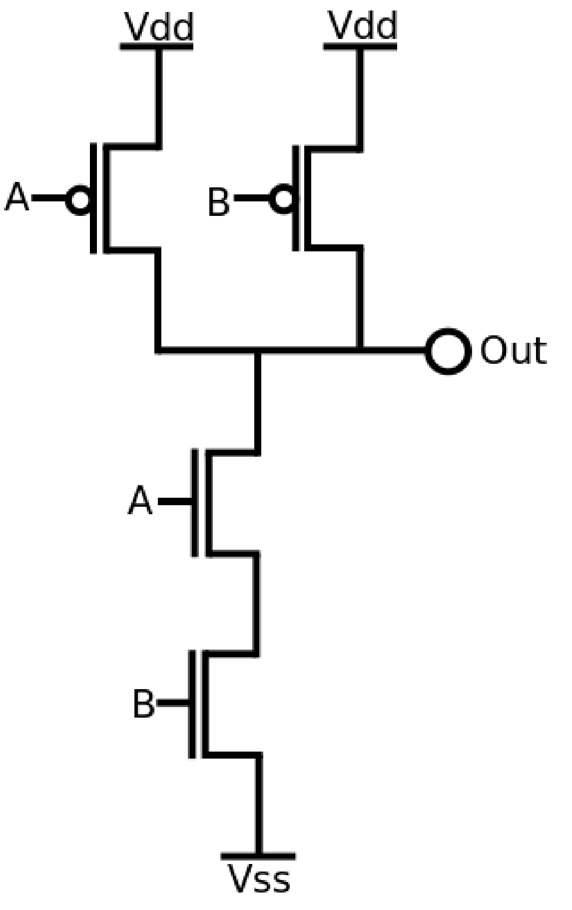




CMOS Logic

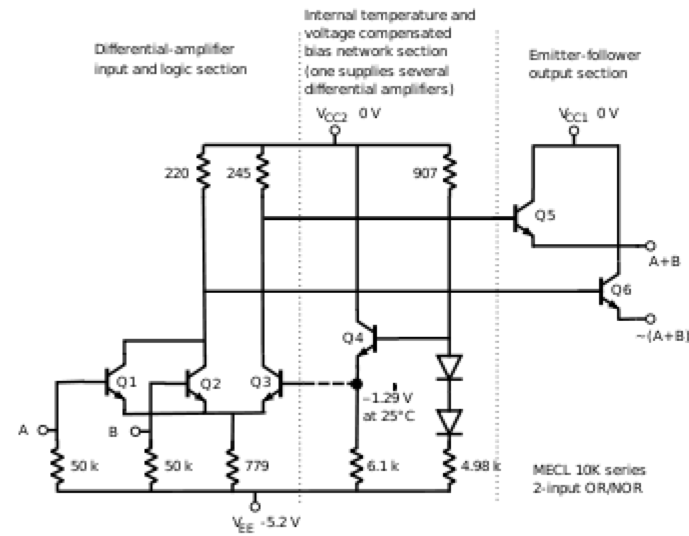
- **CMOS** (**Complementary metal–oxide–semiconductor**) is a technology for constructing integrated circuits.
- Frank Wanlass patented CMOS in 1963
- high noise immunity and low static power consumption
- V_{DD} = supply voltage
- VSS=Ground



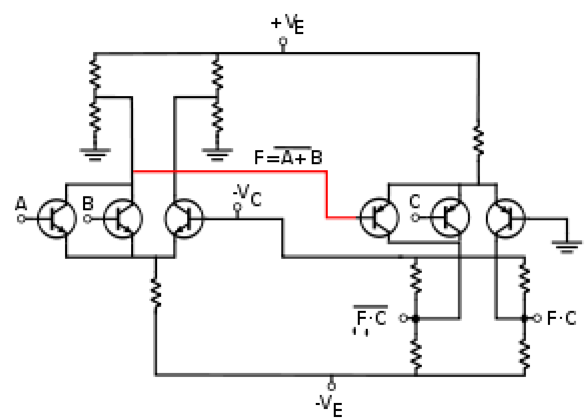


ECL/PECL/LVPECL Logic

- **ECL (emitter-coupled logic)** is a high-speed integrated circuit bipolar transistor logic family
- ECL was invented in August 1956 at IBM by Hannon S. Yourke
- PECL: Positive powered.
- LVPECL: 3.3V PECL



Type	V_{ee}	V_{low}	V_{high}	V_{cc}	V_{cm}
PECL	GND	3.4 V	4.2 V	5.0 V	
LVPECL	GND	1.6 V	2.4 V	3.3 V	2.0 V



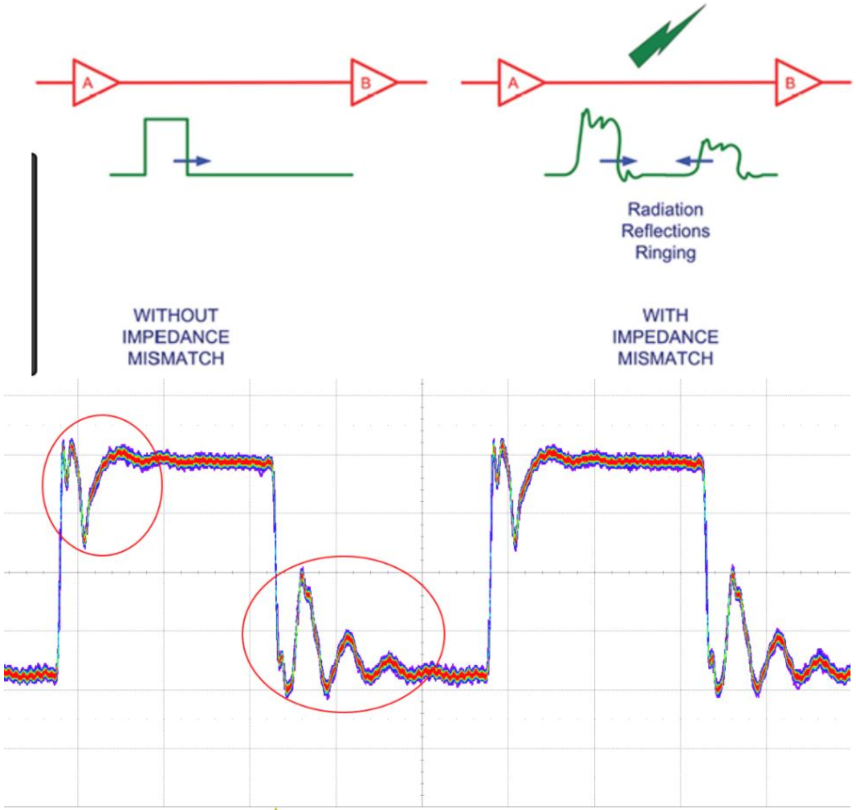
Examples of binary logic levels

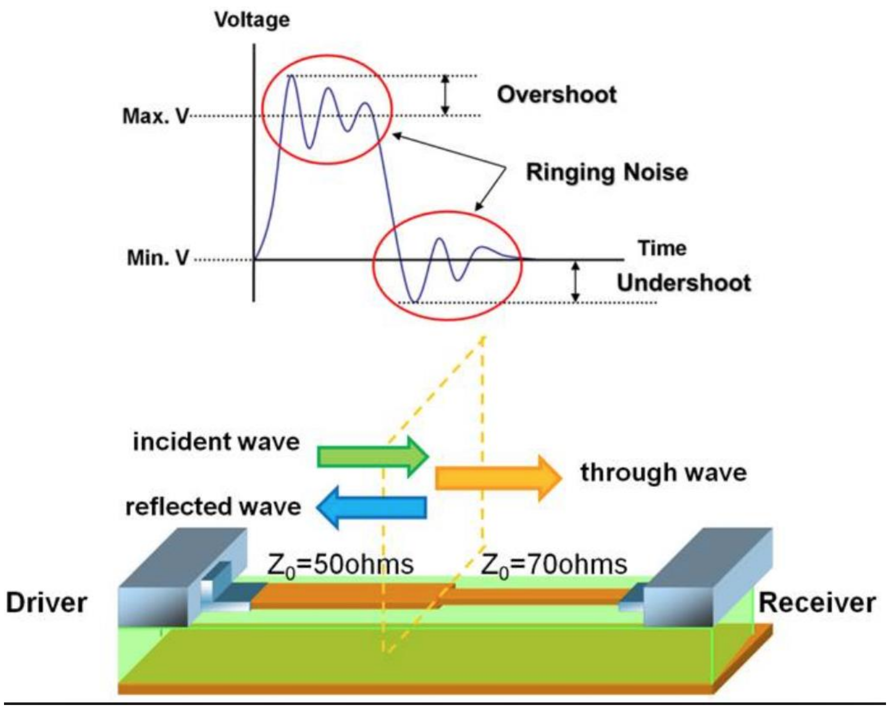
Technology	L voltage	H voltage	Notes
CMOS	0 V to $V_{DD}/2$-a	$V_{DD}/2$+a to V_{DD}	V_{DD} = supply voltage, a=1,2,3.5V for VDD=5,10,15V
TTL	0 V to 0.8 V	2 V to V_{CC}	V_{CC} is 4.75 V to 5.25 V
ECL	-1.175 V to V_{EE}	0.75 V to 0 V	V_{EE} is about -5.2 V. V_{CC}=Ground
NIM	-0.8V	0V	V_{EE} is about -5.2 V. V_{CC}=Ground

NIM logic: levels are defined by current ranges on 50 ohm input/out impedances, correspond to voltages of 0 V and -0.8 V for logic 0 and 1 respectively

Signal Integration

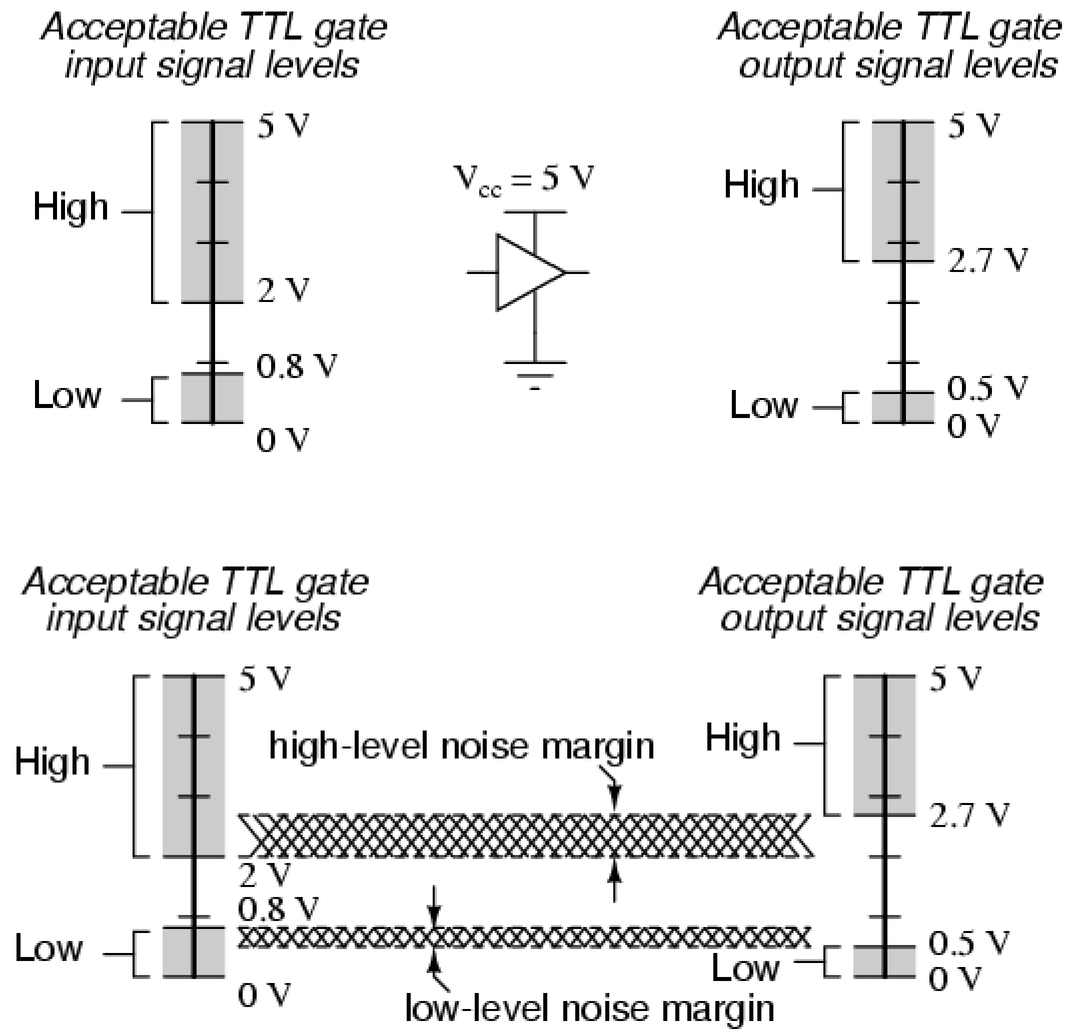
- Termination
- Twix Pair lines
- Shielding





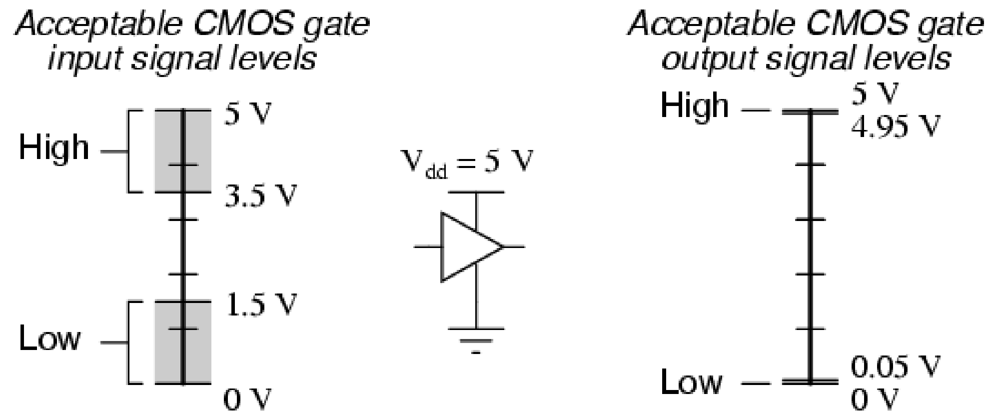
What standard means

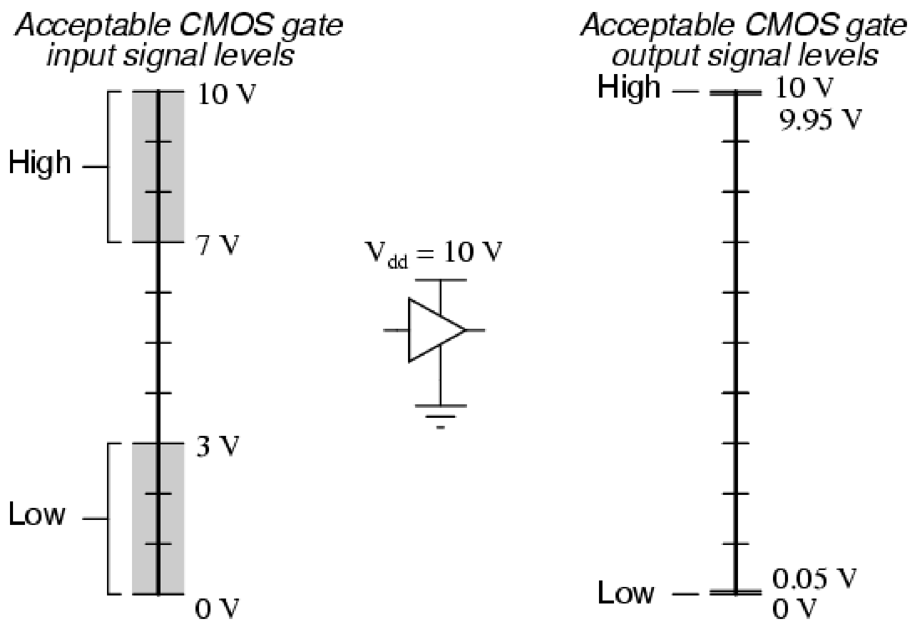
- Forbidden Range
- Range different for input and output for noise tolerance
- Limited noise margin

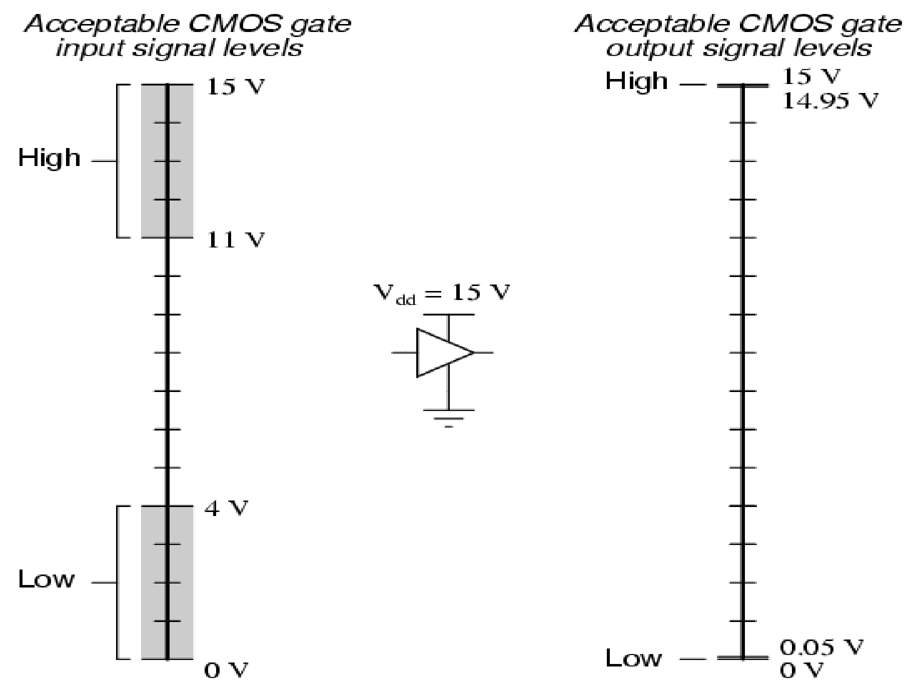


What standard means(2)

- Good noise margin
- High power consumption

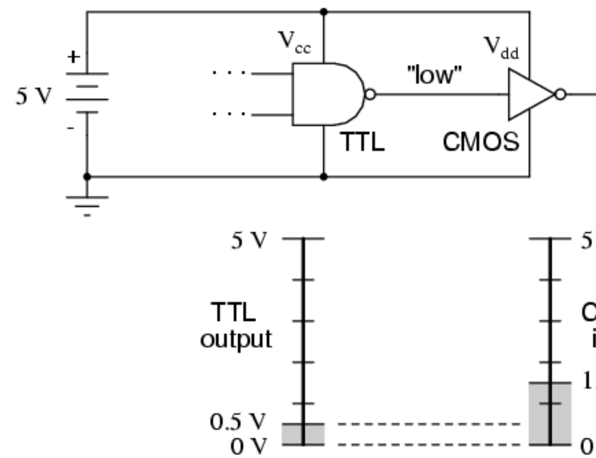




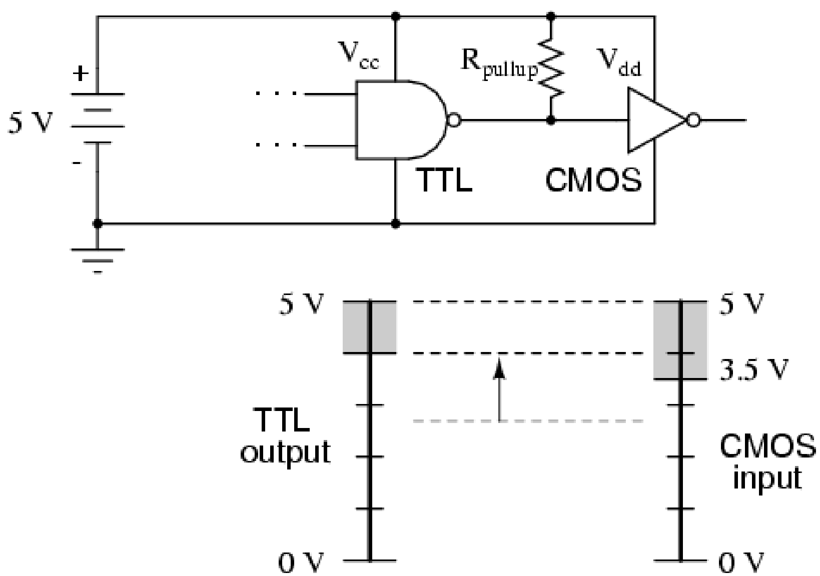


What standard means(3)

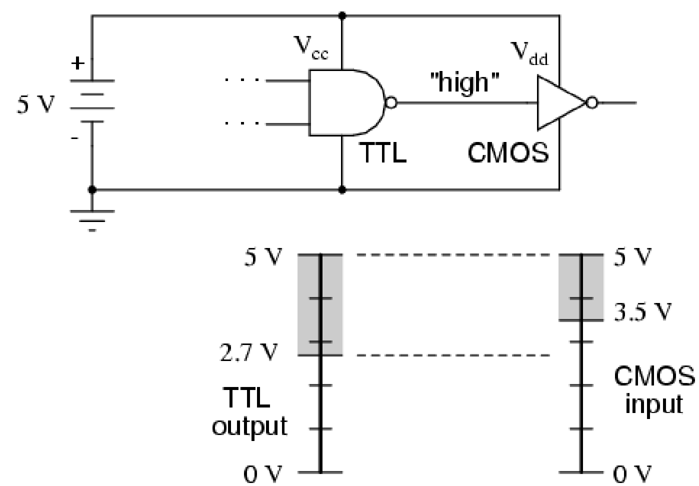
- No direct connection btw devices of different standards
- Level shifting necessary
  - By circuit between, or
  - By commercial device



TTL output falls within acceptable limits for CMOS input



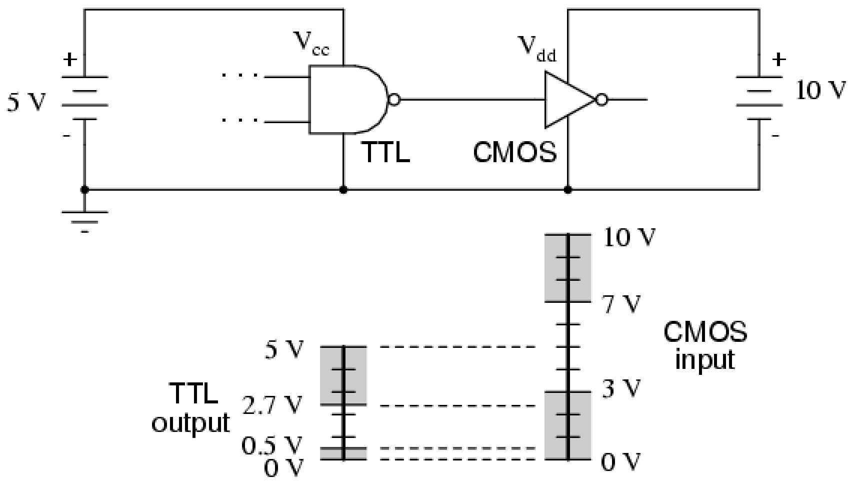
TTL "high" output voltage assisted by R_{pullup}



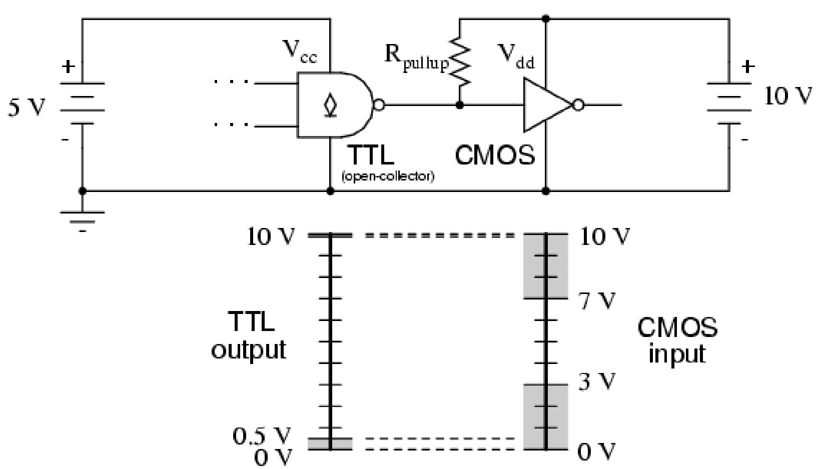
TTL output falls outside of acceptable limits for CMOS input

What standard means(4)

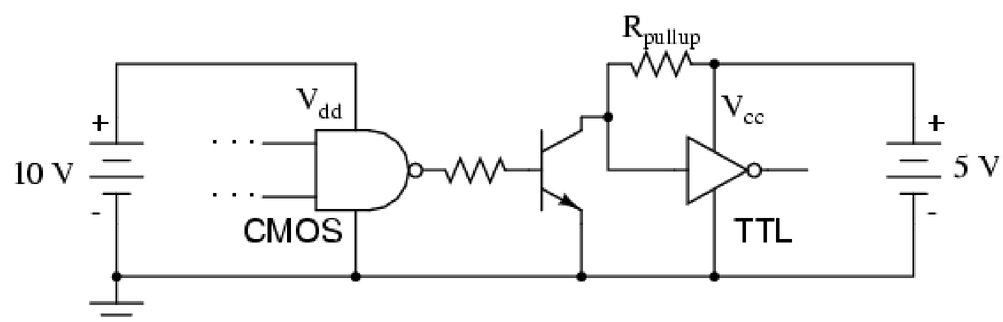
- In 10V CMOS case
- No direct inter-usage
- Level shifting necessary



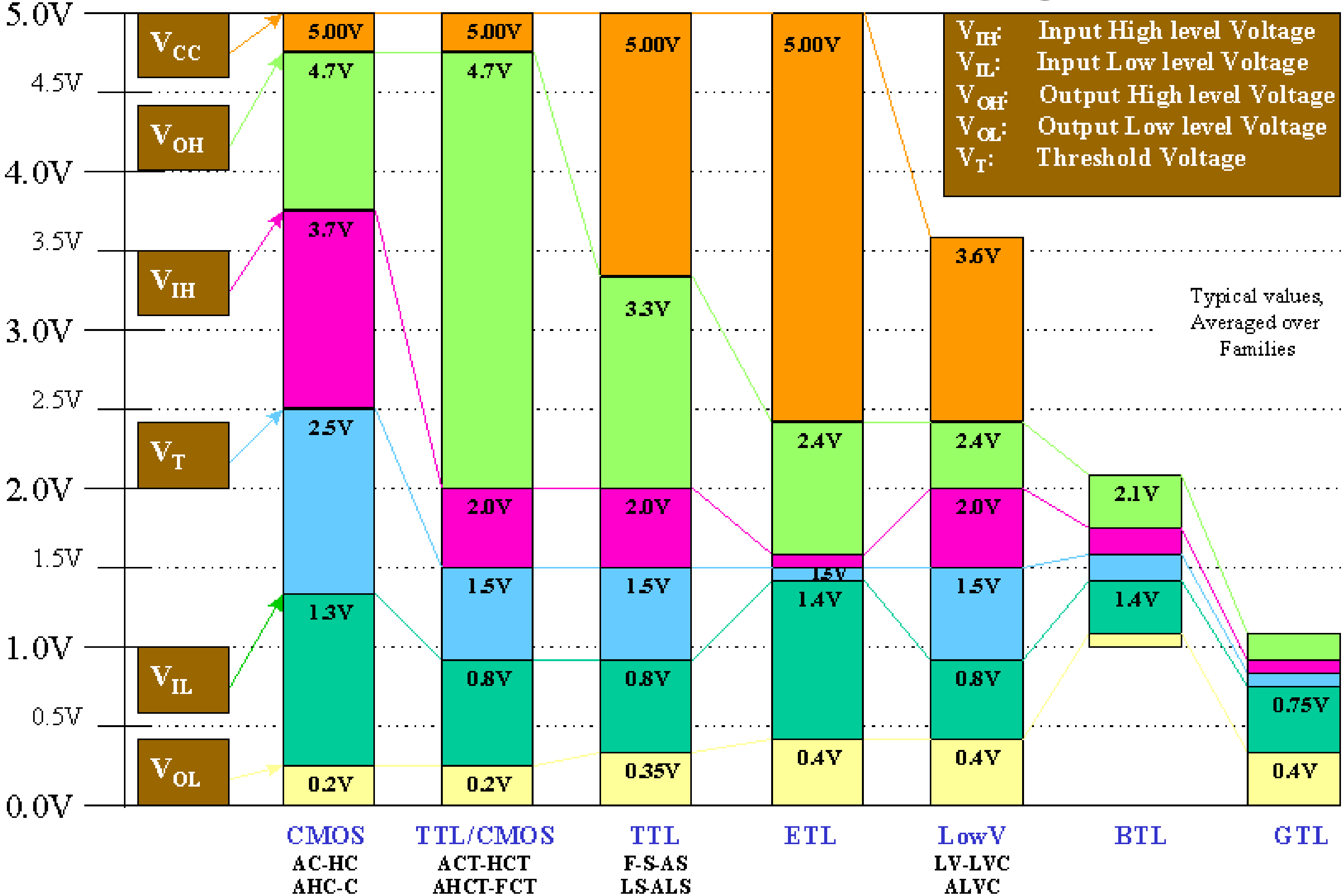
The TTL "high" signal will definitely not fall within the CMOS gate's acceptable limits



Now, both "low" and "high" TTL signals are acceptable to the CMOS gate input

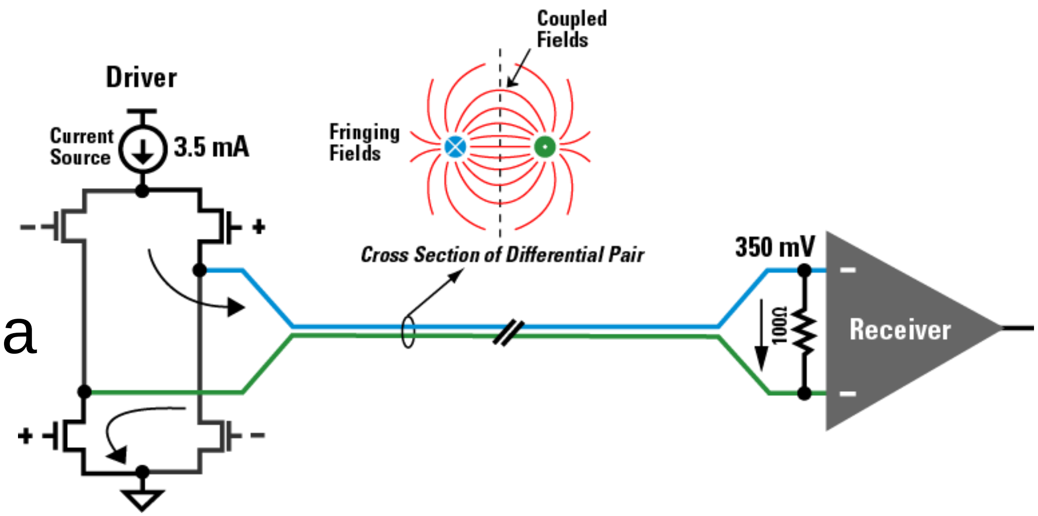


Some of the level ranges

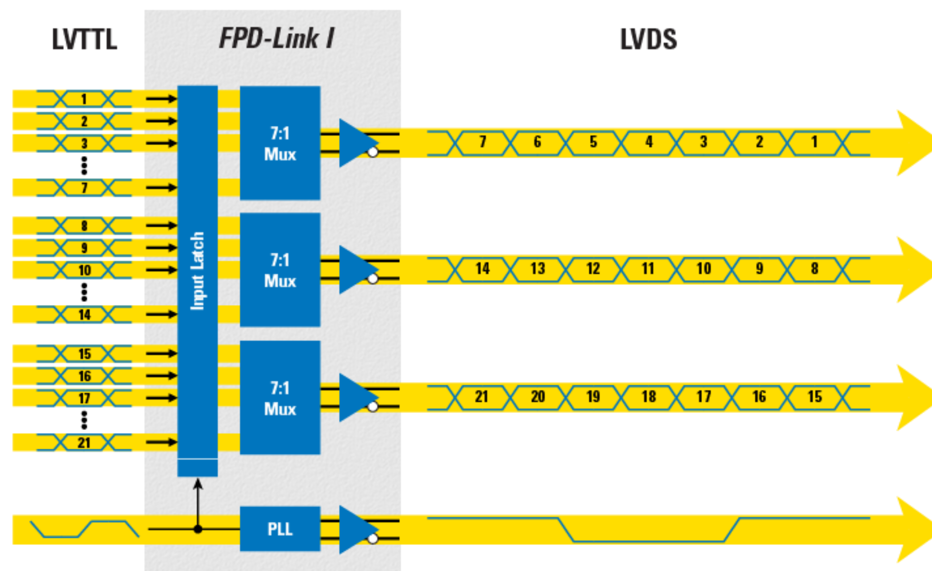


LVDS

- **LVDS(Low-voltage differential signaling)/ TIA/EIA-644**, a technical standard that specifies electrical characteristics of a differential, serial communication protocol
- low power, very high speeds with inexpensive twisted-pair copper cables
- was introduced in 1994
- Point to point

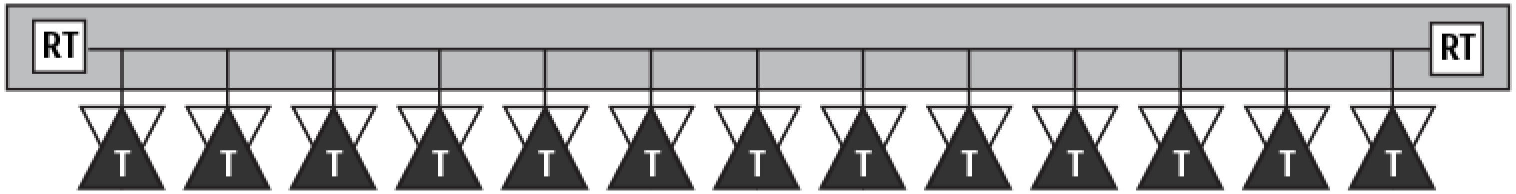


V_{ee}	V_{OL}	V_{OH}	V_{cc}	V_{CMO}
GND	1.0 V	1.4 V	2.5–3.3 V	1.2 V



Multipoint LVDS/MLVDS/BLVDS

- **Bus LVDS** and **LVDM** (by TI) are de facto multipoint LVDS standards
- Multipoint LVDS (**MLVDS**) is the TIA standard (TIA-899). The AdvancedTCA standard specified MLVDS for clock distribution across the backplane to each of the computing module boards in the system

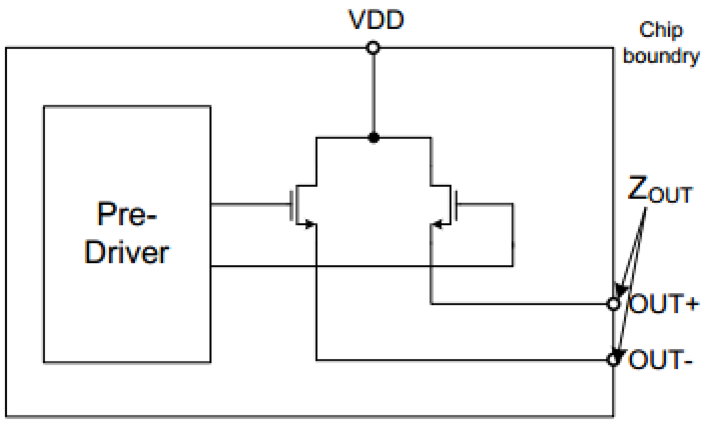


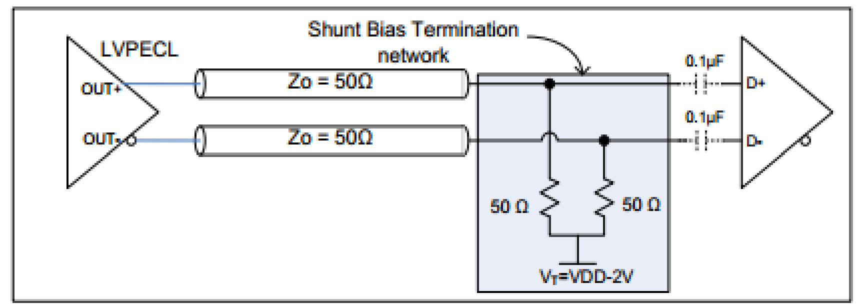
Note – the receivers shown must not have internal terminations.

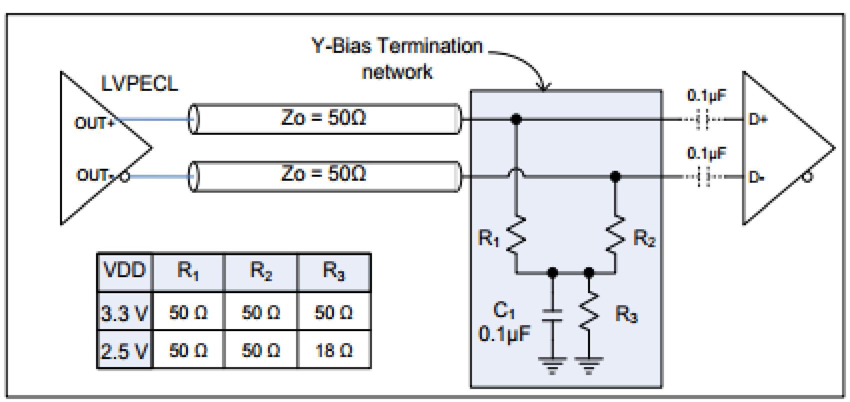
	Output		Input
	Common mode	Amplitude	
Min.	0.3 V	0.480 V	−1.4 V
Max.	2.1 V	0.650 V	3.8 V

Termination, Reflection, Signal Integration

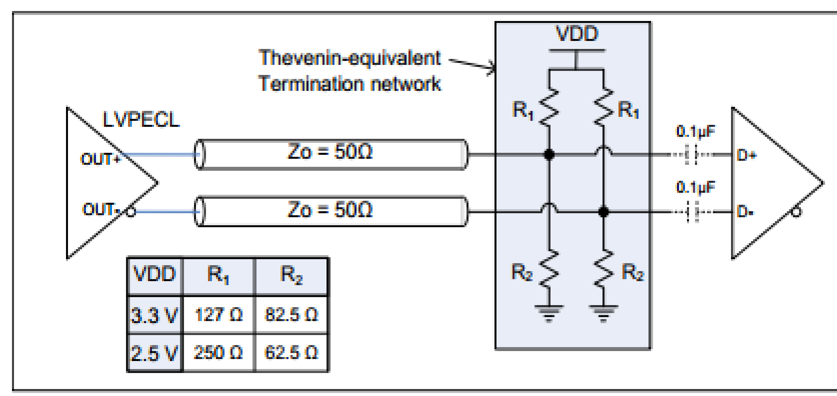
- Coupling
  - DC coupled in low speed
  - AC coupled in high speed
- ECL/LVPECL







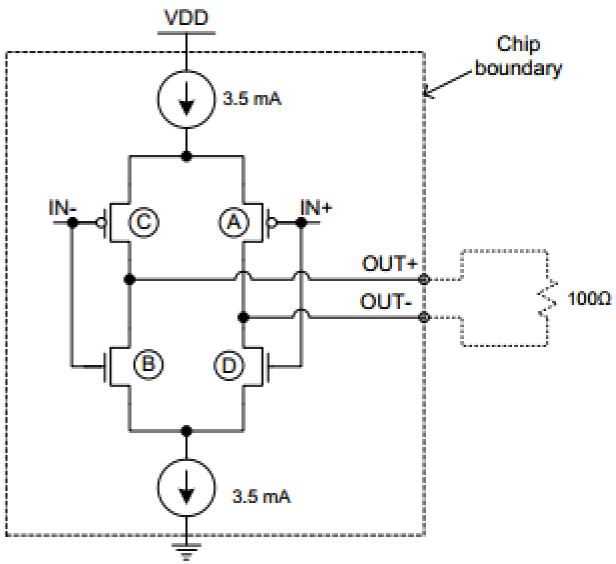
VDD	R_1	R_2	R_3
3.3 V	50 Ω	50 Ω	50 Ω
2.5 V	50 Ω	50 Ω	18 Ω

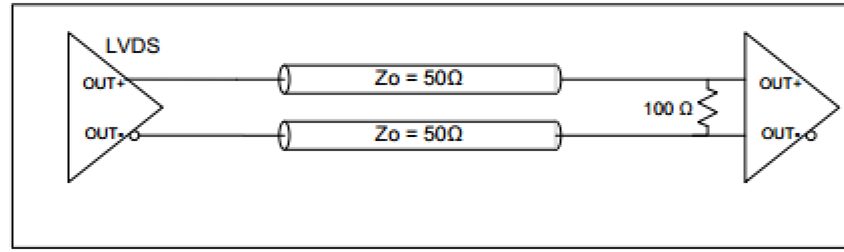


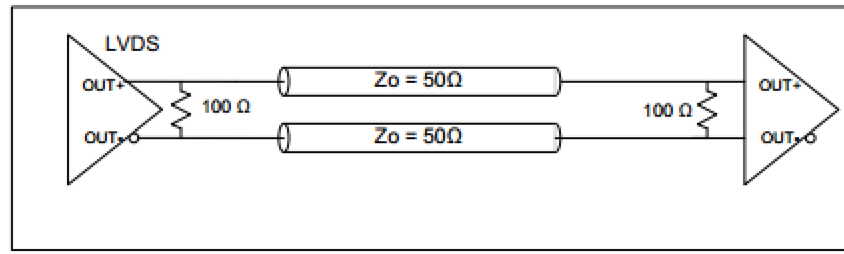
VDD	R_1	R_2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω

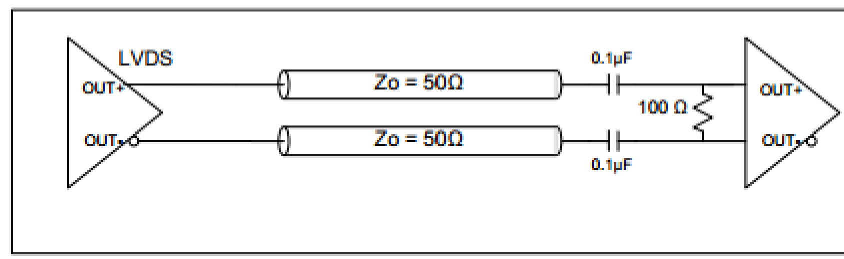
Termination 2

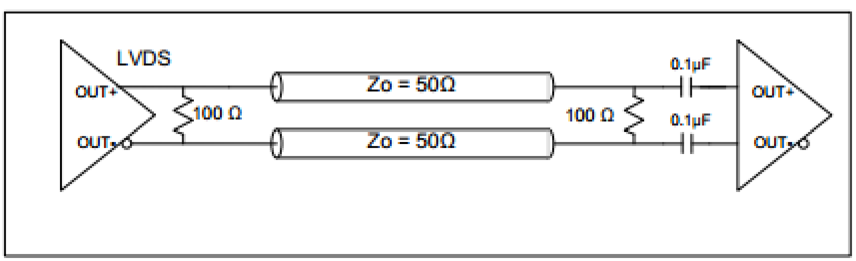
- LVDS

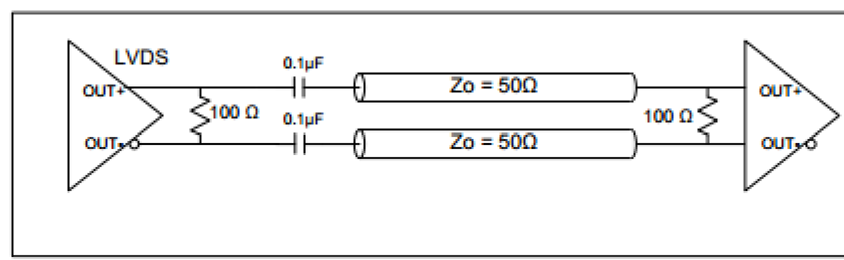




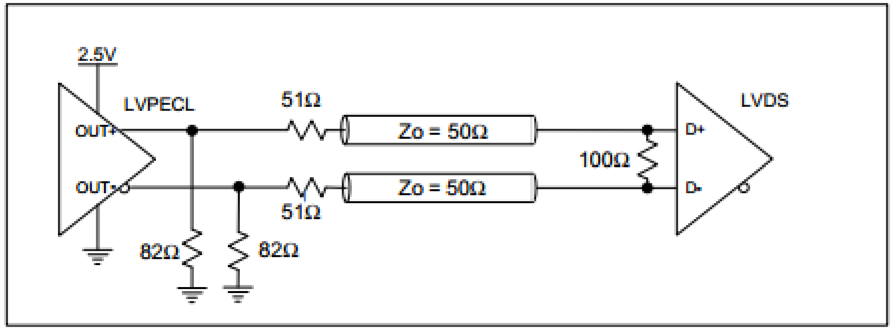


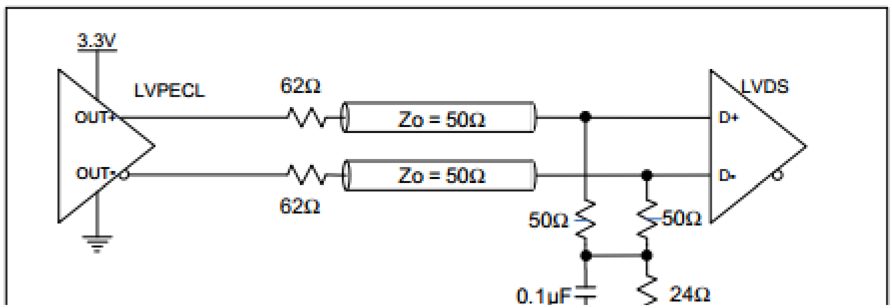


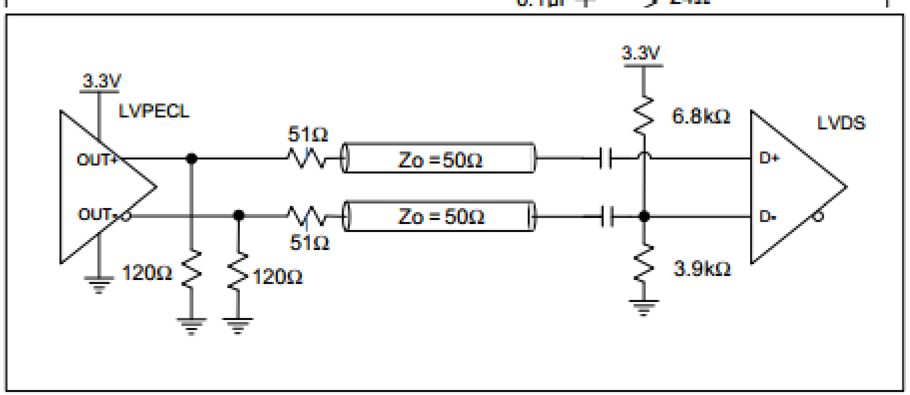




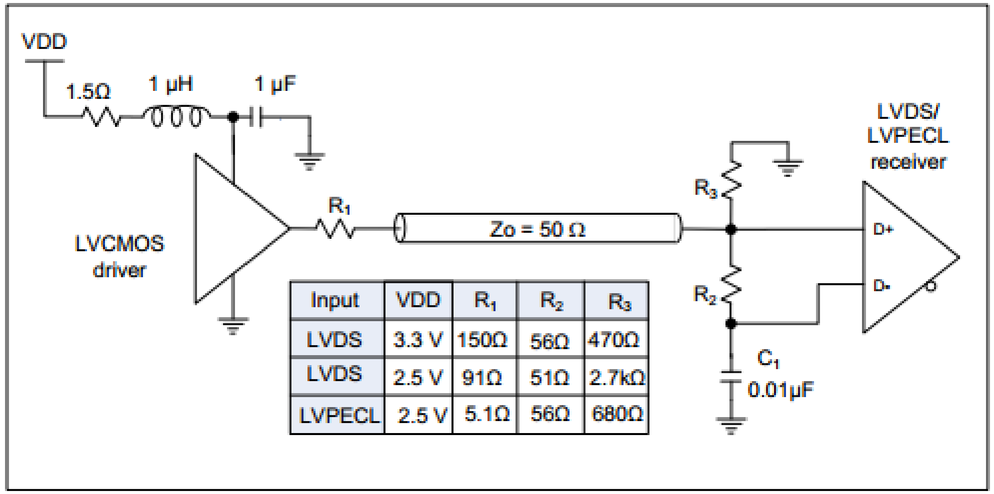
LVPECL-LVDS Level shift



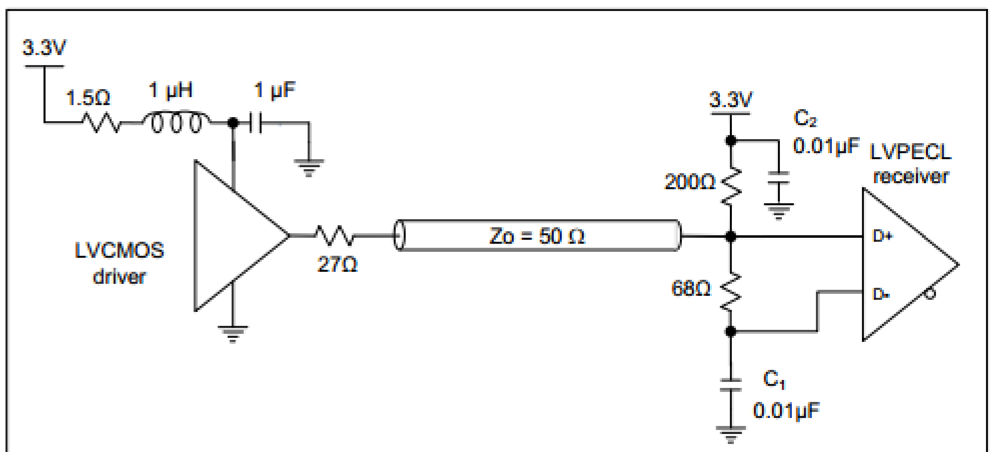




LVCMOS-LVPECL/LVDS Level shift



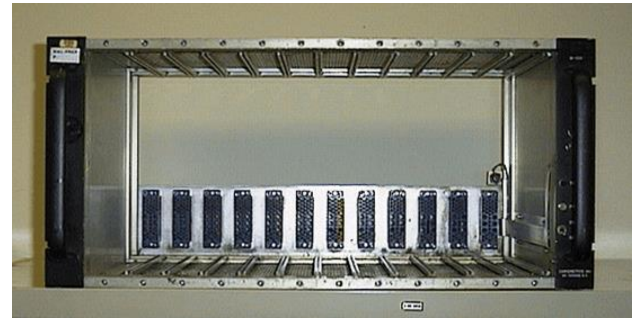
Input	VDD	R_1	R_2	R_3
LVDS	3.3 V	150Ω	56Ω	470Ω
LVDS	2.5 V	91Ω	51Ω	2.7kΩ
LVPECL	2.5 V	5.1Ω	56Ω	680Ω

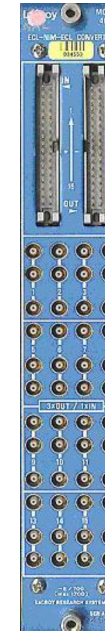


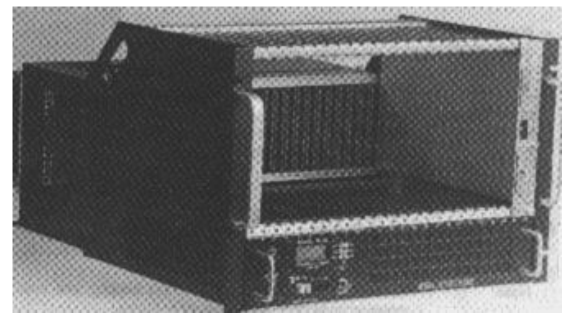
BUS Standards for Nuclear Instrumentation

- 1960's NIM
  - Nuclear Electronics Standard in British Rutherford Lab
  - Same time also in CERN and American Labs
  - NIM: American Standard Bureau and NIM Module Committee
- 70-80's CAMAC, FASTBUS, widely used
  - Nuclear Spectrum Measurement, Particle Physics, Medical Physics, Accelerator Instrument, Accelerator Control, Aerospace, Industrial control.
- ***90's VME from Industry***
- ***2000 CPCI***

- ***Still in use, BUT limited***

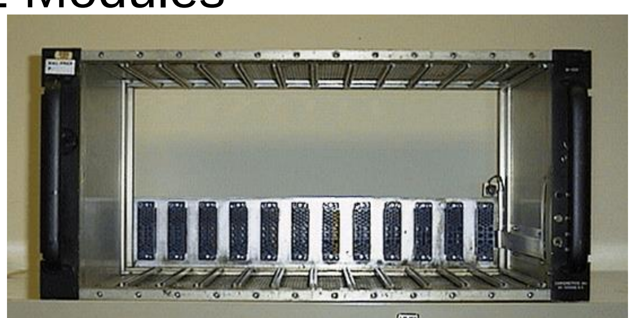






NIM

- **NIM**(Nuclear Instrumentation Module) standard defines
  - mechanical and electrical specifications
  - for electronics modules
  - used in experimental particle and nuclear physics
- Crate
  - Power: ± 6/±12/±24V DC from 220/110V
  - No data BUS
  - 12 Modules

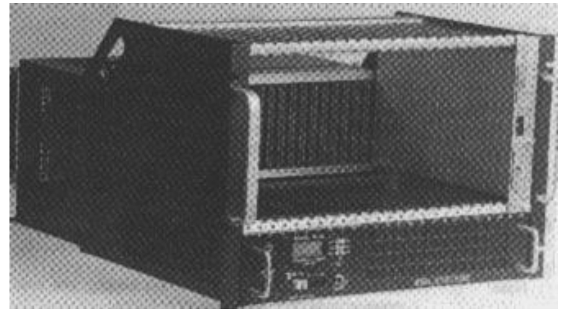


NIM standard module connector pin assignments (required by DOE/ER-0457T)

Pin #	Function	Pin #	Function
1	Reserved [+3 V]	2	Reserved [-3 V]
3	Spare Bus	4	Reserved Bus
5	Coaxial	6	Coaxial
7	Coaxial	8	200 V DC
9	Spare	10	+6 V
11	-6 V	12	Reserved Bus
13	Spare	14	Spare
15	Reserved	16	+12 V
17	-12 V	18	Spare Bus
19	Reserved Bus	20	Spare
21	Spare	22	Reserved
23	Reserved	24	Reserved
25	Reserved	26	Spare
27	Spare	28	+24 V
29	-24 V	30	Spare Bus
31	Spare	32	Spare
33	117 V AC (hot)	34	Power Return Gnd
35	Reset (scaler)	36	Gate
37	Reset (aux)	38	Coaxial
39	Coaxial	40	Coaxial
41	117 V AC (neutral)	42	High Quality Gnd
G	Gnd Guide Pin		

CAMAC

- **CAMAC**: Computer Automated Measurement And Control



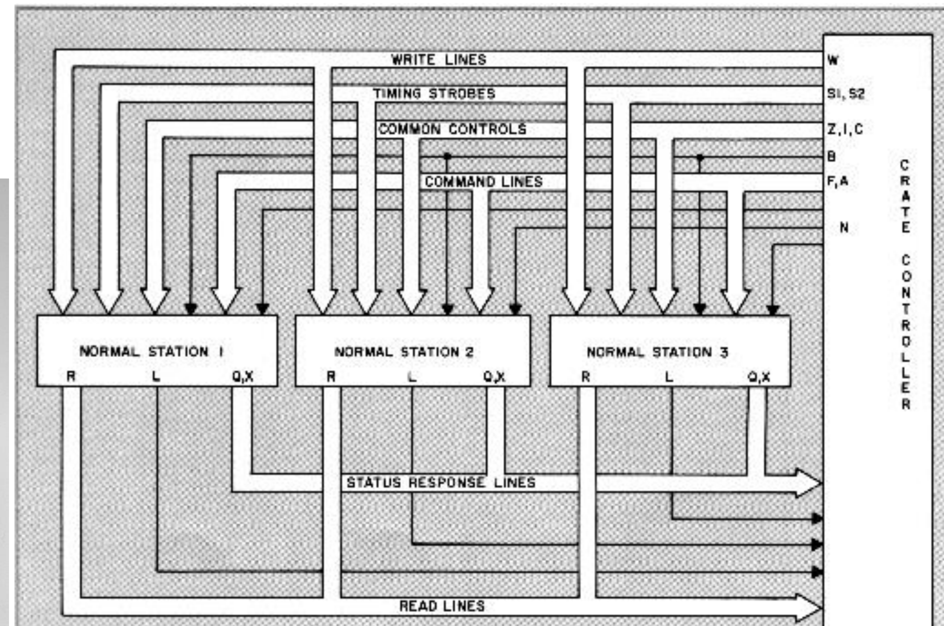
MAXIMUM CURRENT LOADS			
SUPPLY VOLTAGE	VOLTAGE TOLERANCE	IN THE PLUG-IN (PER UNIT WIDTH)*	IN THE CRATE**
Mandatory			
+24 V DC	±0.5%	1 A	6 A
+6 V DC	±2.5%	2 A	25 A
-6 V DC	±2.5%	2 A	25 A
-24 V DC	±0.5%	1 A	6 A
Additional (as required)			
+12 V DC	±0.5%		
-12 V DC	±0.5%		

* See Notes 1 and 3.
** See Note 2.

Table 2

- ESONE Committee: standard EUR 4100 in 1972

- Crate:
  - Data bus:24b
  - Power
  - Control
  - 24+1 station
  - Controller on 25th



Block diagram and signal paths for 3 CAMAC modules and a Crate Controller

!, 2, 3, 4,………………………………23, 25

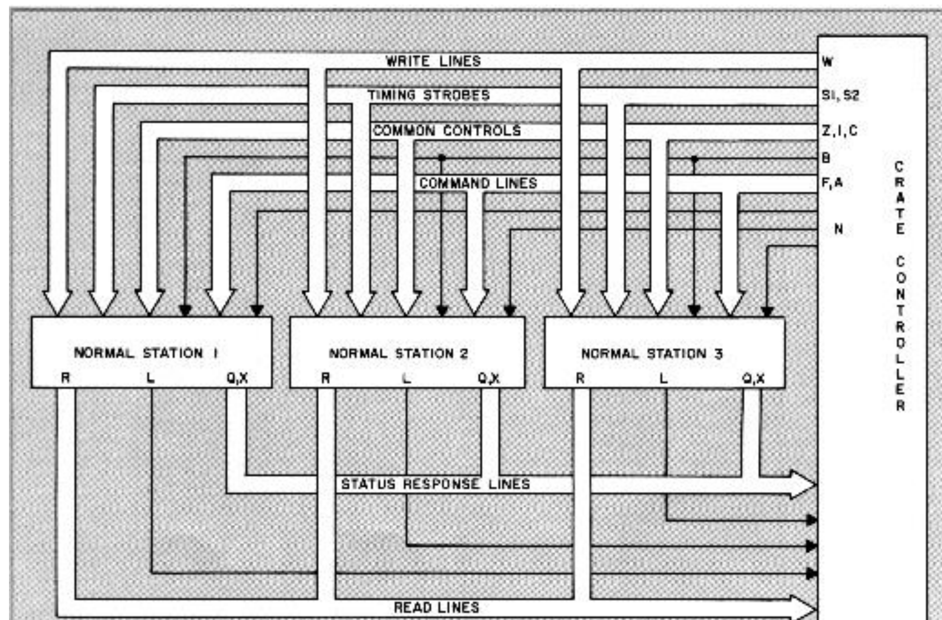
Pin assignments

- Data Way(W24,R24)
- Interrupt:L24
- Station:N24+1
- FA:5+4
- Power:6
- Control:S1S2 ZICB QX

STANDARD DATAWAY USAGE

TITLE	DESIGNATION	CON-TACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module (individual line from control station).
Sub-Address	A1,2,4,8	4	Selects a section of the module.
Function	F1,2,4,8,16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation. (Dataway signals may change.)
Strobe 2	S2	1	Controls second phase. (Dataway signals may change.)
Data			
Write	W1-W24	24	Bring information to the module.
Read	R1-R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.

TITLE	DESIGNATION	CON-TACTS	USE AT A MODULE
Common Controls			Operate on all stations connected to them, no command required.
Initialize	Z	1	Sets module to a defined state. (accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers (accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1, P2	2	For specified uses.
Patch Contacts	P3-P5	3	For unspecified interconnections. No Dataway lines.
Mandatory Power Lines			
+24 V DC	+24	1	
+6 V DC	+6	1	
-6 V DC	-6	1	
-24 V DC	-24	1	
0 V	0	2	Power return.
Additional Power Lines			Lines are reserved for the following power supplies.
+12 V DC	+12	1	Low current for indicators, etc.
-12 V DC	-12	1	Reference for circuits requiring clean earth.
Clean Earth	E	1	
Reserved Y1, Y2	2		Reserved for future allocation.



Block diagram and signal paths for 3 CAMAC modules and a Crate Controller.

A-599

Pin assignment

Normal Module station

PIN ALLOCATION AT NORMAL STATION
(view from module side)
(STATIONS 1-24)

Bus line	Free Bus line	P1	B	Busy	Bus line
Bus line	Free Bus line	P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual line	Station Number	N	A2	Subaddress	Bus line
Individual line	Look-at-Me	L	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
24 Write Bus Lines		W16	W15		
W1=LSB		W14	W13		
W24=MSB		W12	W11		
		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
24 Read Bus Lines		R16	R15		
R1=LSB		R14	R13		
R24=MSB		R12	R11		
		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
	-12 V DC	-12	-24	-24 V DC	
		NC	-6	-6 V DC	
		NC	NC		
Power	Auxiliary -6 V supply	Y1	E	Clean Earth	Power
Bus lines	-12 V DC	+12	+24	+24 V DC	Bus lines
	Auxiliary +6 V supply	Y2	+6	+6 V DC	
	0 V (Power Return)	0	0	0 V (Power Return)	

Table 3b

Control Module station

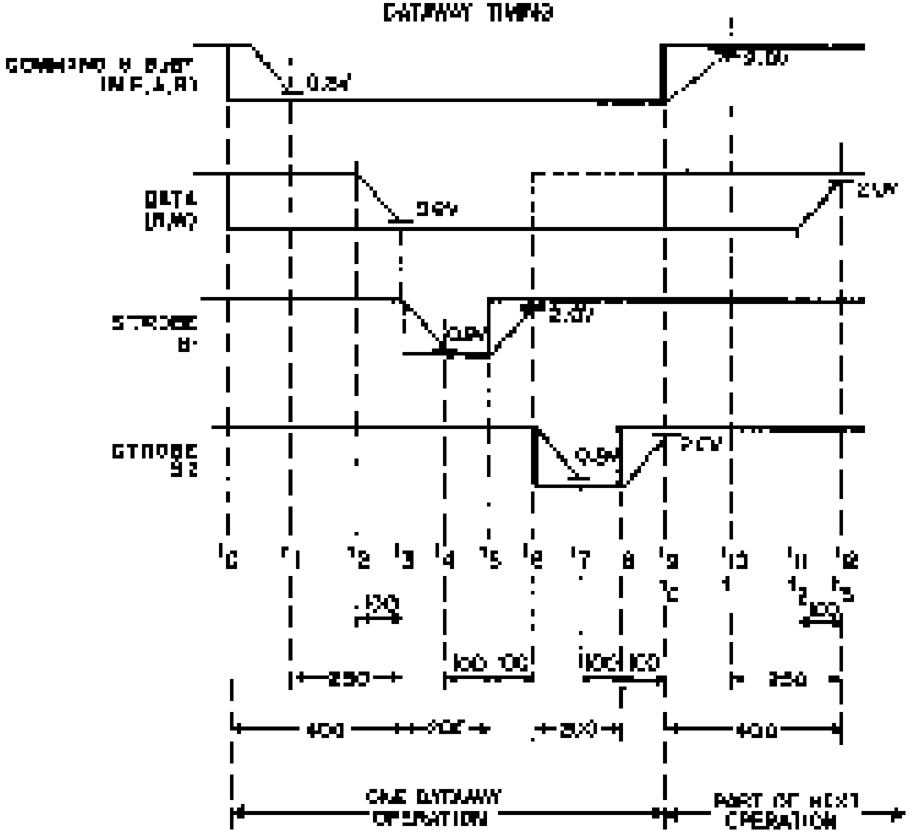
PIN ALLOCATION AT CONTROL STATION
(STATION 25)

Individual patch contact		P1	B	Busy	Bus line
Individual patch contact		P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual patch contact		P6	A2	Subaddress	Bus line
Individual patch contact		P7	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
		L13	N13		
24 Individual Look-at-Me Lines		L12	N12	24 Individual Station	
L1 from Station 1, etc.		L11	N11	Number lines	
		L10	N10	N1 to Station 1, etc.	
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
	-12 V DC	-12	-24	-24 V DC	
		NC	-6	-6 V DC	
		NC	NC		
Power	Auxiliary -6 V supply	Y1	E	Clean Earth	Power
Bus lines	-12 V DC	+12	+24	+24 V DC	Bus lines
	Auxiliary +6 V supply	Y2	+6	+6 V DC	
	0 V (Power Return)	0	0	0 V (Power Return)	

Table 3a

Timing and data rate

- Data Cycle: 1us
- Data width:24b=3B
- Rate:24bps=3Bps



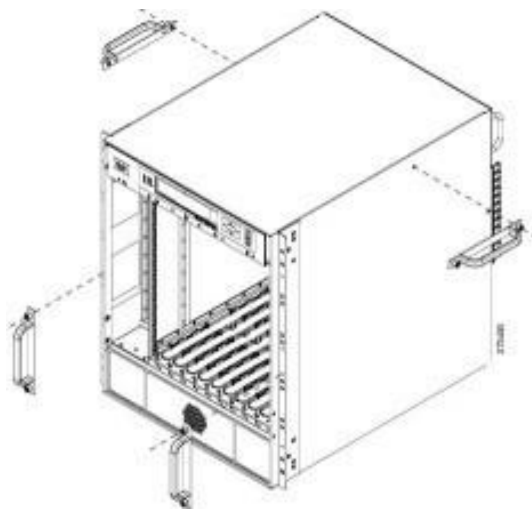
Times given are maximum values in ideal timing of a Dataway operation.

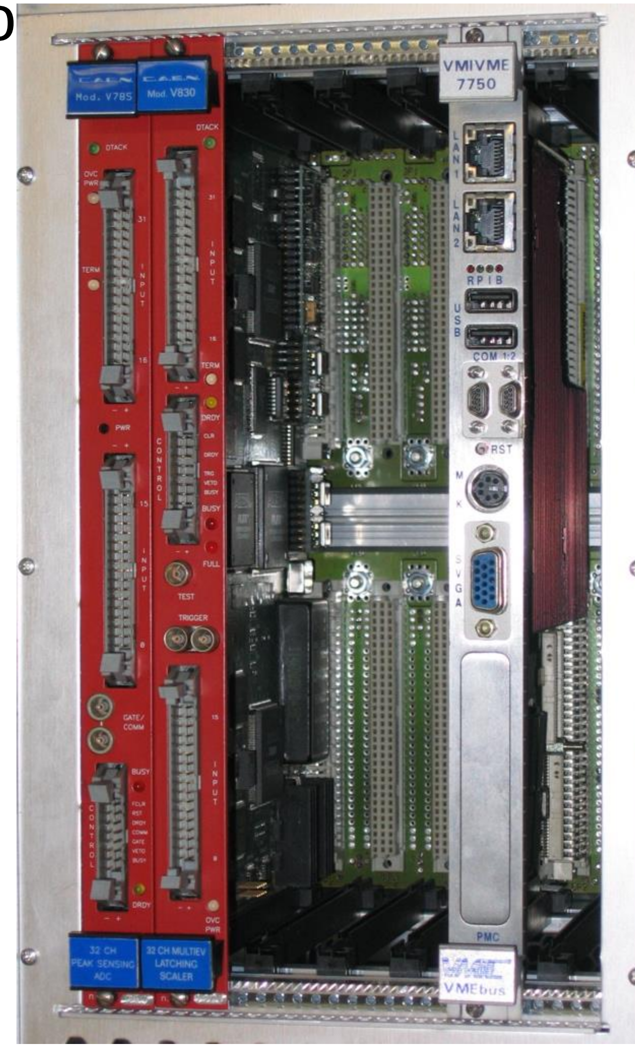
Fastbus/CPCI/PCI-E

- I skip these standards due time limit but you could note them for later reference

VMEbus was commonly used

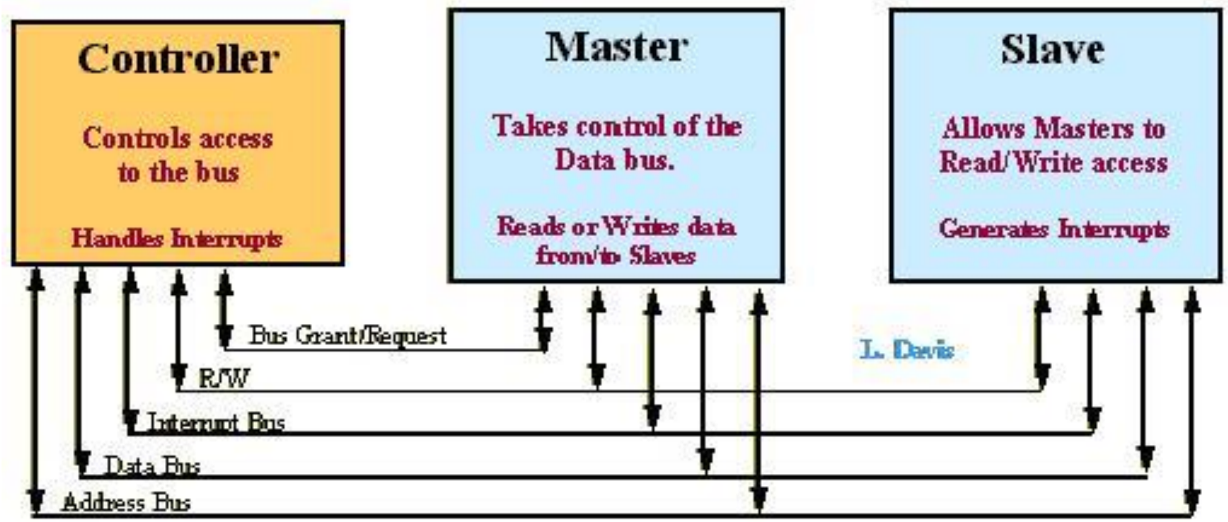
- **VMEbus**(Versa Module Europa bus)
  - a computer bus standard, originally fo the Motorola 68000 CPUs,
  - standardized by the IEC as ANSI/IEEE 1014-1987
- Crate:
  - 1-21 stations
  - Controller on 1st
- Modules
  - 3U,6U and 9U
- Power:
  - VME32: +5volt,and +/-12volt supply; VME64a 3.3volt supply





Module types

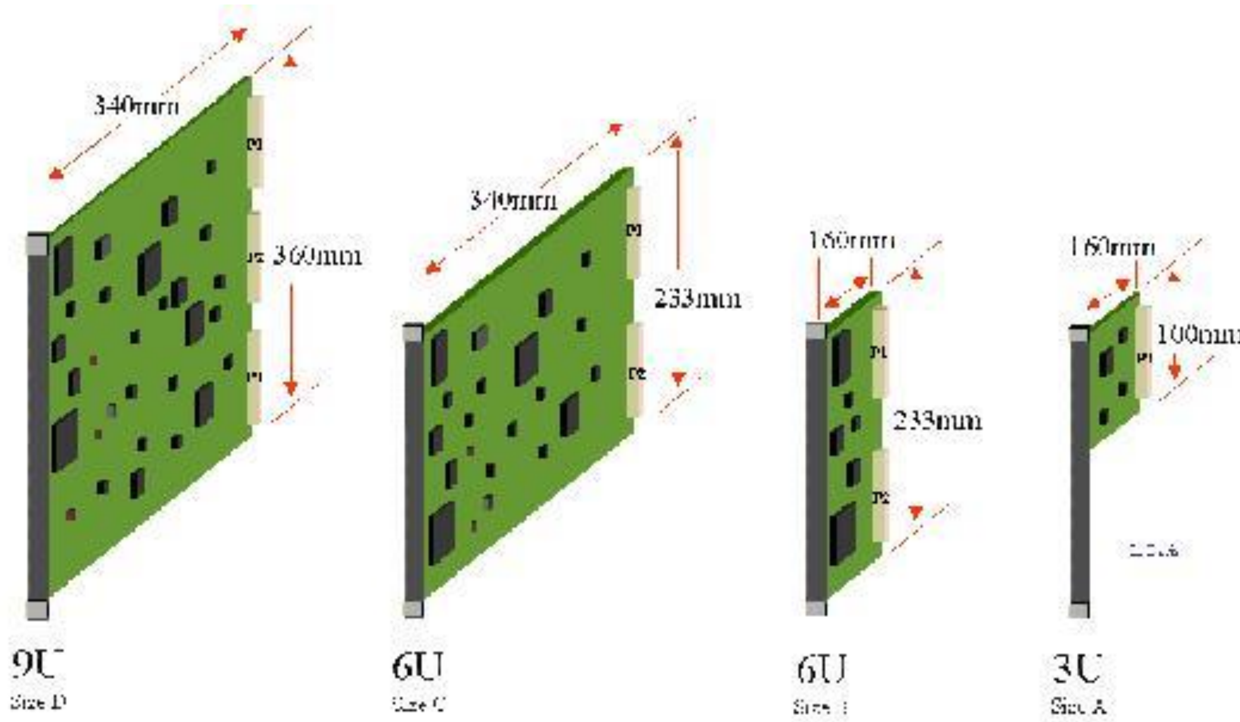
- Controller
- Master
- Slave



Evolution of VME			
Topology	Year	Bus Cycle	Maximum Speed (Mbyte / Sec)
VMEbus32 Parallel Bus Rev A	1981	BLT	40
VMEbus IEEE-1014	1987	BLT	40
VME64	1994	MBLT	80
VME64x	1997	2eVME	160
VME320	1997	2eSST	320

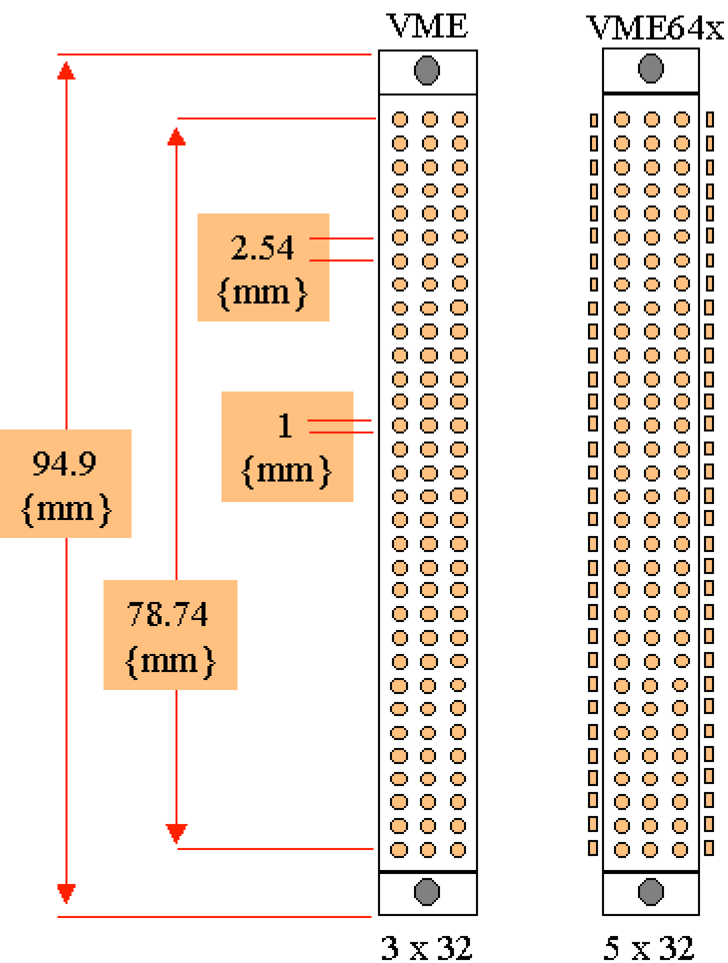
Module types

- Types
  - 3U
    - 160×100mm
    - P1
  - 6U
    - 160×233mm
    - 340×233mm
    - P1 + P2
  - 9U
    - 340×366mm
    - 400×366mm
    - P1+P2+P3



- Data/Addr space:
  - 8/16/32/64b

VMEbus and VME64 P1 Connectors



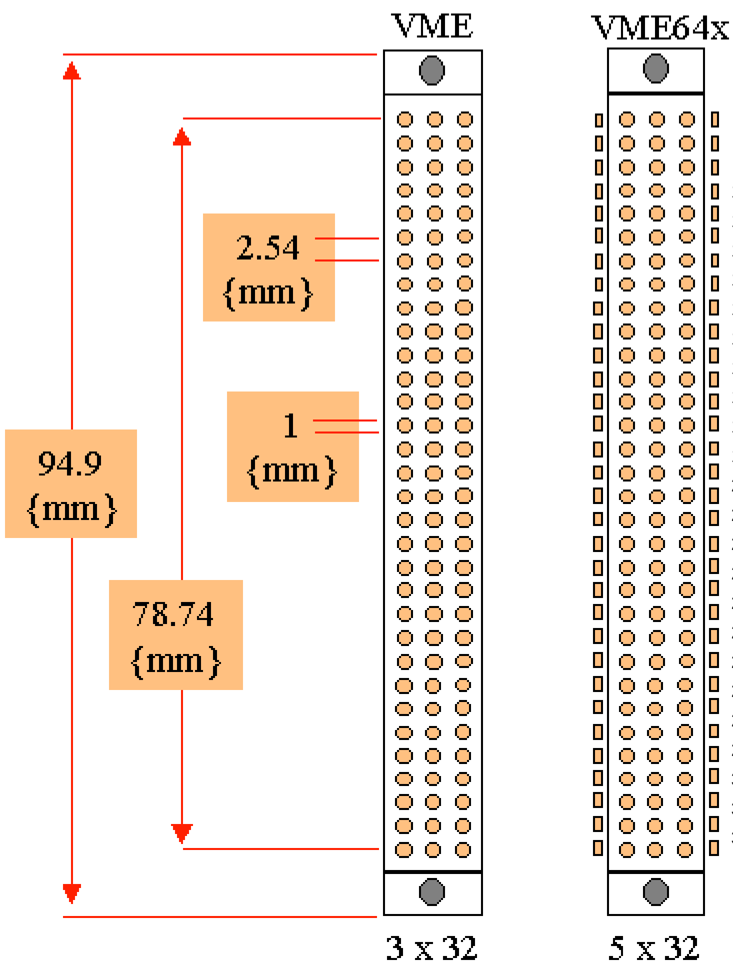
Pin #	Signal Name Row A	Signal Name Row B	Signal Name Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BRO*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12v	+5v Standby	+12v
32	+5v	+5v	+5v

VME64x P1 Connector

Pin	Signal Name Row z	Signal Name Row A	Signal Name Row B	Signal Name Row C	Signal Name Row d
1	MPR	D00	BBSY*	D08	VPC
2	GND	D01	BCLR*	D09	GND
3	MCLK	D02	ACFAIL*	D10	+1V
4	GND	D03	BG0IN*	D11	+V2
5	MSD	D04	BG0OUT*	D12	RsvU
6	GND	D05	BG1IN*	D13	-V1
7	MMD	D06	BG1OUT*	D14	-V2
8	GND	D07	BG2IN*	D15	RsvU
9	MCTL	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0
11	RESP*	GND	BG3OUT*	BERR*	GA1
12	GND	DS1*	BR0*	SYSREST*	+3.3v
13	RsvBus	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3V
15	RsvBus	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3.3V
17	RsvBus	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3.3V
19	RsvBus	GND	AM3	A19	RsvBus
20	GND	IACK*	GND	A18	+3.3V
21	RsvBus	IACKIN*	SERCLK	A17	RsvBus
22	GND	IACKOUT*	SERDAT*	A16	+3.3V
23	RsvBus	AM4	GND	A15	RsvBus
24	GND	A07	IRQ7*	A14	+3.3V
25	RsvBus	A06	IRQ6*	A13	RsvBus
26	GND	A05	IRQ5*	A12	+3.3V
27	RsvBus	A04	IRQ4*	A11	LI/I*
28	GND	A03	IRQ3*	A10	+3.3V
29	RsvBus	A02	IRQ2*	A09	LI/O*
30	GND	A01	IRQ1*	A08	+3.3V
31	RsvBus	-12V	+5V Standby	+12V	GND
32	GND	+5V	+5v	+5V	VPC

www.interfacebus.com L. Davis

VMEbus and VME64 P2 Connectors



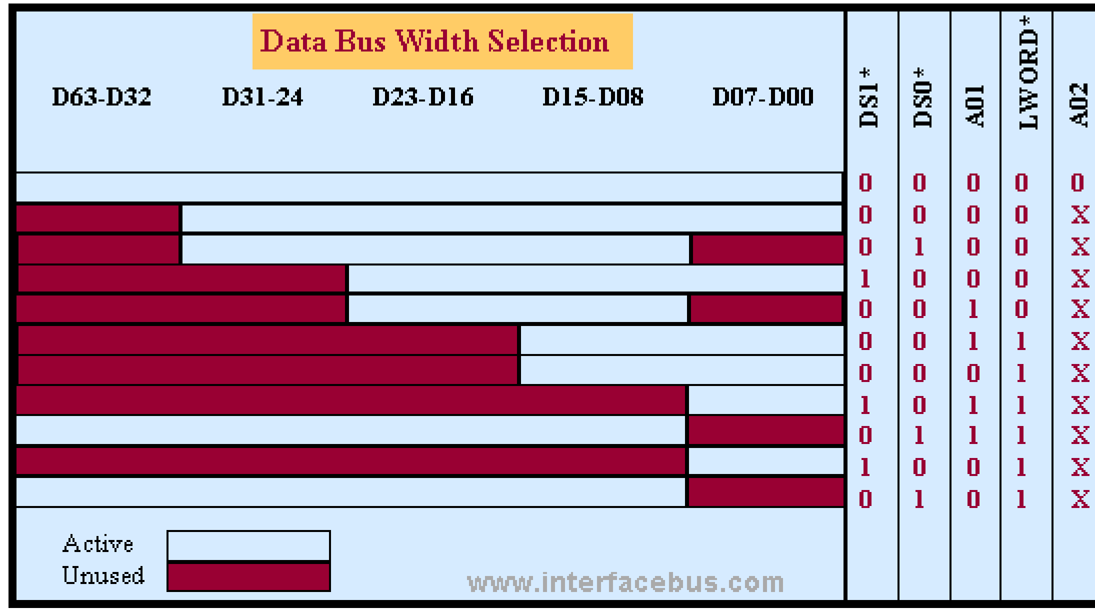
Pin #	Signal Name Row A	Signal Name Row B	Signal Name Row C
1		+5v	
2		GND	
3		RETRY	
4		A24	
5		A25	
6		A26	
7		A27	
8		A28	
9		A29	
10		A30	
11		A31	
12		GND	
13		+5v	
14		D16	
15		D17	
16	User Defined	D18	User Defined
17		D19	
18		D20	
19		D21	
20		D22	
21		D23	
22		GND	
23		D24	
24		D25	
25		D26	
26		D27	
27		D28	
28		D29	
29		D30	
30		D31	
31		GND	
32		+5V	

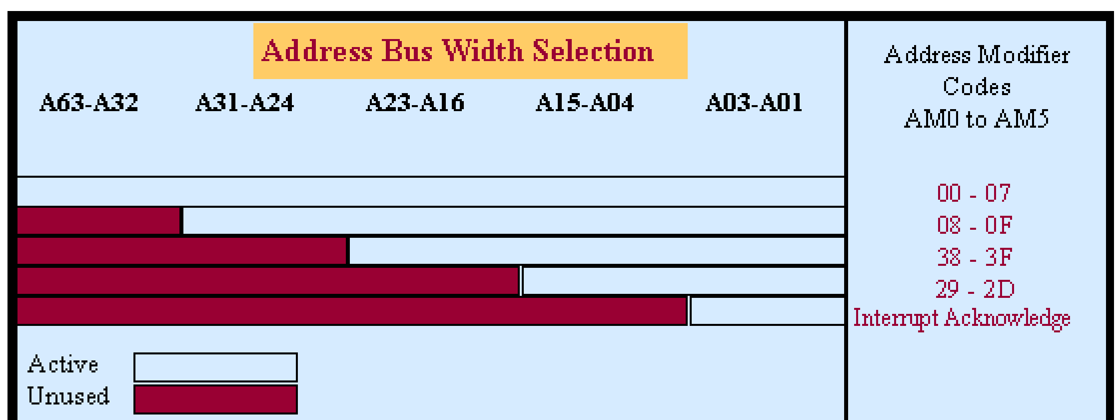
VME64x P2 Connector					
Pin	Signal Name Row z	Signal Name Row A	Signal Name Row B	Signal Name Row C	Signal Name Row d
1	UsrDef	UsrDef	+5V	UsrDef	UsrDef
2	GND	UsrDef	GND	UsrDef	UsrDef
3	UsrDef	UsrDef	RETRY	UsrDef	UsrDef
4	GND	UsrDef	A24	UsrDef	UsrDef
5	UsrDef	UsrDef	A25	UsrDef	UsrDef
6	GND	UsrDef	A26	UsrDef	UsrDef
7	UsrDef	UsrDef	A27	UsrDef	UsrDef
8	GND	UsrDef	A28	UsrDef	UsrDef
9	UsrDef	UsrDef	A29	UsrDef	UsrDef
10	GND	UsrDef	A30	UsrDef	UsrDef
11	UsrDef	UsrDef	A31	UsrDef	UsrDef
12	GND	UsrDef	GND	UsrDef	UsrDef
13	UsrDef	UsrDef	+5V	UsrDef	UsrDef
14	GND	UsrDef	D16	UsrDef	UsrDef
15	UsrDef	UsrDef	D17	UsrDef	UsrDef
16	GND	UsrDef	D18	UsrDef	UsrDef
17	UsrDef	UsrDef	D19	UsrDef	UsrDef
18	GND	UsrDef	D20	UsrDef	UsrDef
19	UsrDef	UsrDef	D21	UsrDef	UsrDef
20	GND	UsrDef	D22	UsrDef	UsrDef
21	UsrDef	UsrDef	D23	UsrDef	UsrDef
22	GND	UsrDef	GND	UsrDef	UsrDef
23	UsrDef	UsrDef	D24	UsrDef	UsrDef
24	GND	UsrDef	D25	UsrDef	UsrDef
25	UsrDef	UsrDef	D26	UsrDef	UsrDef
26	GND	UsrDef	D27	UsrDef	UsrDef
27	UsrDef	UsrDef	D28	UsrDef	UsrDef
28	GND	UsrDef	D29	UsrDef	UsrDef
29	UsrDef	UsrDef	D30	UsrDef	UsrDef
30	GND	UsrDef	D31	UsrDef	UsrDef
31	UsrDef	UsrDef	GND	UsrDef	GND
32	GND	UsrDef	+5v	UsrDef	VPC

www.interfacebus.com L. Davis

Very convenient Data Width and Adr. Width

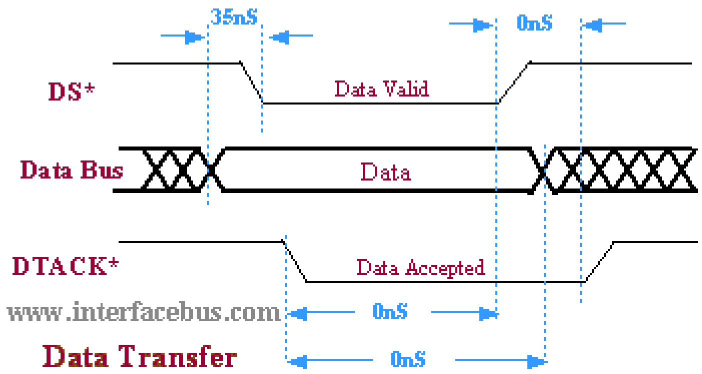
- Data Width:
  - 8-64bits
- Addr Width
  - 8-64bits

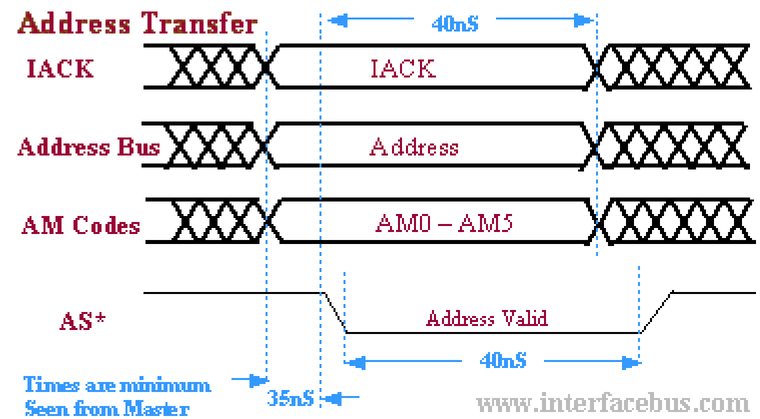


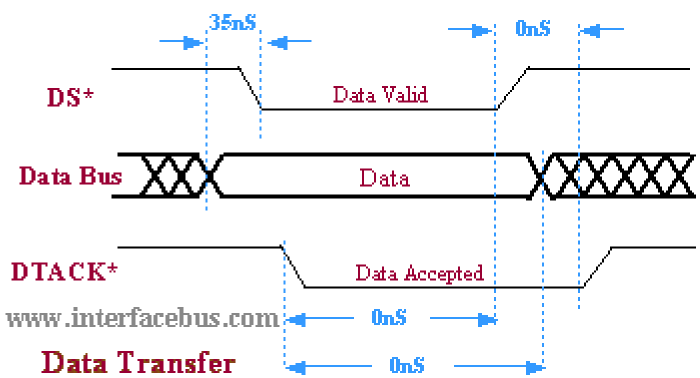


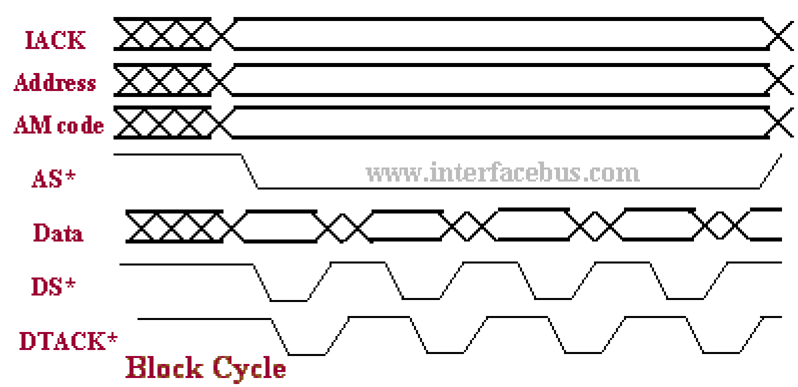
Asynchronous Timing makes compatibility

- Strobe
- As
- DTACK
- Block



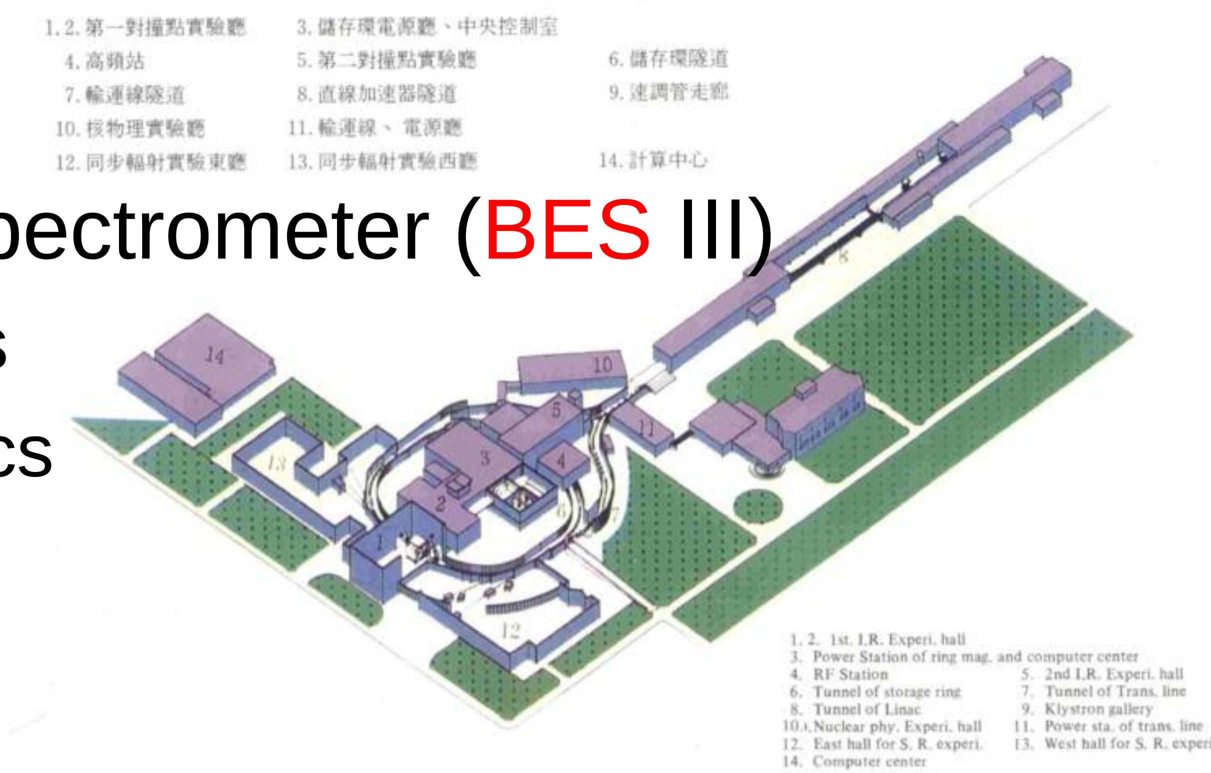






New Standard again?

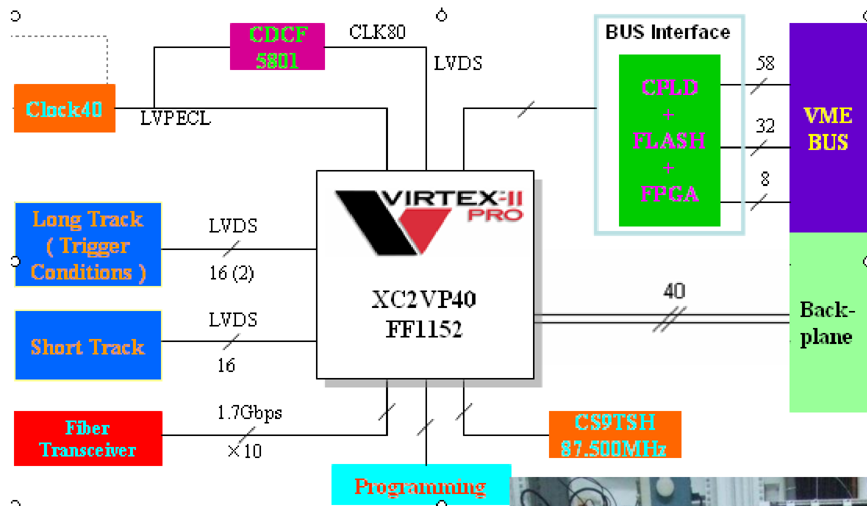
- Upgrade of Beijing Electron Positron Collider (BEPC II） in China Beijing in 2002
  - From single ring to double Rings
  - L~$10^{33}cm^{-2}S^{-1}$

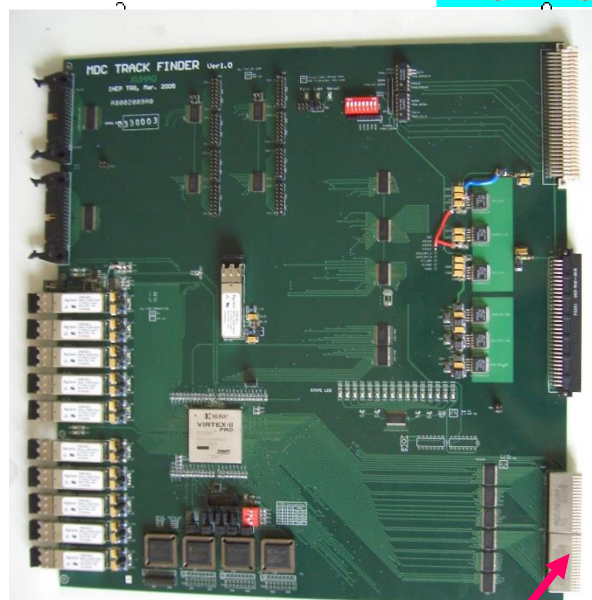


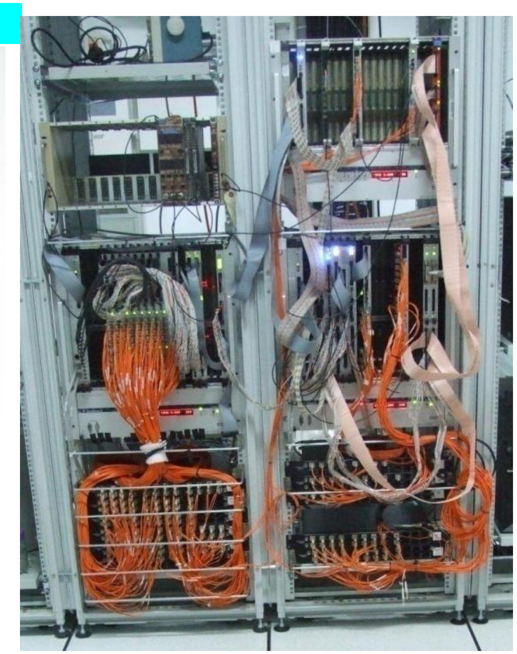
- New BEijing Spectrometer (BES III)
  - New Detectors
  - New Electronics
  - New Trigger
  - New DAQ

We did meet BUS Problems!

- VME（2003/4）Not satisfactory
  - Higher samples/s
  - Powerful FPGA
  - >3Gbps transmission
  - reconfiguration
  - ……
- Problem
  - Bus bandwidth too low
  - No serial interconnection
  - No Intelligence
- New standard is needed







BESIII Module

Private BUS

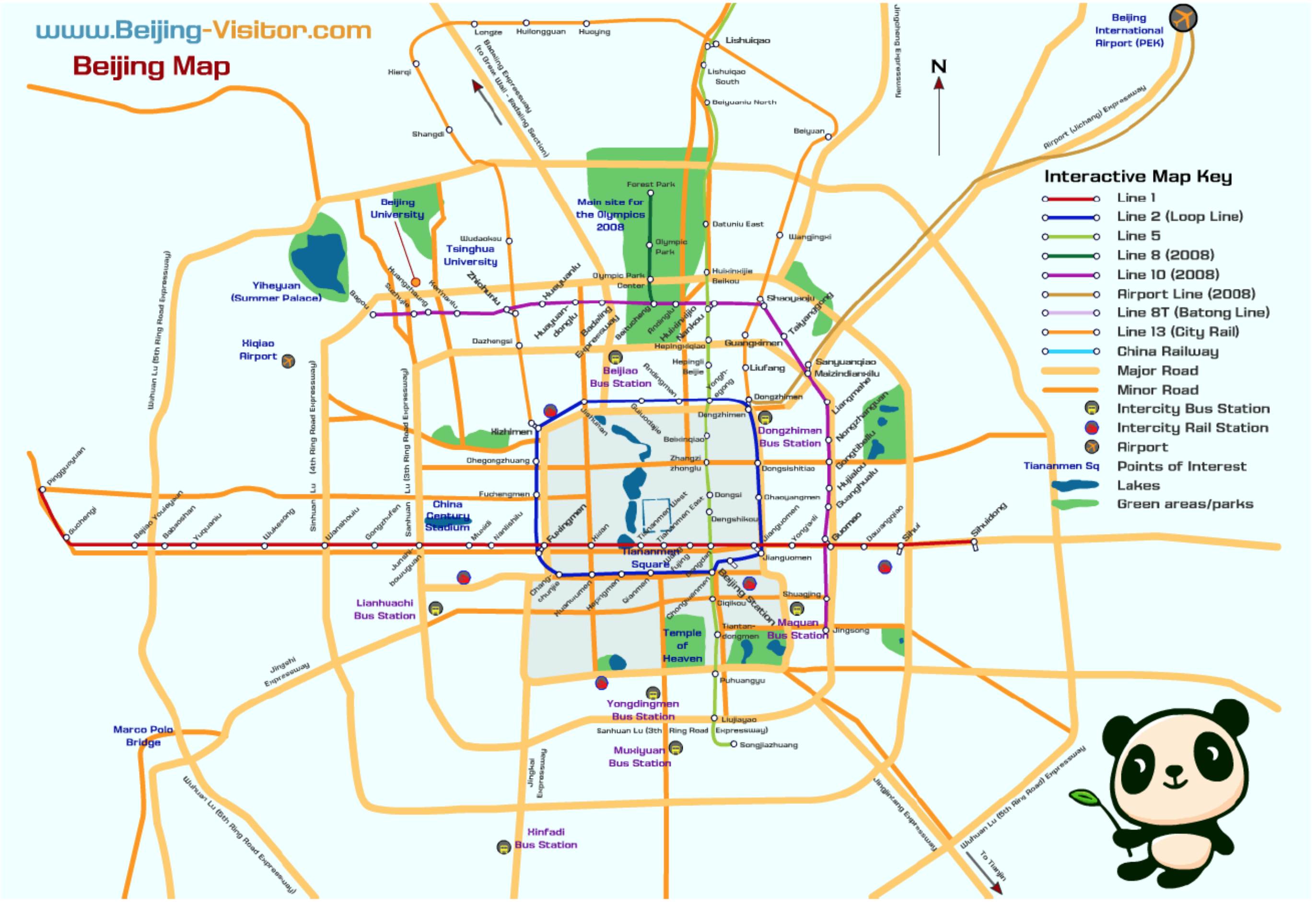
205Gb/s synch trans. In BESIII

Pre-xTCA workshops

- At same time, ongoing International Linear Collider, XFEL workshops
  - 2004 - ATCA, MTCA intro paper NSS-MIC, Rome
  - 2005 – ILC Snowmass Conference + Availability Workshop @ Grömitz on ATCA for *high availability*
  - 2007 – 1st ATCA workshop, IEEE RT2007 Fermilab
  - 2008 – 2nd ATCA workshop, IEEE NSS-MIC Dresden

Problem with BUSed crate?

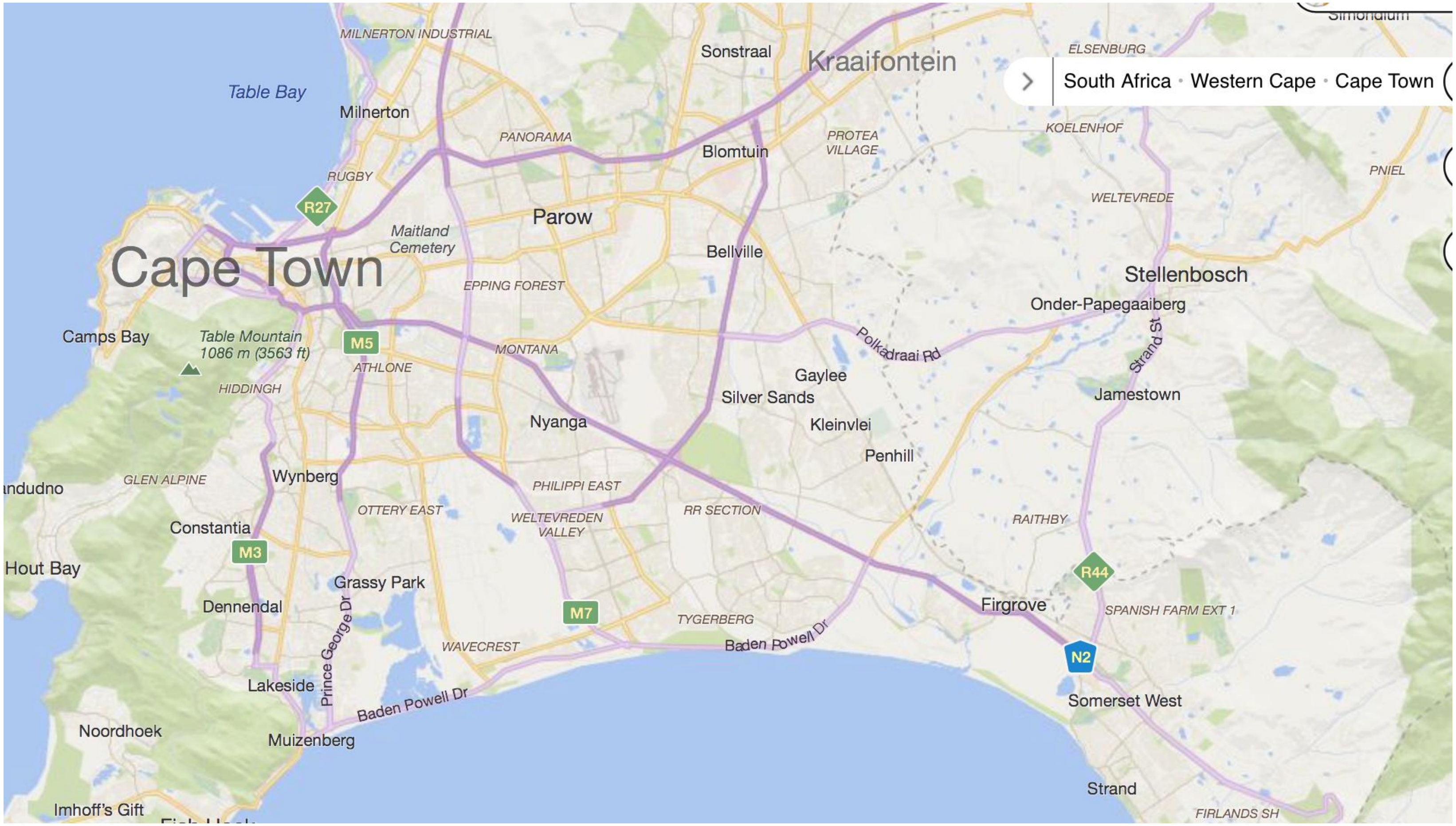
- Beijing Traffic Rings(BUS like) do make problem!
  - 2nd ring
  - 3rd ring
  - 4th ring
  - 5th ring
  - 6th ring
  - 7th ring



- Bottlenecks!

Good solution like Cape Town Routes

- Point to point direct or via limited routing is effective!



What is the new standard?

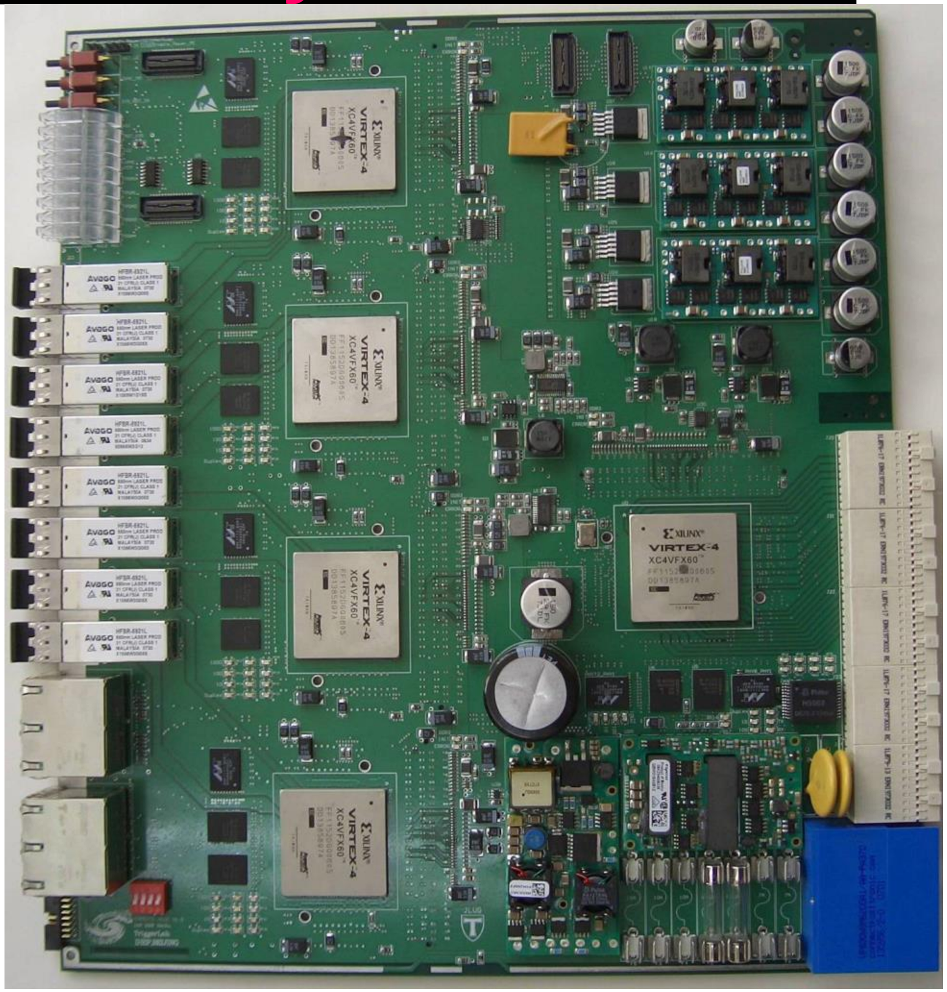
- ATCA
  - Advantages
    - High speedIO and 10Gb/s interconnections
    - HA ~99.999%
    - IP management
- MicroTCA (MTCA)
  - Advantages of ATCA
  - Half height, compact system
- AdvancedMC（AMC）
  - Modular design

Should we adopt industrial standard again as VME？

Good idea!

Why xTCA for Physics

- ATCA shortages
  - Height 8U, not suitable for machine control
  - No rear transition board yet
  - No control signals
  - ……
- MTCA shortages
  - No rear transition board yet （HA）
  - No control sysnals …
- AMC shortages
  - Inter connection?
  - Control signals?
  - pin signal difinition
  - …

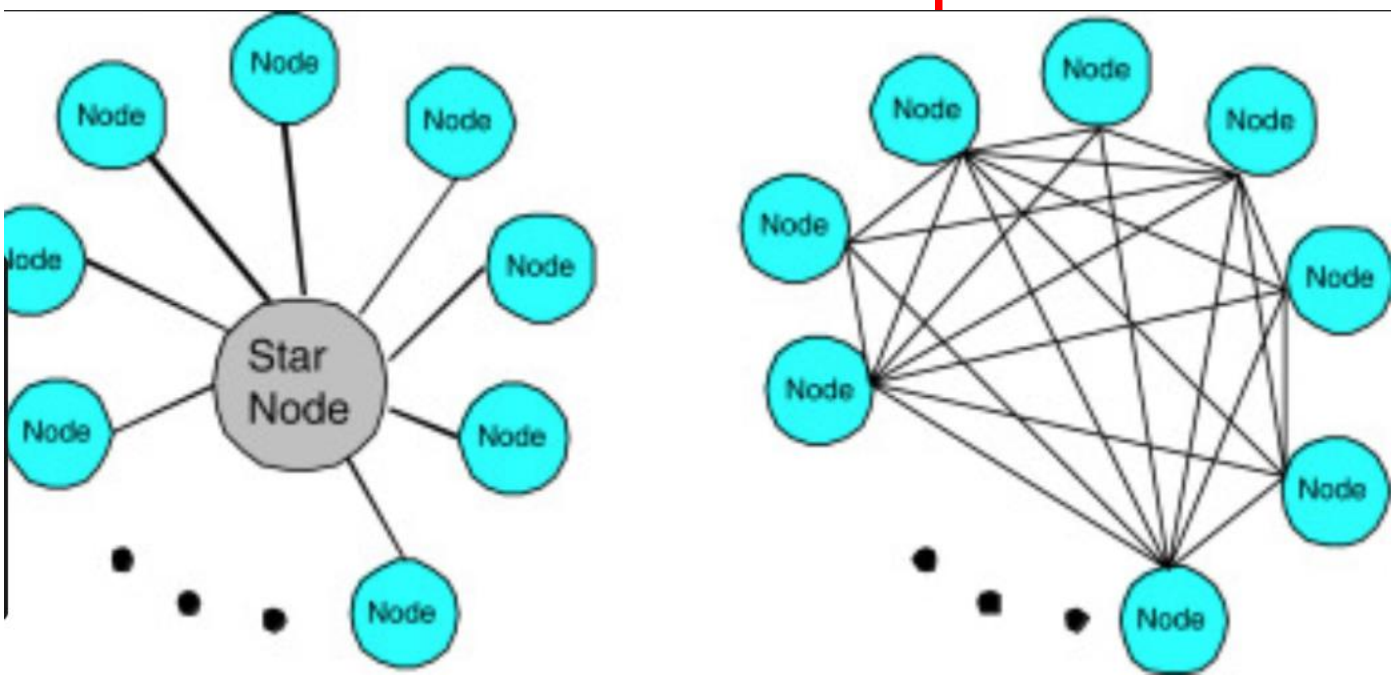


Compute Node designed by IHEP

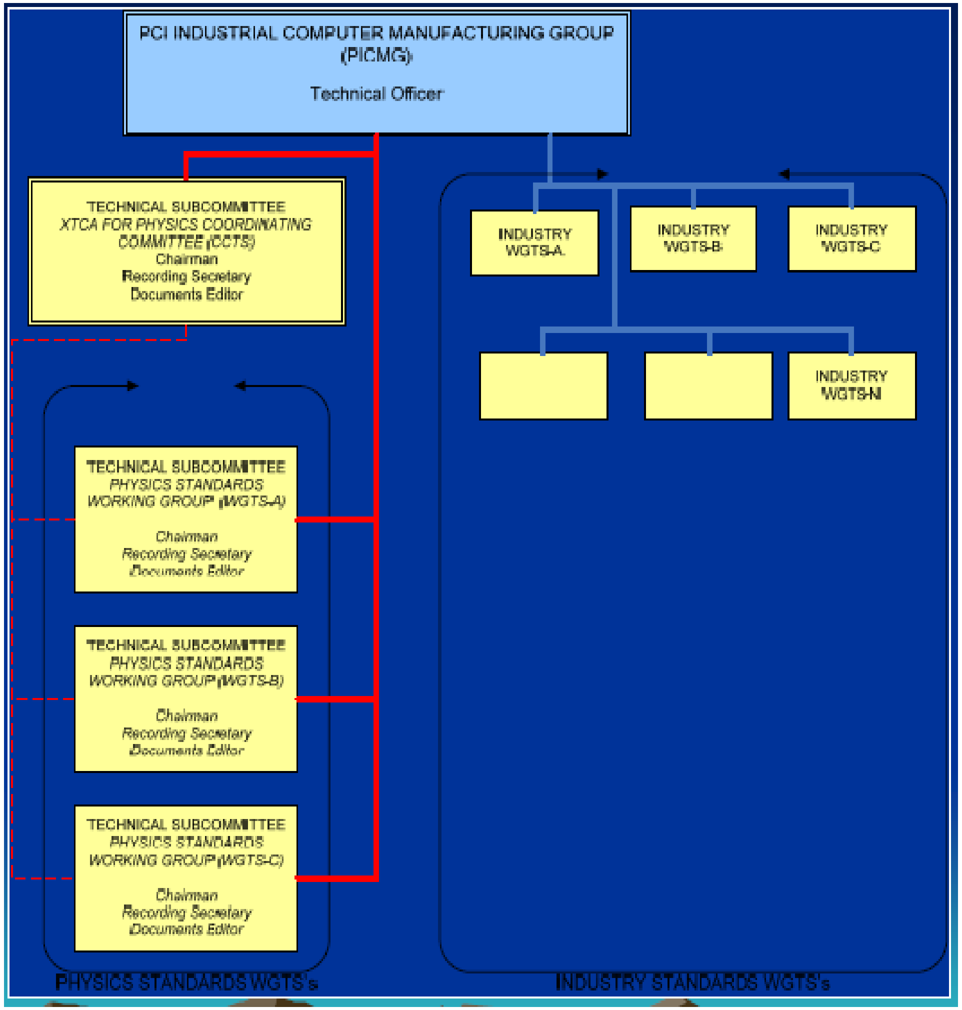
New standard: xTCA for Physics

It is possible to have a direct link!

- YES! That ATCA/xTCA
  - 2009 –xTCA for Physics subcommittees formed under PICMG open source telecom standards ~200 vendors
- 2009 – First xTCA Workshops at IHEP Beijing



xTCA for Physics CCTS



- Founded Mar. 10 2009 under PICMG
  - DESY/FNAL/IHEP/SLAC
  - >40 companies
  - Officers
    - Chair: SLAC Ray Larsen
    - Secretory: TriCircle Augustus Lowell
    - Doc Editor: IHEP Z.-A. Liu

New Standard

- Serial Point2Point transmission to substitute BUS-ed data transmission!
- Present and Future
  - Point to Point
    - VPX, new generation from VME from Industry (do not talk this time)
    - xTCA for Physics initiated from Physics
  - High speed
    - 1.6Gbps,3.2Gbps,6.4Gbps,10Gbps（present）
  - Future: 16Gbps/25Gbps(100G) and System on Chip?

xTCA features

- ATCA & MicroTCA Unique Features
  - ATCA board, shelf is first modular computer architecture with completely serial multi-Gbps backplane
  - Serial ports are bidirectional pairs in star or mesh topology
  - Serial bit rate of one port at 2.5 Gbps exceeds data rate of parallel bus backplanes, e.g. VME 32/64 bit word at 10 MHz => 320/640 Mbps (*now 2.5G=>10G=> 40 G*)
  - Architecture based on FPGAs with imbedded SERDES Tx-Rx, LVDS balanced logic
  - High processing power of single ATCA card (Blade)
  - MCH enables module to any other module communication
  - Special low jitter switches for clocks
  - Dual redundancy MCH, Processor, Power Units - optional

xTCA **Standards – Hardware Extensions**

- 3 Key specifications
  - ATCA Card => PICMG 3.8
    - Zone 3 area defined but interface left to discretion of vendors
    - Severely limits interoperability of vendor modules
    - Physics developed ATCA Standard RTM Interface
    - Fabric, power, JTAG, IPMI, managed from ATCA
  - MicroTCA Double-Wide Card => MTCA.4
    - MTCA.0 defined double-wide AMC but not Zone 3 or RTM mechanics
    - MTCA.4 developed new crate, RTM, interface, cooling
    - Fabric, power, JTAG, IPMI, managed from AMC
    - RTM hot-swappable
  - **Physics Design Guide**

xTCA **Physics Extensions to PICMG Standards**

AdvancedTCA®

PICMG® 3.8
Draft RC1.0 for Revision 1.0

AdvancedTCA Rear Transition Module Zone 3A

26 July 2011

PICMG®
Open Modular
Computing Specifications

MicroTCA™

PICMG® Specification MTCA.4
R 1.0 Draft 0.9xi

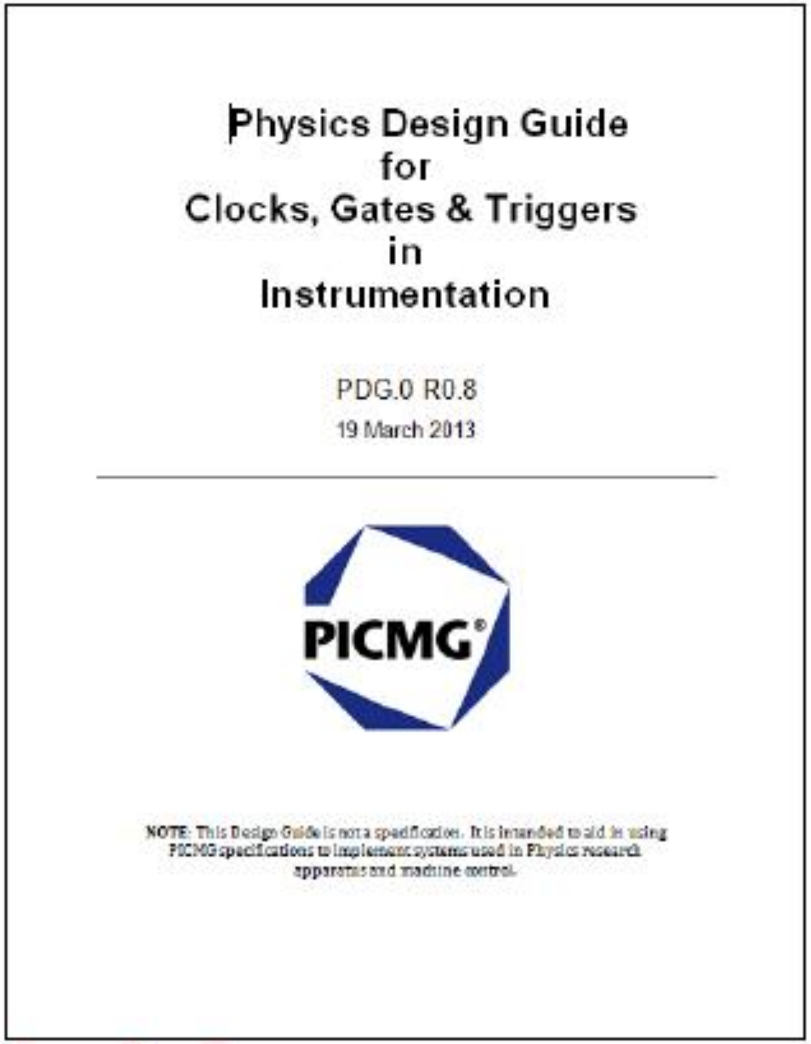
MicroTCA Enhancements for Rear I/O and Precision Timing

18 July 2011

PICMG®
Open Modular
Computing Specifications

μTCA®

xTCA Extn:
Physics Design Guide ATCA



Physics Design Guide
for
Clocks, Gates & Triggers
in
Instrumentation

PDG.0 R0.8

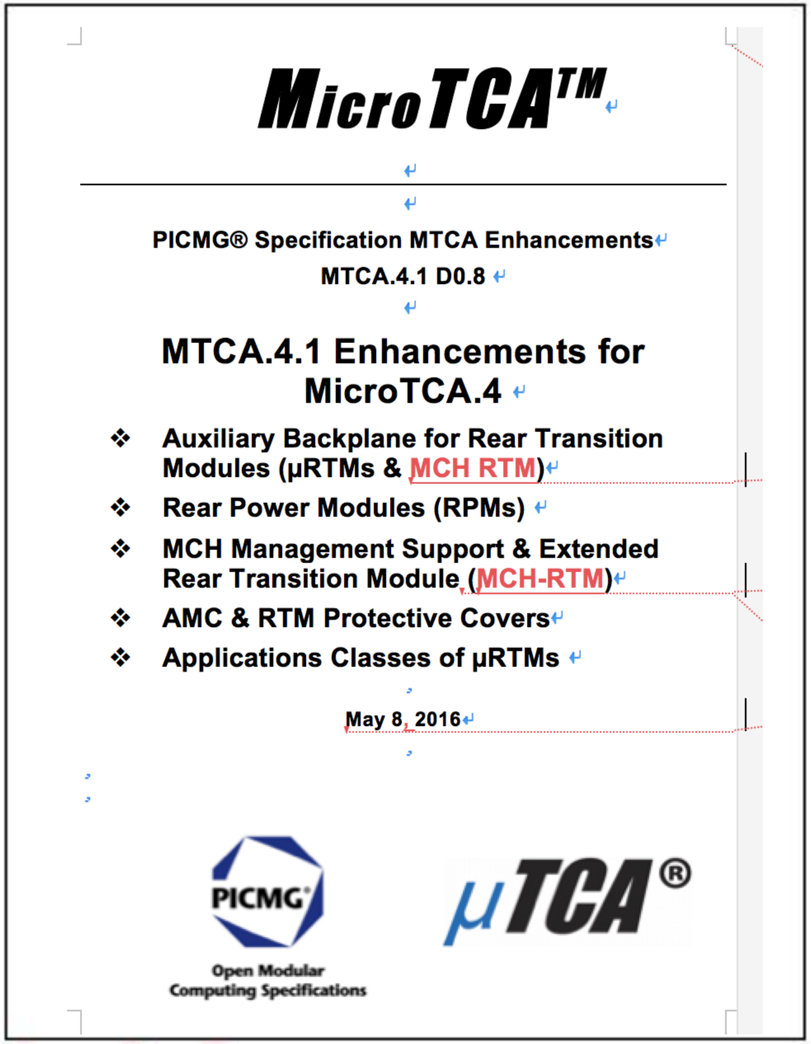
19 March 2013

PICMG®

NOTE: This Design Guide is not a specification. It is intended to aid in using PICMG specifications to implement systems used in Physics research apparatus and machine control.

xTCA further Extension:

MTCA.4.1 for RTM backplane



MicroTCA™

PICMG® Specification MTCA Enhancements

MTCA.4.1 D0.8

MTCA.4.1 Enhancements for MicroTCA.4

- Auxiliary Backplane for Rear Transition Modules (µRTMs & MCH RTM)
- Rear Power Modules (RPMs)
- MCH Management Support & Extended Rear Transition Module (MCH-RTM)
- AMC & RTM Protective Covers
- Applications Classes of µRTMs

May 8, 2016

PICMG

Open Modular Computing Specifications

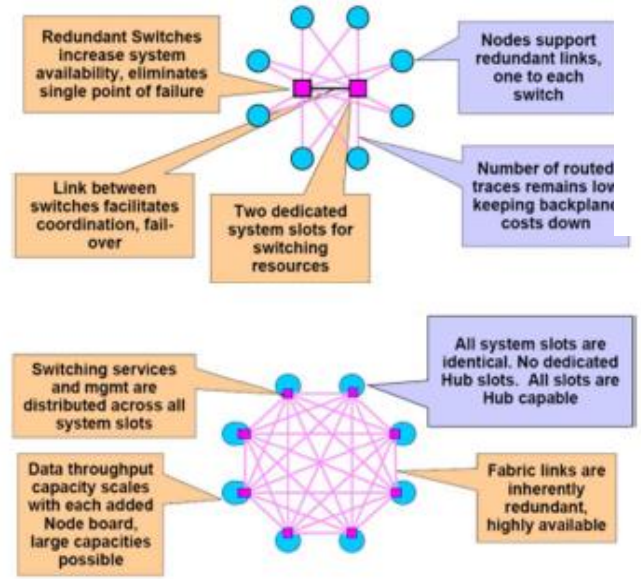
µTCA®

ATCA

ATCA Interfaces

Zone 2 Backplane Interfaces

- Base Interface
  - 10/100/1000 BASE-T Ethernet
  - Always Dual Star topology
- Fabric Interface
  - Star topology
  - Mesh topology
- Clock Interface
  - Three dedicated clock interfaces
- Update Channel
  - Direct connection between two slots



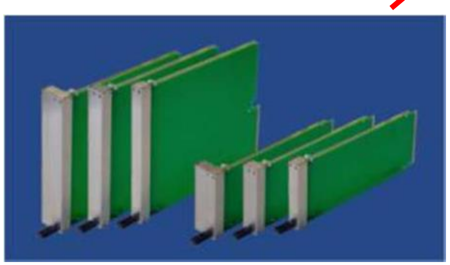
Point to Point
Link speed: 10Gbps

AMC/ATCA/MTCA.0

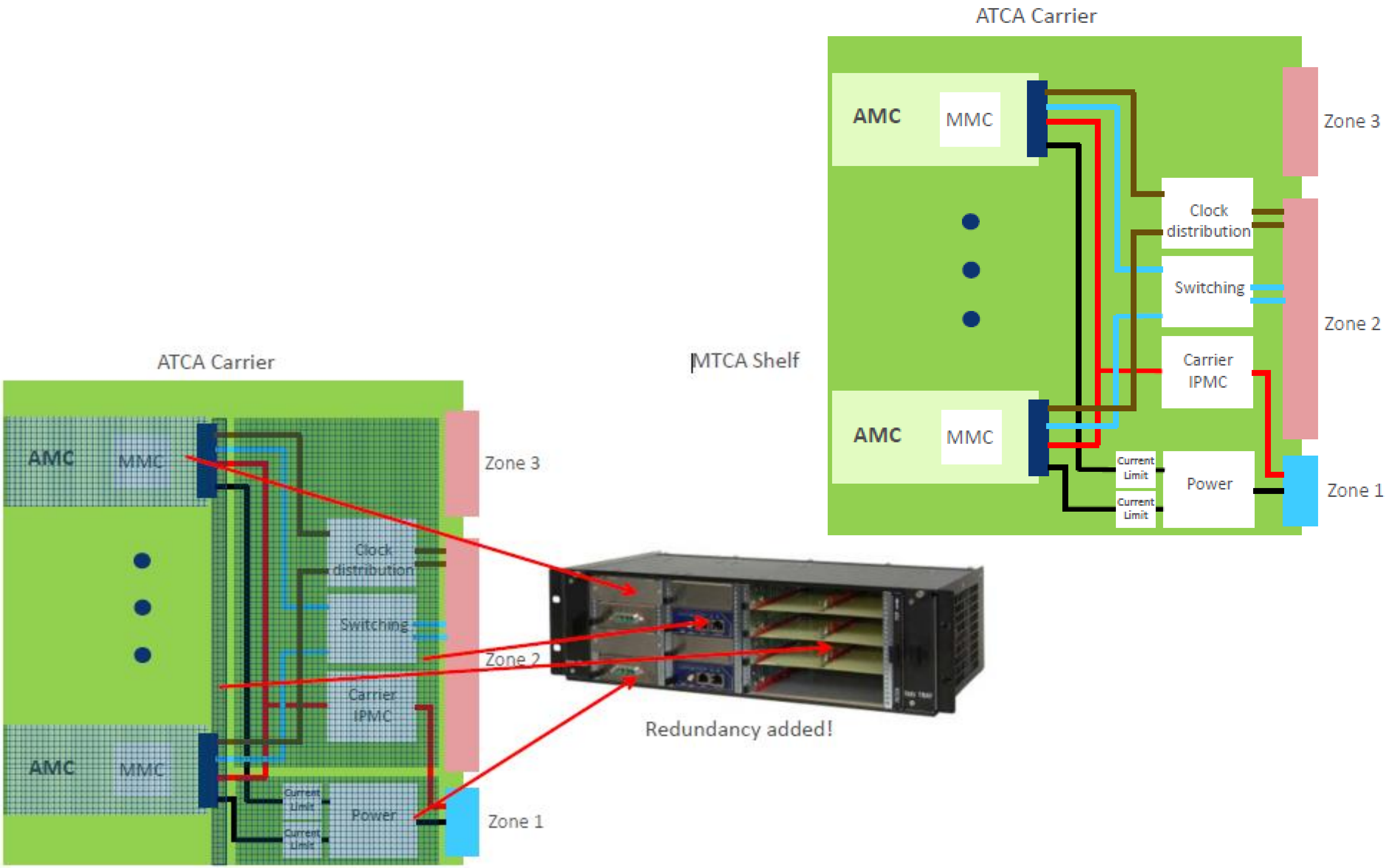
- AMC: Advanced Mezzanine Card
  - Initially developed as function extension for ATCA Boards
  - Fully integrated into the ATCA IPMI management structure
- Plugged into a so called ATCA Carrier
- Hot Swap capability

MTCA

ATCA

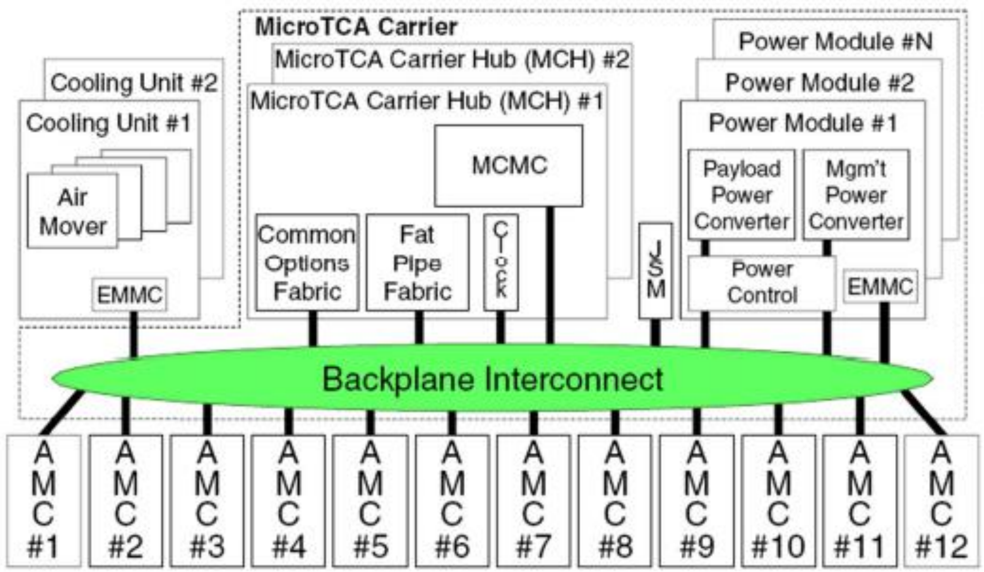


ATCA Carrier/MTCA.0



MTCA.0

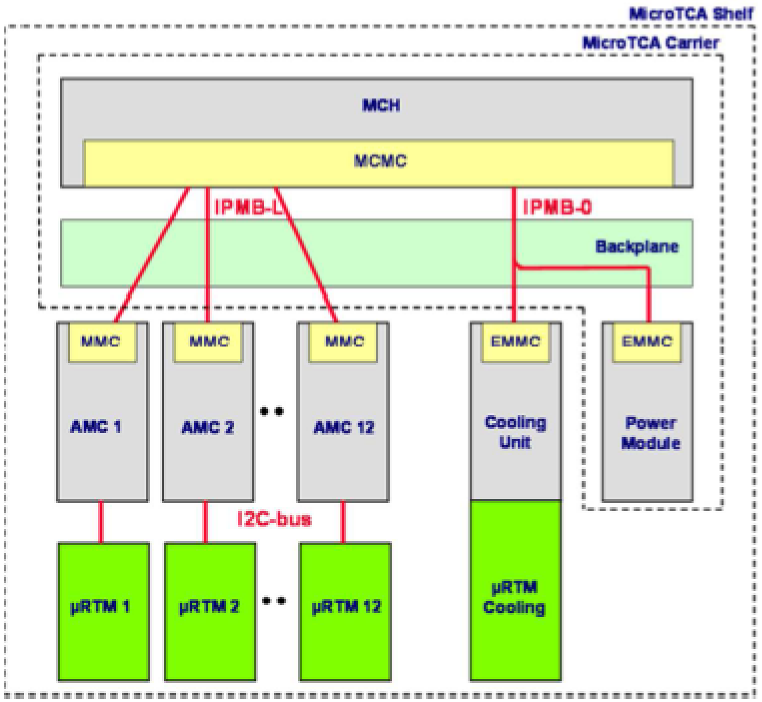
MicroTCA block diagram



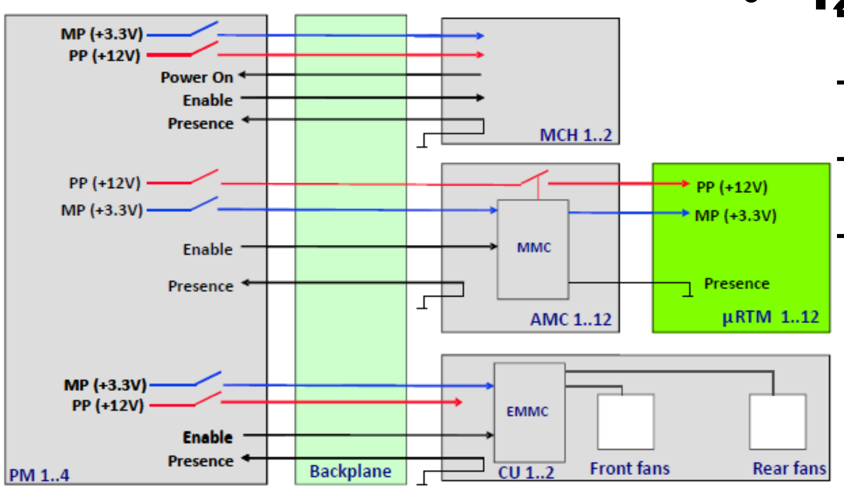
Terms and Acronyms

- **MCH** MicroTCA Carrier Hub
  - This is the complete module you can buy from a vendor
- **MCMC** MicroTCA Carrier Management Controller
  - This is the physical IPMI controller on the MCH
- **MMC** Module Management Controller
  - This is the physical IPMI controller on an AMC
- **EMMC** Enhanced MicroTCA Carrier Management Controller
  - This is the physical IPMI controller on a Cooling Unit and on Power Module
- **IPMB-0** Intelligent Platform Management Bus 0
  - Logical IPMB, physically divided into redundant IPMB-A and IPMB-B
- **IPMB-L** IPMB-Local
  - IPMI link between MCH and AMCs

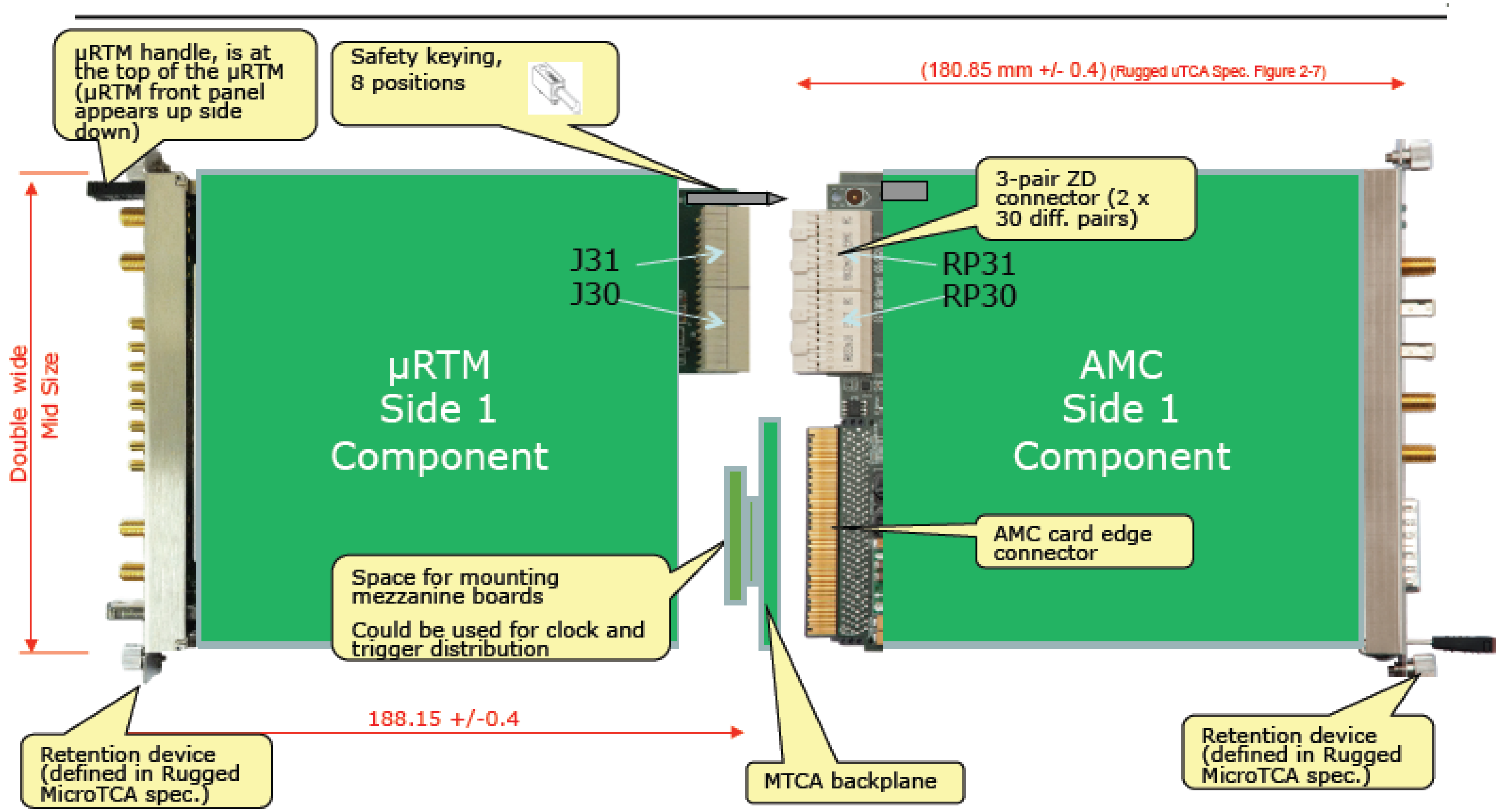
Management extensions in MTCA.4



- **IPMB-L**
  - Connects the MCMC on the MCH to the MMC on the AMC Modules
  - Radial architecture
- **IPMB-0**
  - Connects the MCMC on the MCH to the EMMC on the PM and CU
  - Bused architecture
- **I2C-Bus**
  - Connects the AMC to the µRTM
  - The µRTM is treated as managed
  - FRU of the AMC



MTCA.4 (xTCA for Physics) AMC and uRTM



Summary

- Signal Levels and BUS standards are important in Physics Instrumentation.
- xTCA introduction with PICMG 3.8, MTCA.4, PDG.0 MTCA.4.1 was introduced
- Standardization is not only in Physics Experiment, but anywhere with importance.

Feel free to ask questions !

contact : Zhenan.liu@cern.ch

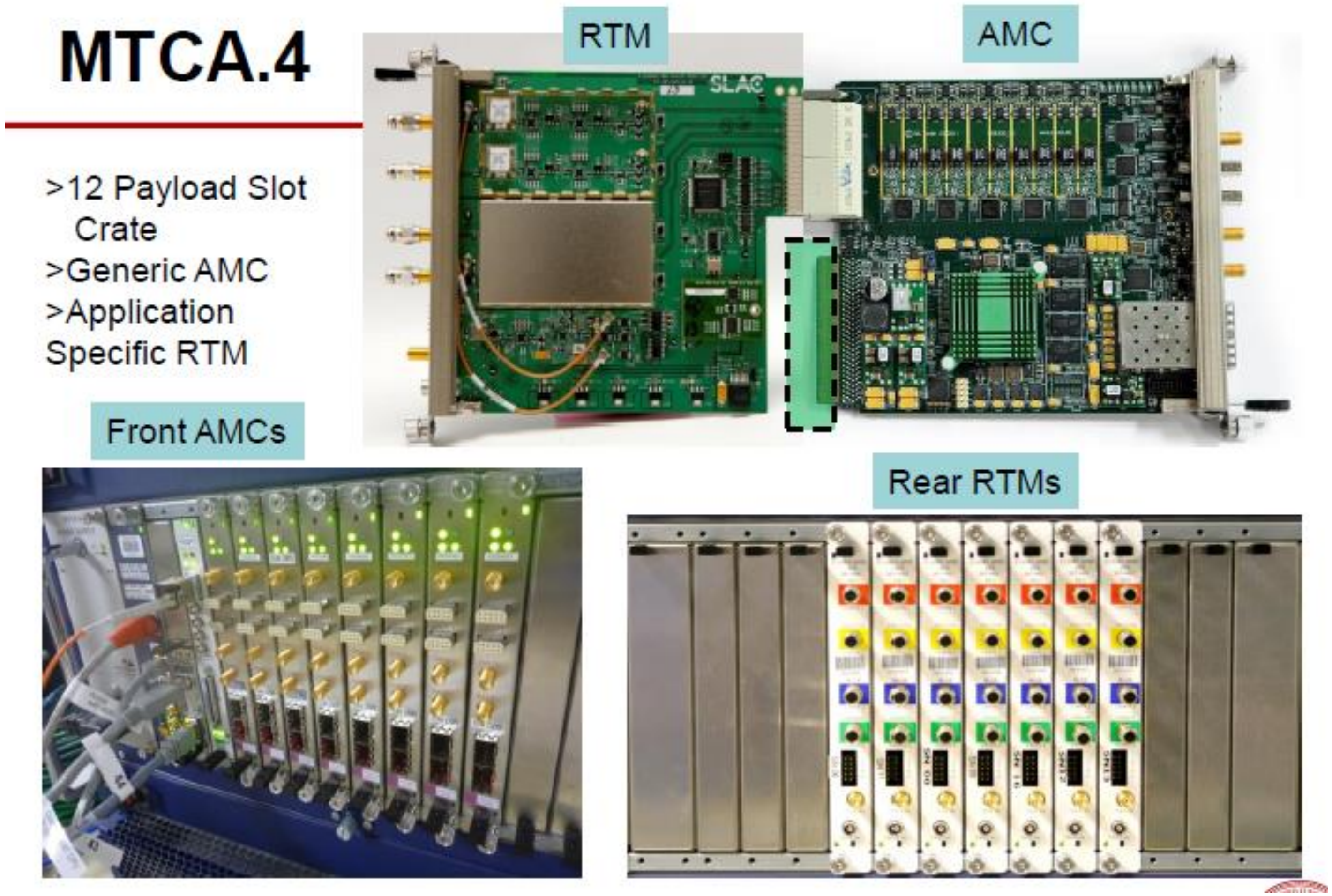
or

Liuza@ihep.ac.cn

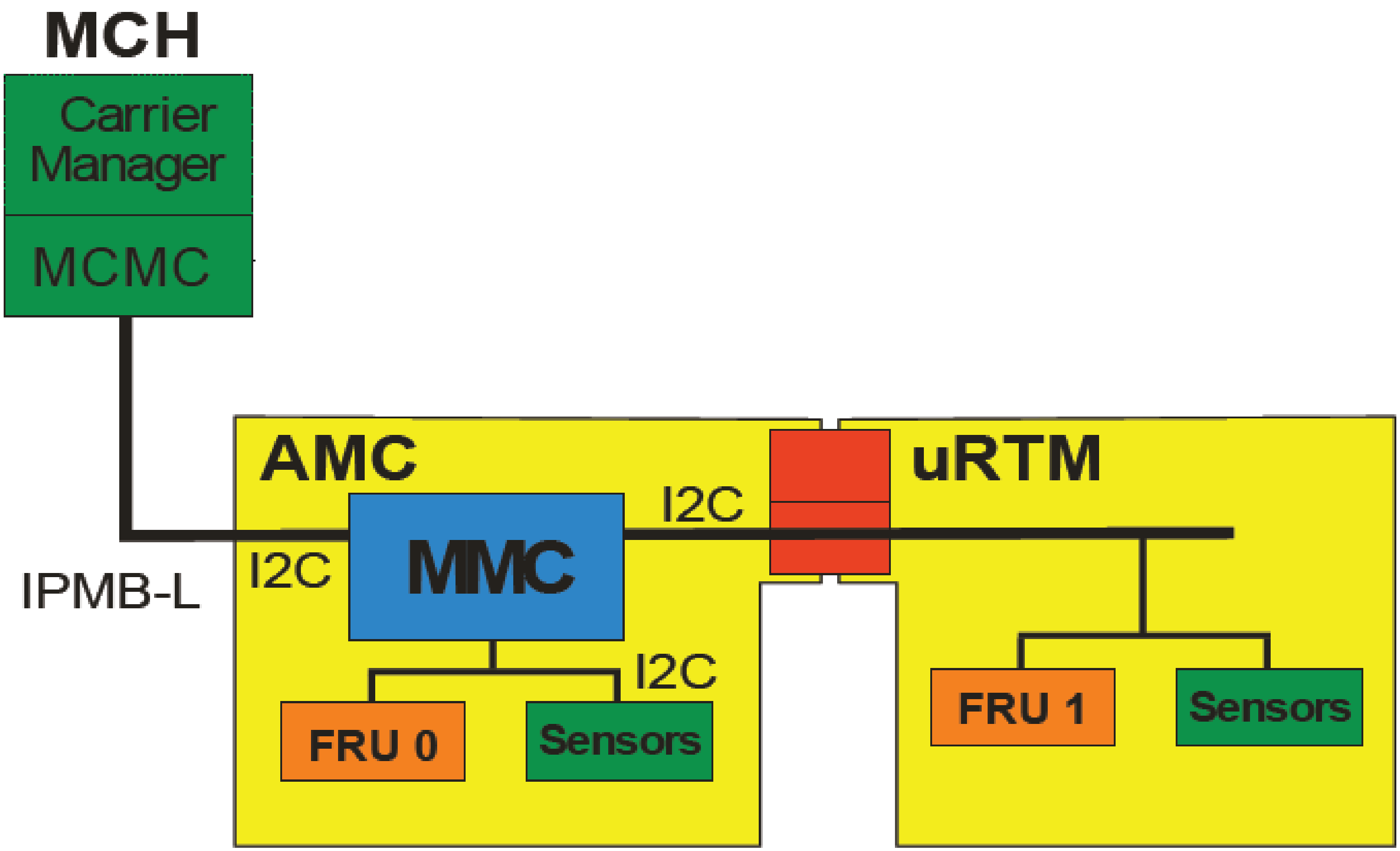
Backups

A lot progress in hardware development

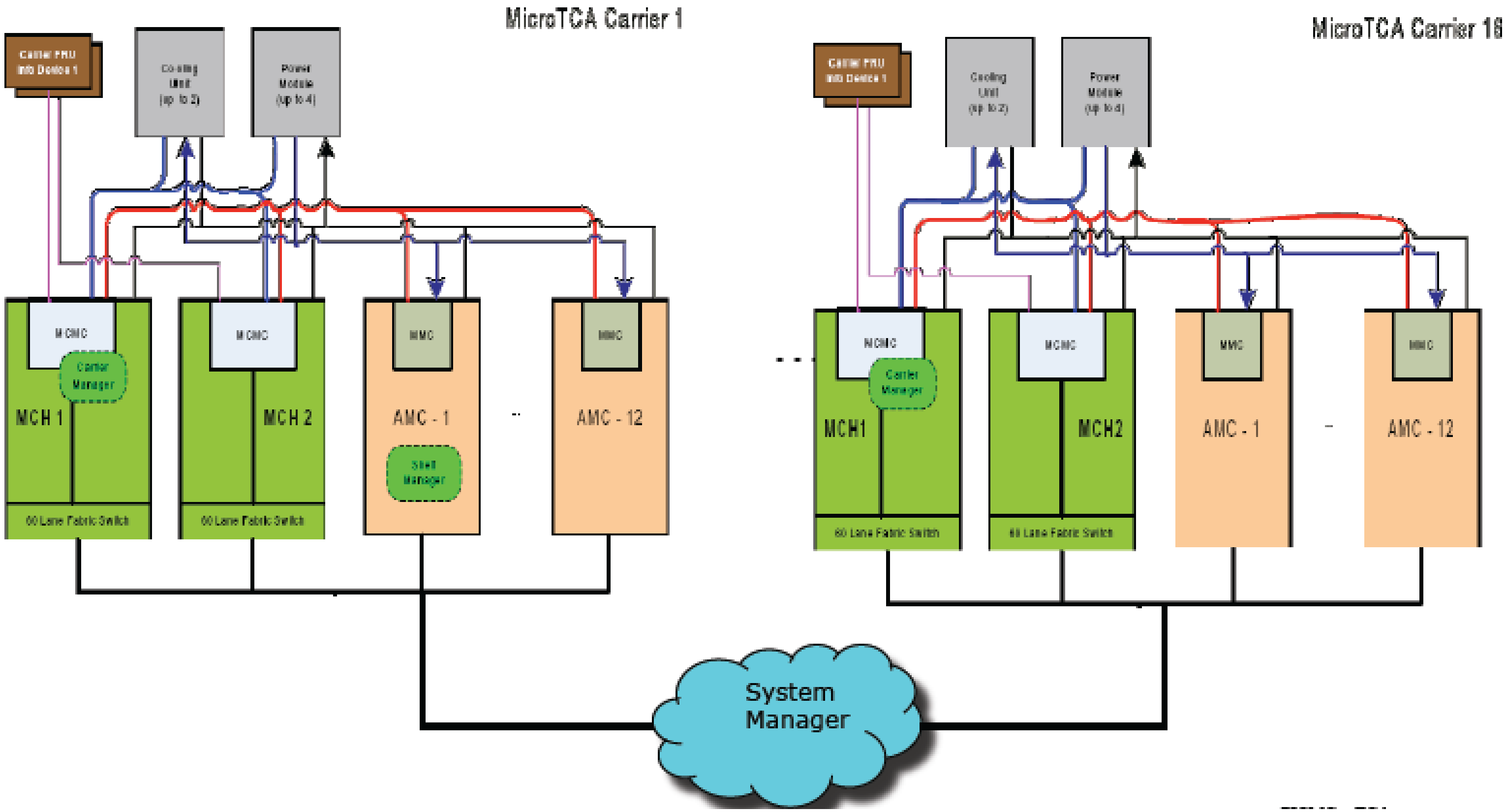
- At DESY,SLAC,IHEP (see later)



MTCA.4 – Hardware Management



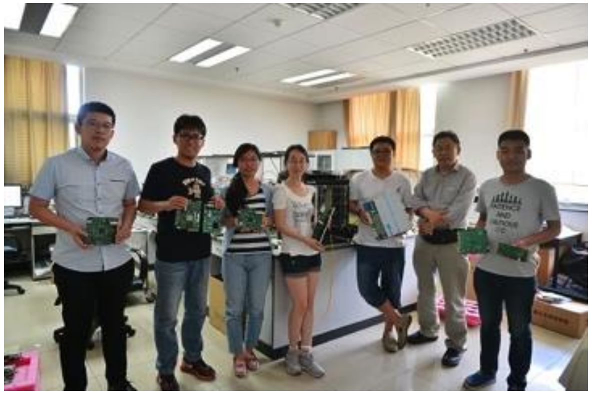
MCH Functionality:Management



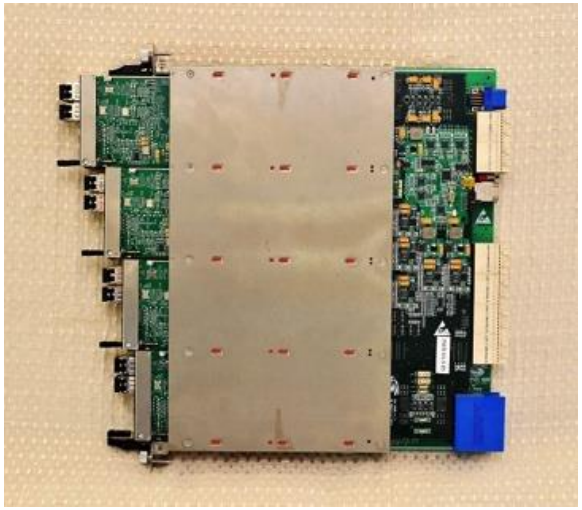
Examples at TrigLab/IHEP

- AMC/ATCA





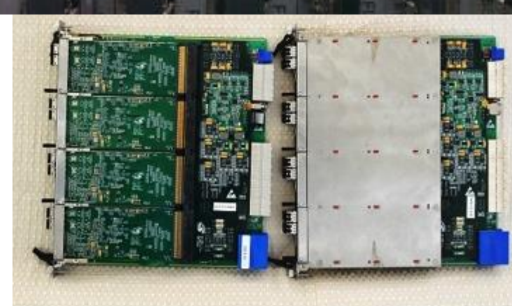
- for PANDA

Examples at TrigLab/IHEP

- BelleII/Belle2link

- BelleII/
  PXD/DAQ



Examples at TrigLab/IHEP

- CMS Trigger Upgrade
  - Inputs:
    - 10 Gbps/ch，36 Chs
  - Outputs:
    - 10Gbps，12 chs
  - Concentration,PreProcessing and Fanout