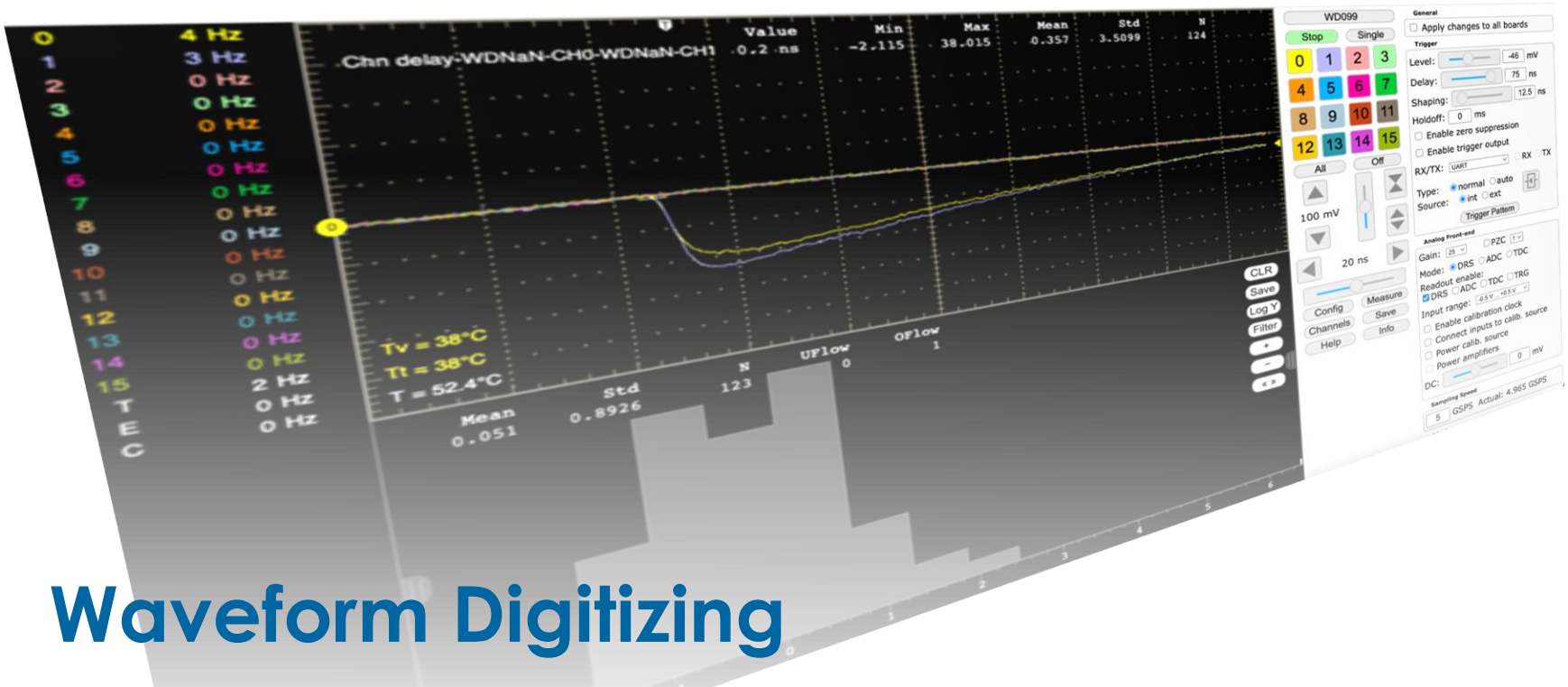



# Waveform Digitizing

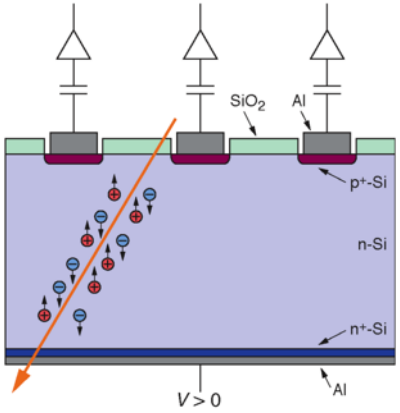
*Stefan Ritt, Paul Scherrer Institute, Switzerland*

*IEEE NPSS Workshop on Applicatioins of Radiation Instrumentation*

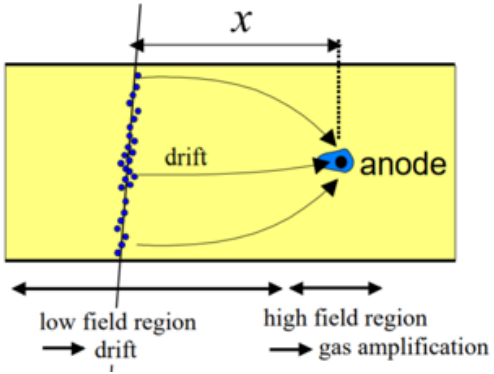
*Nov. 25th, 2022, Dakar, Senegal*

# 2 Principles of Detection of Ionizing Radiation

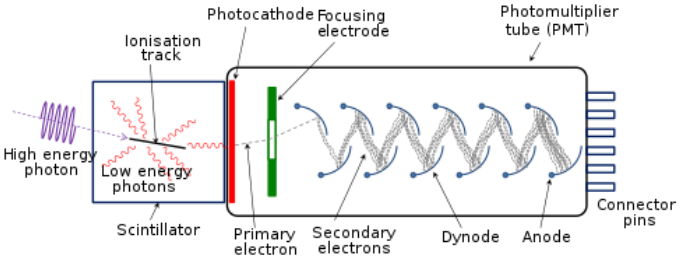
1. Detectors convert **property** to be measured directly into **electrical signal** → **position, time**
2. **Indirect** via light generation in scintillator → **energy, time**




Silicon detector

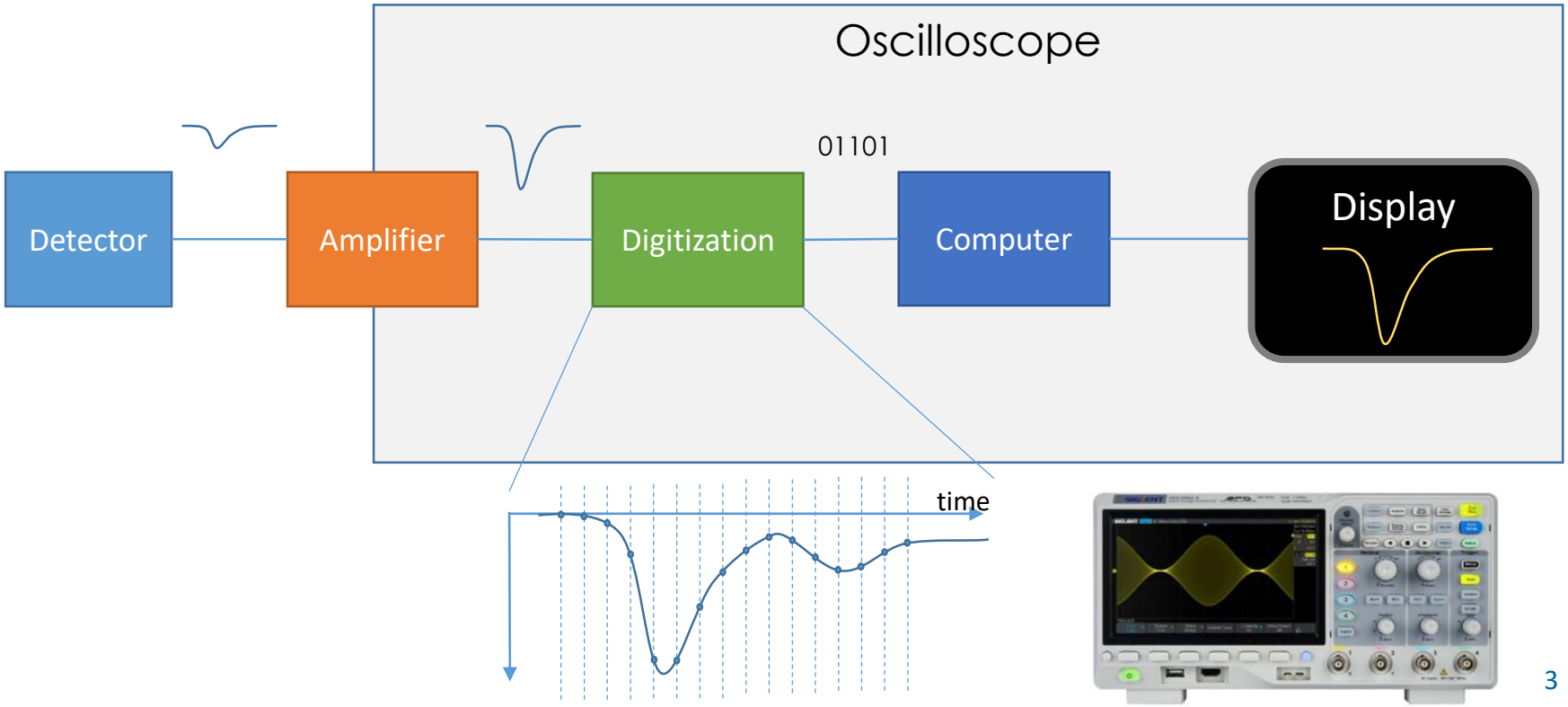



Wire chamber




Photomultiplier

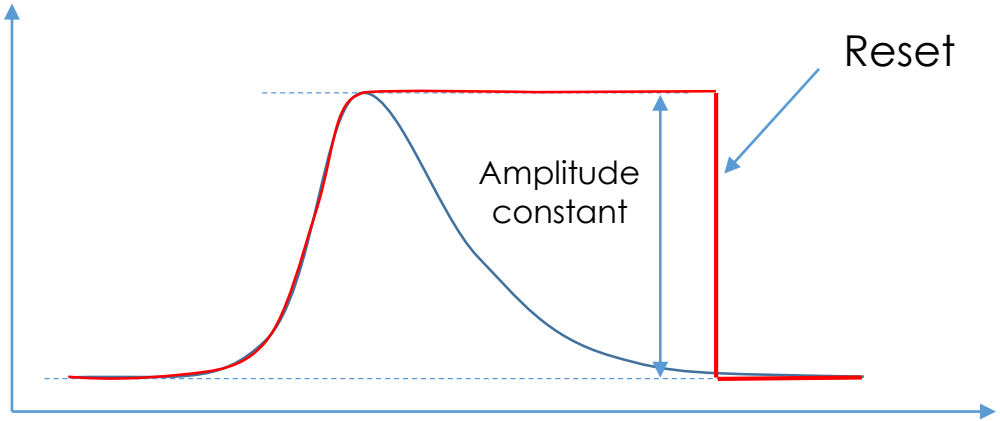
# Modern Digital Oscilloscopes



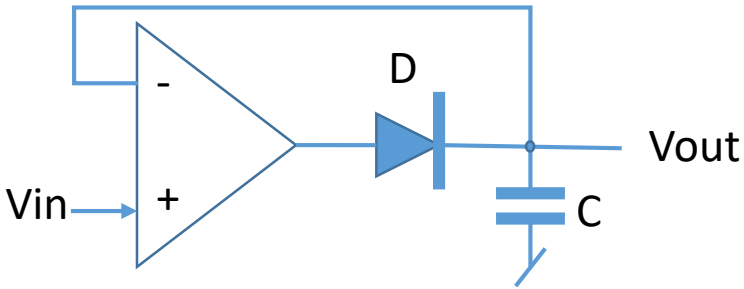
# Analog-to-Digital Conversion

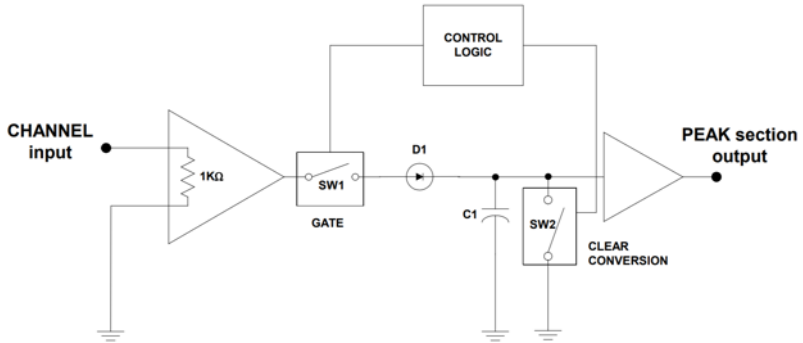
*ADCs & More*

# Digitization: Peak-sensing ADC

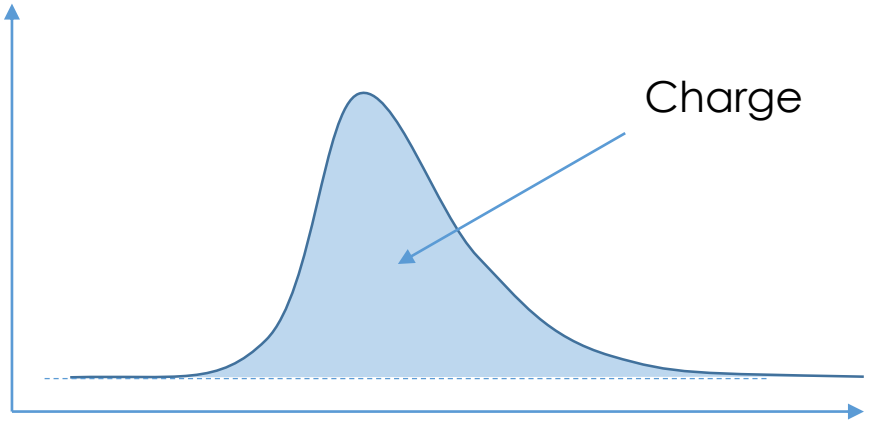


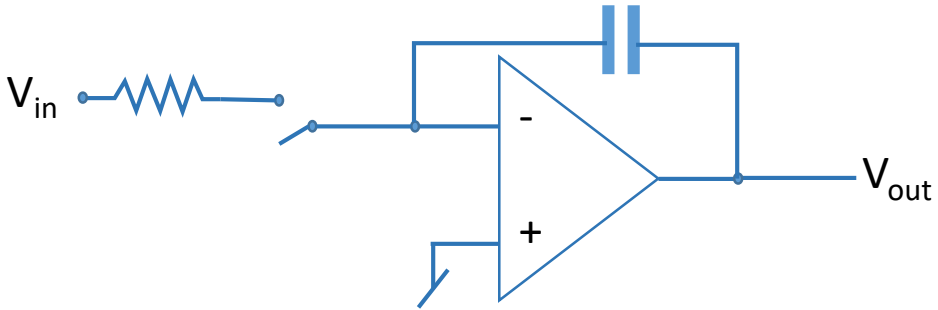

- Technique to digitize **fast** signals with **slow** ADCs
- Needs **reset** after each signal
- Mainly **historical**



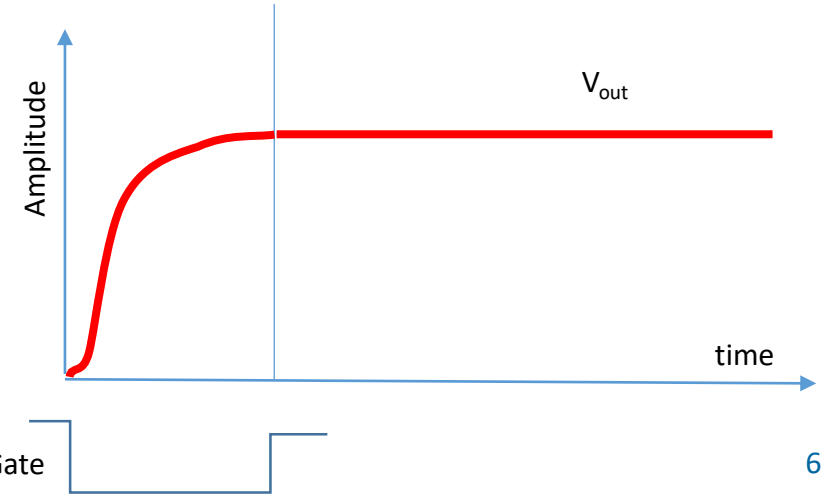



# Digitization: Charge integration



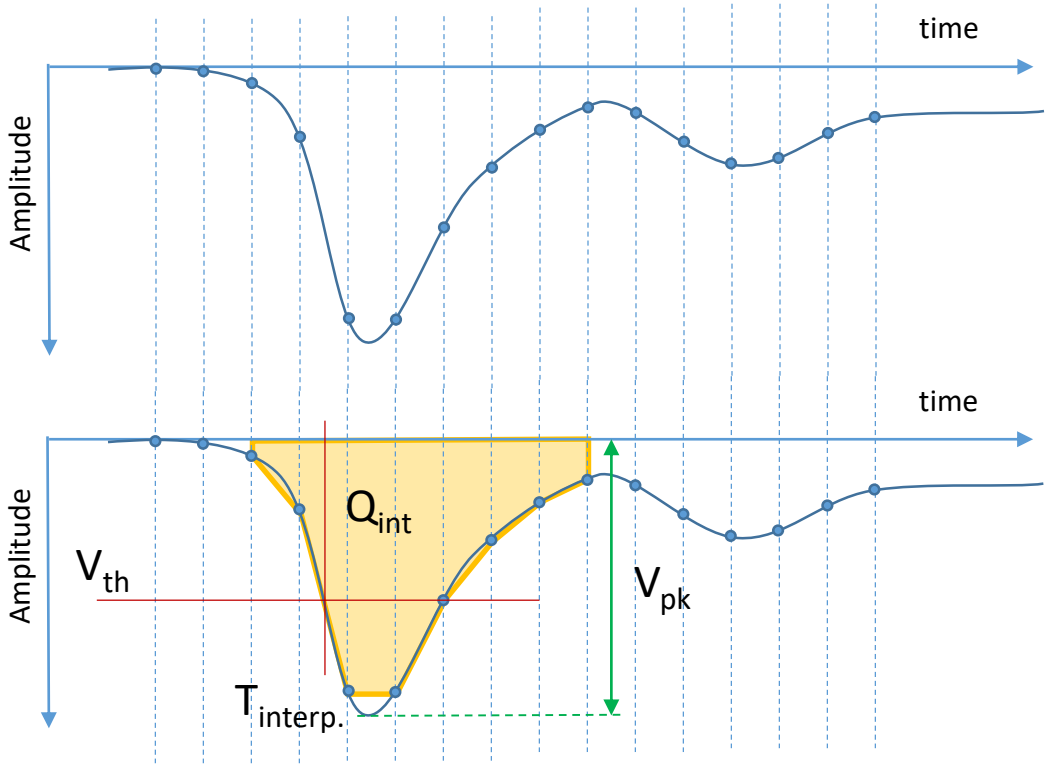




- Many detectors have a **proportionality** between **charge** and particle **energy**
- Noise **immunity**



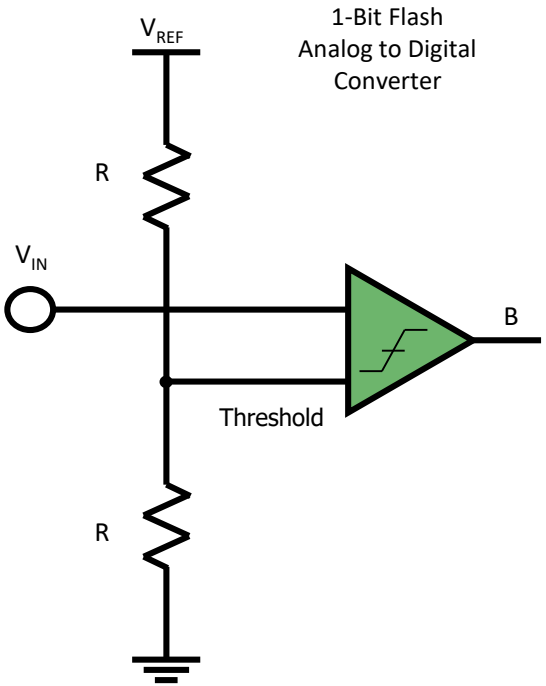
# Digitization: Waveform sampling

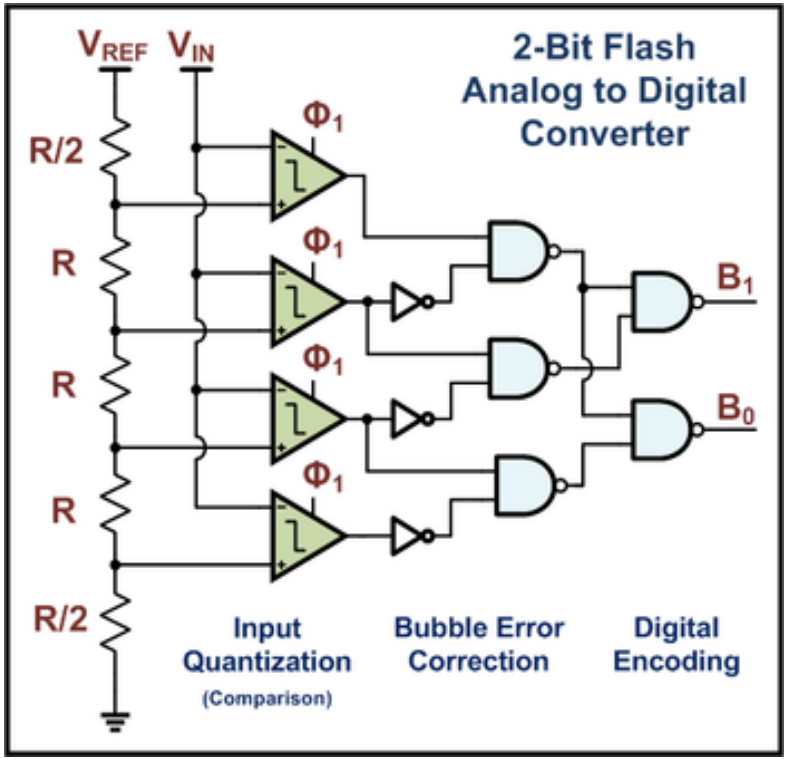
Sample waveform at discrete points (sampling rate) and extract features in digital world




| ADC Type | Resolution (bits) | Conversion rate |
|---|---|---|
| Dual Slope | 12-20 | 100 sample/s |
| Successive approximation | 8-18 | 10 Msample/s |
| Flash | 4-12 | 10 Gsample/s |
| Pipeline | 8-16 | 1 Gsample/s |
| Delta-sigma | 8-32 | 1 Msample/s |

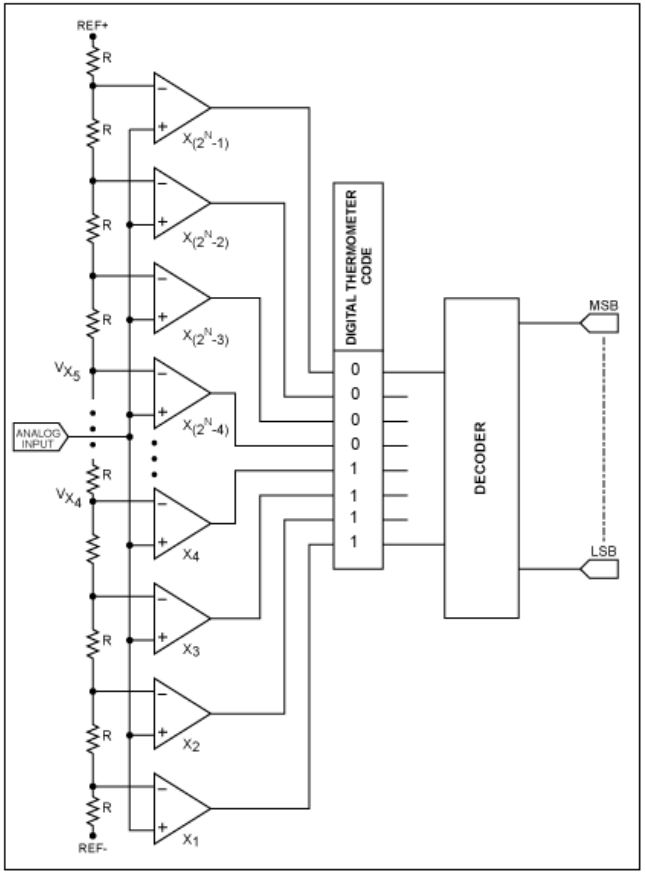
# Digitization: Flash ADC 1-bit and 2-bit



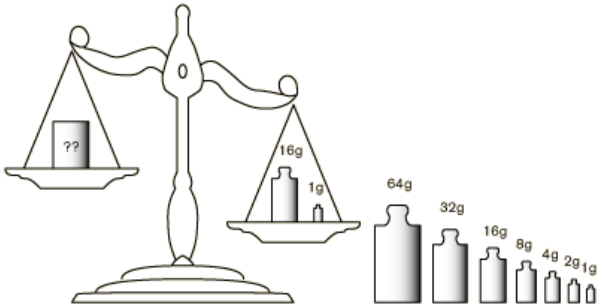



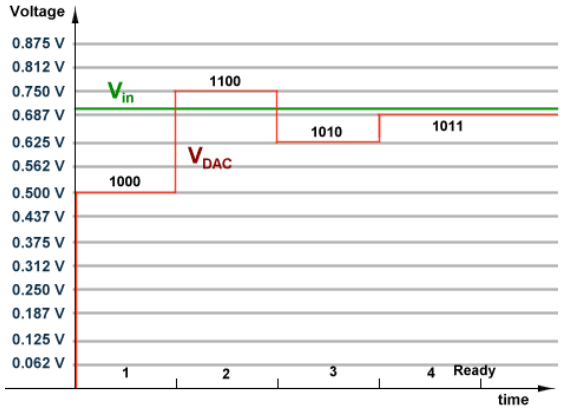
# Digitization: Flash ADC n-bit

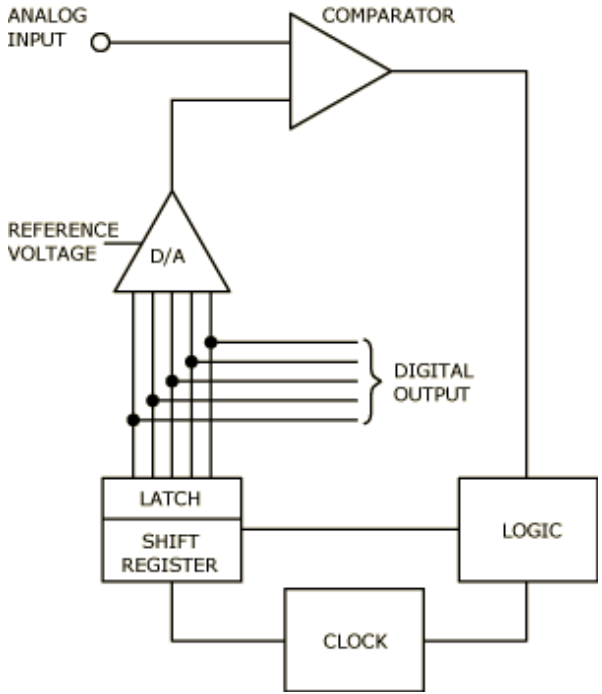
- Flash ADC very **fast**
- Requires **$2^n$** comparators
- Typically **<=8 bit** resolution



# Digitization: Successive approximation ADC

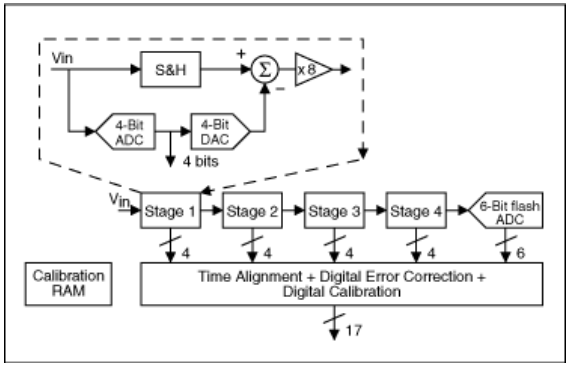


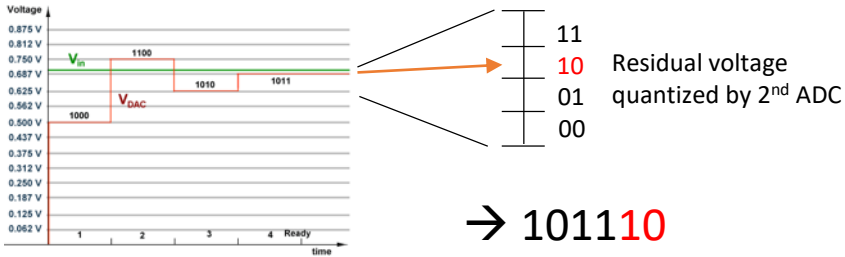



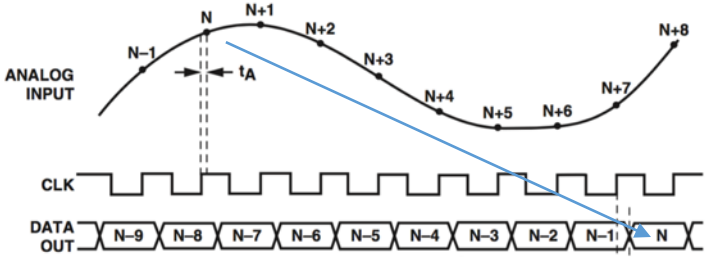
# Digitization: Pipeline ADC

- Combine **several flash ADCs** with successive approximation logic
- Only requires **4-Bit** flash ADC
- Can convert **one sample** in each **clock cycle**
- Has a **latency** depending on the number of pipeline stages
- Most common technology for fast ADCs b)




→ 101110



# ADC Datasheets

ANALOG DEVICES

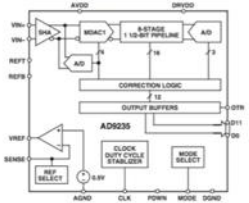
## 12-Bit, 20/40/65 MSPS 3 V A/D Converter

## AD9235

**FEATURES**
- Single 3 V Supply Operation (2.7 V to 3.6 V)
- SNR = 70 dBc to Nyquist at 65 MSPS
- SFDR = 85 dBc to Nyquist at 65 MSPS
- Low Power: 300 mW at 65 MSPS
- Differential Input with 500 MHz Bandwidth
- On-Chip Reference and SHA
- DNL = ±0.4 LSB
- Flexible Analog Input: 1 V p-p to 2 V p-p Range
- Offset Binary or Twos Complement Data Format
- Clock Duty Cycle Stabilizer

**APPLICATIONS**
- Ultrasound Equipment
- IF Sampling in Communications Receivers: IS-95, CDMA-One, IMT-2000
- Battery-Powered Instruments
- Hand-Held Scopemeters
- Low Cost Digital Oscilloscopes

**FUNCTIONAL BLOCK DIAGRAM**




**PRODUCT DESCRIPTION**

The AD9235 is a family of monolithic, single 3 V supply, 12-bit, 20/40/65 MSPS analog-to-digital converters. This family features a high performance sample-and-hold amplifier (SHA) and voltage reference. The AD9235 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 20/40/65 MSPS data rates and guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available analog-to-digital converters, the AD9235 is suitable for applications in communications, imaging, and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in straight binary or twos complement formats. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9235 is available in a 28-lead thin shrink small outline package (TSSOP) and a 32-lead chip scale package (LFCSP) and is specified over the industrial temperature range (–40°C to +85°C).

**PRODUCT HIGHLIGHTS**

1. The AD9235 operates from a single 3 V power supply and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
2. Operating at 65 MSPS, the AD9235 consumes a low 300 mW.
3. The patented SHA input maintains excellent performance for input frequencies up to 100 MHz and can be configured for single-ended or differential operation.
4. The AD9235 pinout is similar to the AD9214-65, a 10-bit, 65 MSPS ADC. This allows a simplified upgrade path from 10 bits to 12 bits for 65 MSPS systems.
5. The clock DCS maintains overall ADC performance over a wide range of clock pulsewidths.
6. The OTR output bit indicates when the signal is beyond the selected input range.

REV. B



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703 

## AD9235–SPECIFICATIONS

**DC SPECIFICATIONS** (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, 2 V p-p Differential Input, 1.0 V internal reference, $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

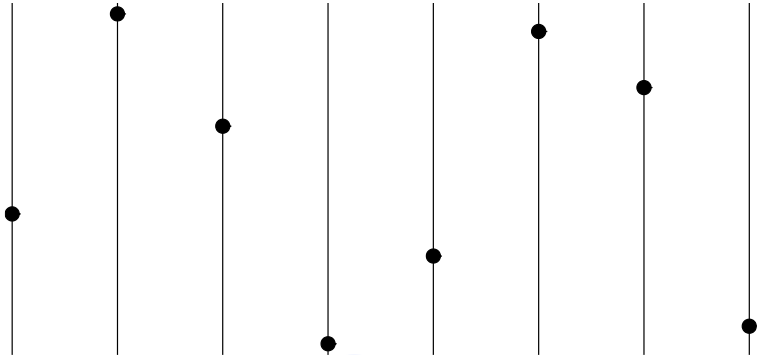
| Parameter | Temp | Test Level | AD9235BRU-20 Min | Typ | Max | AD9235BRU-40 Min | Typ | Max | AD9235BRU/BCP-65 Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESOLUTION | Full | VI | 12 | | | 12 | | | 12 | | | Bits |
| ACCURACY | | | | | | | | | | | | |
| No Missing Codes Guaranteed | Full | VI | 12 | | | 12 | | | 12 | | | Bits |
| Offset Error | Full | VI | | ±0.30 | ±1.20 | | ±0.50 | ±1.20 | | ±0.50 | ±1.20 | % FSR |
| Gain Error[1] | Full | VI | | ±0.30 | ±2.40 | | ±0.50 | ±2.50 | | ±0.50 | ±2.60 | % FSR |
| Differential Nonlinearity (DNL)[2] | Full | IV | | ±0.35 | ±0.65 | | ±0.35 | ±0.75 | | ±0.40 | ±0.80 | LSB |
| | 25°C | I | | ±0.35 | | | ±0.35 | | | ±0.35 | | LSB |
| Integral Nonlinearity (INL)[2] | Full | IV | | ±0.45 | ±0.80 | | ±0.50 | ±0.90 | | ±0.70 | ±1.30 | LSB |
| | 25°C | I | | ±0.40 | | | ±0.40 | | | ±0.45 | | LSB |
| TEMPERATURE DRIFT | | | | | | | | | | | | |
| Offset Error | Full | V | | ±2 | | | ±2 | | | ±3 | | ppm/°C |
| Gain Error[1] | Full | V | | ±12 | | | ±12 | | | ±12 | | ppm/°C |
| INTERNAL VOLTAGE REFERENCE | | | | | | | | | | | | |
| Output Voltage Error (1 V Mode) | Full | VI | | ±5 | ±35 | | ±5 | ±35 | | ±5 | ±35 | mV |
| Load Regulation @ 1.0 mA | Full | V | | 0.8 | | | 0.8 | | | 0.8 | | mV |
| Output Voltage Error (0.5 V Mode) | Full | V | | ±2.5 | | | ±2.5 | | | ±2.5 | | mV |
| Load Regulation @ 0.5 mA | Full | V | | 0.1 | | | 0.1 | | | 0.1 | | mV |
| INPUT REFERRED NOISE | | | | | | | | | | | | |
| VREF = 0.5 V | 25°C | V | | 0.54 | | | 0.54 | | | 0.54 | | LSB rms |
| VREF = 1.0 V | 25°C | V | | 0.27 | | | 0.27 | | | 0.27 | | LSB rms |
| ANALOG INPUT | | | | | | | | | | | | |
| Input Span, VREF = 0.5 V | Full | IV | | 1 | | | 1 | | | 1 | | V p-p |
| Input Span, VREF = 1.0 V | Full | IV | | 2 | | | 2 | | | 2 | | V p-p |
| Input Capacitance[3] | Full | V | | 7 | | | 7 | | | 7 | | pF |
| REFERENCE INPUT | | | | | | | | | | | | |
| RESISTANCE | Full | V | | 7 | | | 7 | | | 7 | | kΩ |
| POWER SUPPLIES | | | | | | | | | | | | |
| Supply Voltages | | | | | | | | | | | | |
| AVDD | Full | IV | 2.7 | 3.0 | 3.6 | 2.7 | 3.0 | 3.6 | 2.7 | 3.0 | 3.6 | V |
| DRVDD | Full | IV | 2.25 | 3.0 | 3.6 | 2.25 | 3.0 | 3.6 | 2.25 | 3.0 | 3.6 | V |
| Supply Current | | | | | | | | | | | | |
| IAVDD[2] | Full | V | | 30 | | | 55 | | | 100 | | mA |
| IDRVDD[2] | Full | V | | 2 | | | 5 | | | 7 | | mA |
| PSRR | Full | V | | ±0.01 | | | ±0.01 | | | ±0.01 | | % FSR |
| POWER CONSUMPTION | | | | | | | | | | | | |
| DC Input[4] | Full | V | | 90 | | | 165 | | | 300 | | mW |
| Sine Wave Input[5] | Full | VI | | 95 | 110 | | 180 | 205 | | 320 | 350 | mW |
| Standby Power[5] | Full | V | | 1.0 | | | 1.0 | | | 1.0 | | mW |

NOTES
[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0 V external reference).
[2]Measured at maximum clock rate, $f_{IN}$ = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3]Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 2 for the equivalent analog input structure.
[4]Measured with dc input at maximum clock rate.
[5]Standby power is measured with a dc input, the CLK pin inactive (i.e., set to AVDD or AGND).

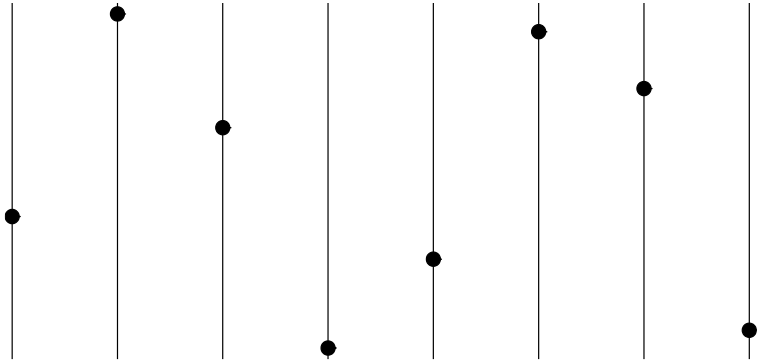
Specifications subject to change without notice.

# Nyquist-Shannon Sampling Theorem

$f_{signal} < f_{sampling}/2$



$f_{signal} > f_{sampling}/2$

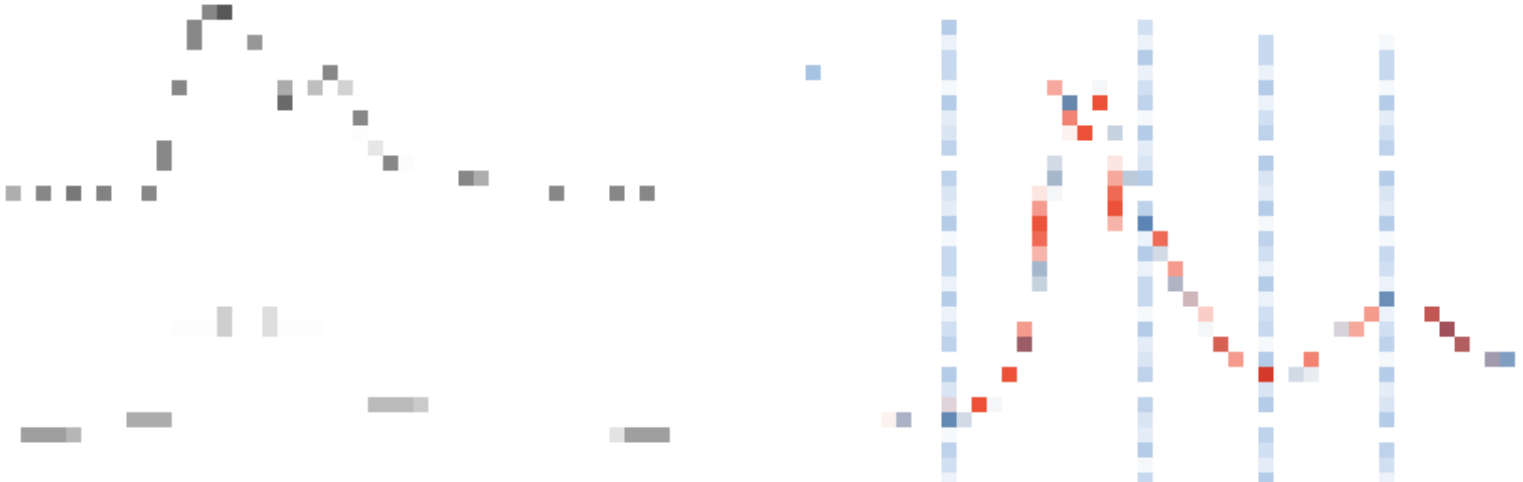


Only signals with frequencies below half the sampling frequency can be perfectly sampled.

Then the original signal can be recovered from the discrete sampling points.

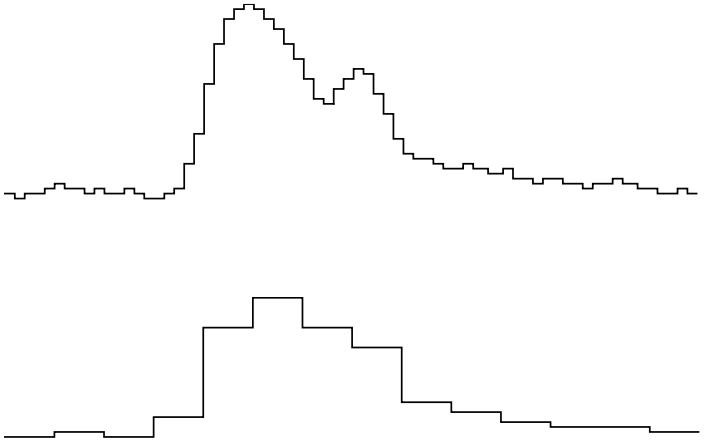
# [illegible]

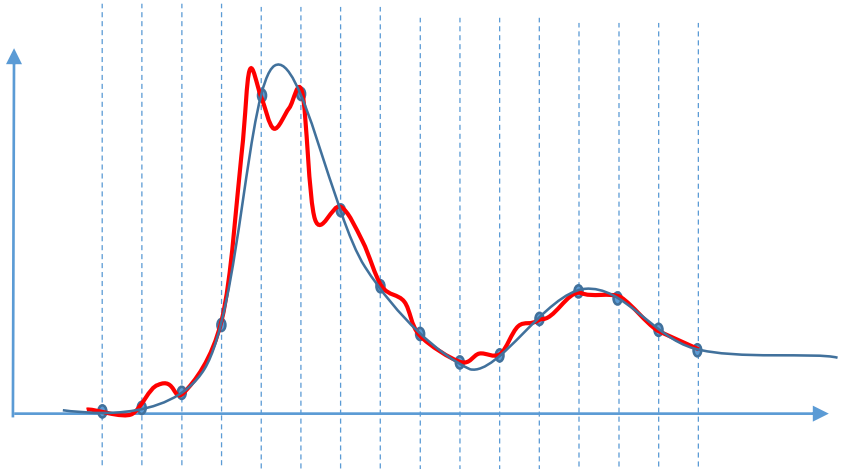
- [illegible]
- [illegible]
- [illegible]



# Limits of waveform digitizing

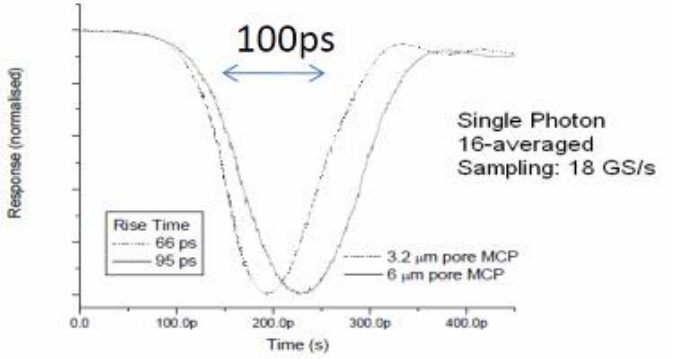
- **Aliasing** occurs if $f_{signal} > 0.5 * f_{sampling}$
- Features of the signal can be lost ("**pile-up**")
- Precise time measurement and good energy resolution need **very fast high resolution** ADCs



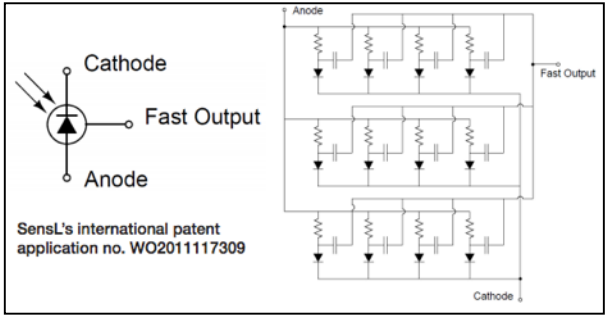


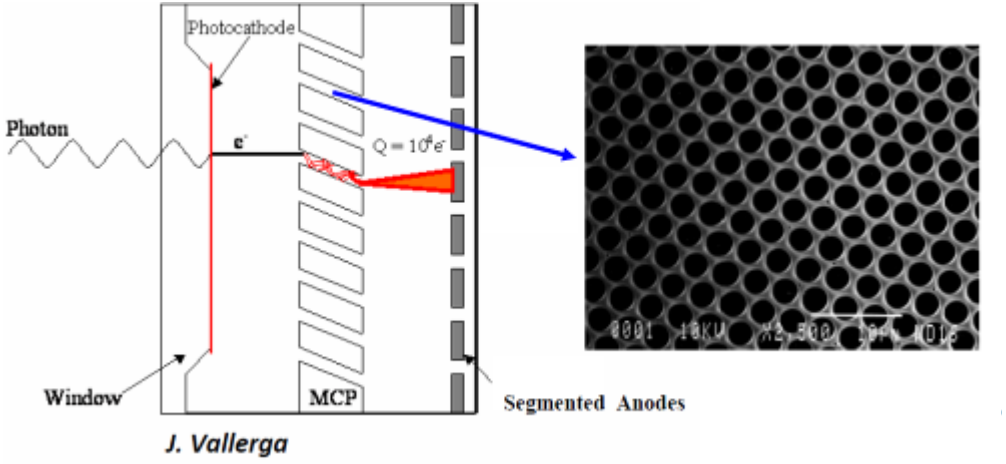
# What are the fastest detectors?

- Micro-Channel-Plates (MCP)
  - Photomultipliers with thousands of tiny channels (3-10 μm)
  - Typical gain of 10,000 per plate
  - Very fast rise time down to 70 ps
- 70 ps rise time → **4-5 GHz BW** → **10 GSPS**
- SiPMs (Silicon PMTs) are also getting < 100 ps



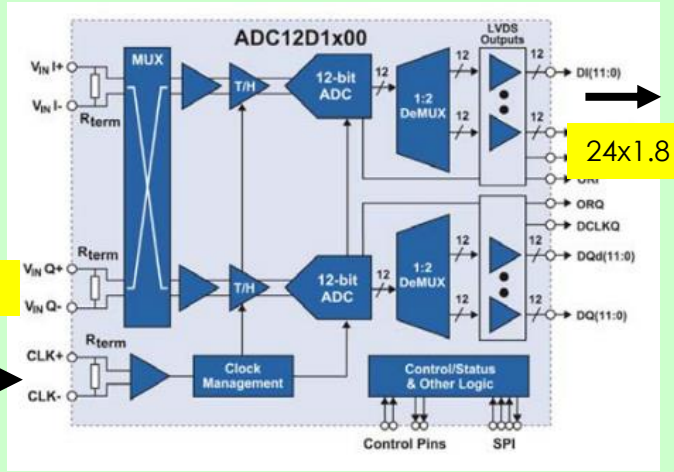

J. Milnes, J. Howoth, Photek



# Can it be done with FADCs?

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s




24x1.8 Gbits/s

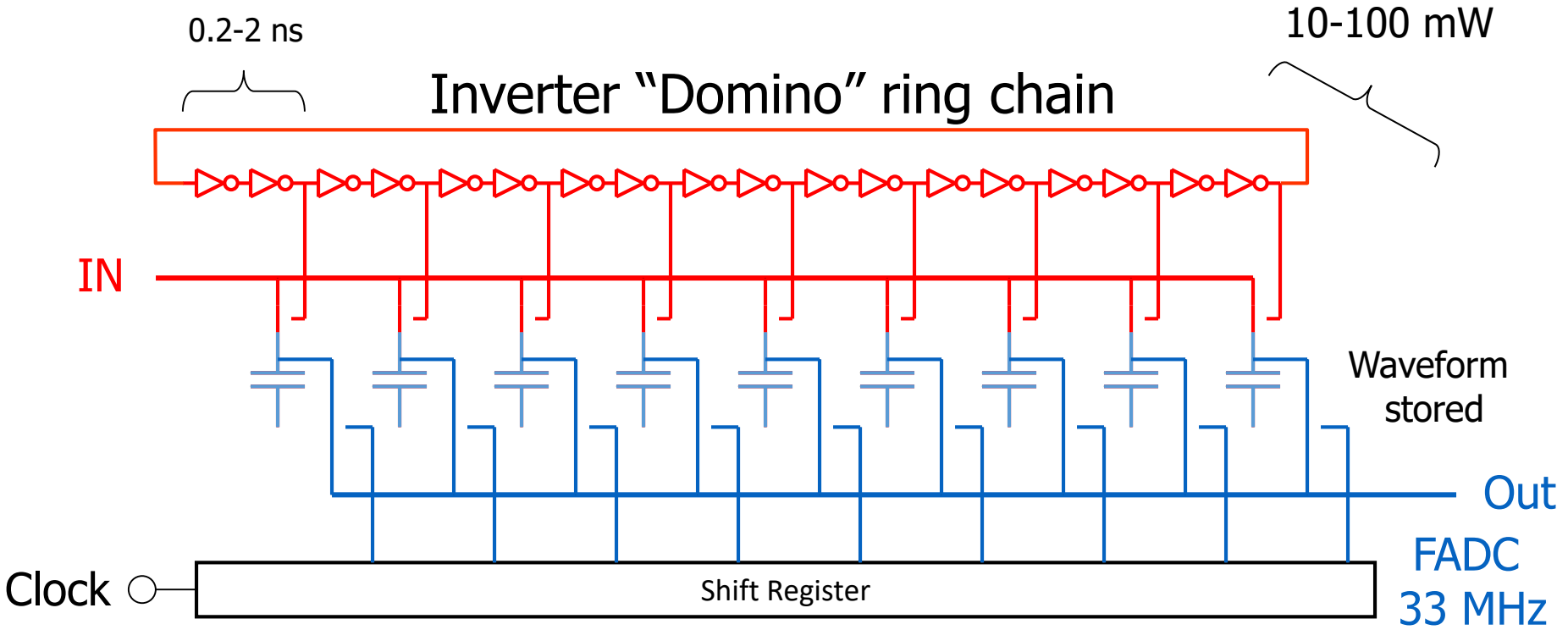
1.8 GHz!

- Requires high-end FPGA
- Complex board design
- High FPGA power

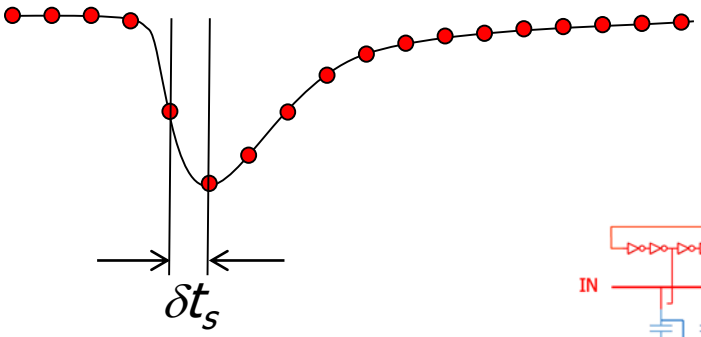
V1761: 2 Channels, 4 GS/s, 10 bits

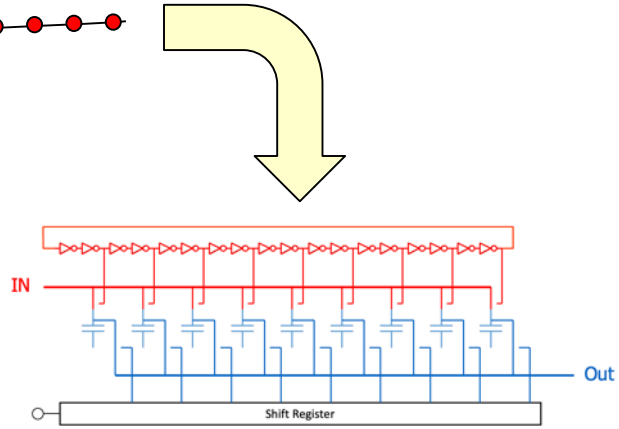
- Costs: 1-10 k$ / channel
- What about 1000+ channels?

# Digitization: Application Specific Integrated Circuit (ASIC) for Waveform Sampling: Switched Capacity Arrays (SCA)



# Time Stretch Ratio (TSR)



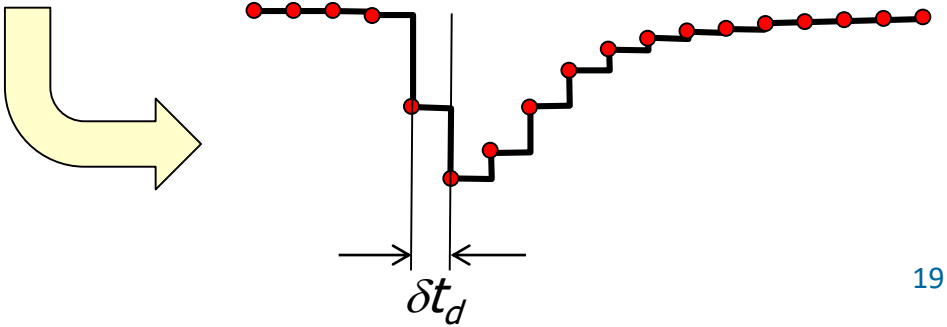

$$TSR \propto \frac{dt_s}{dt_d}$$

Typical values:

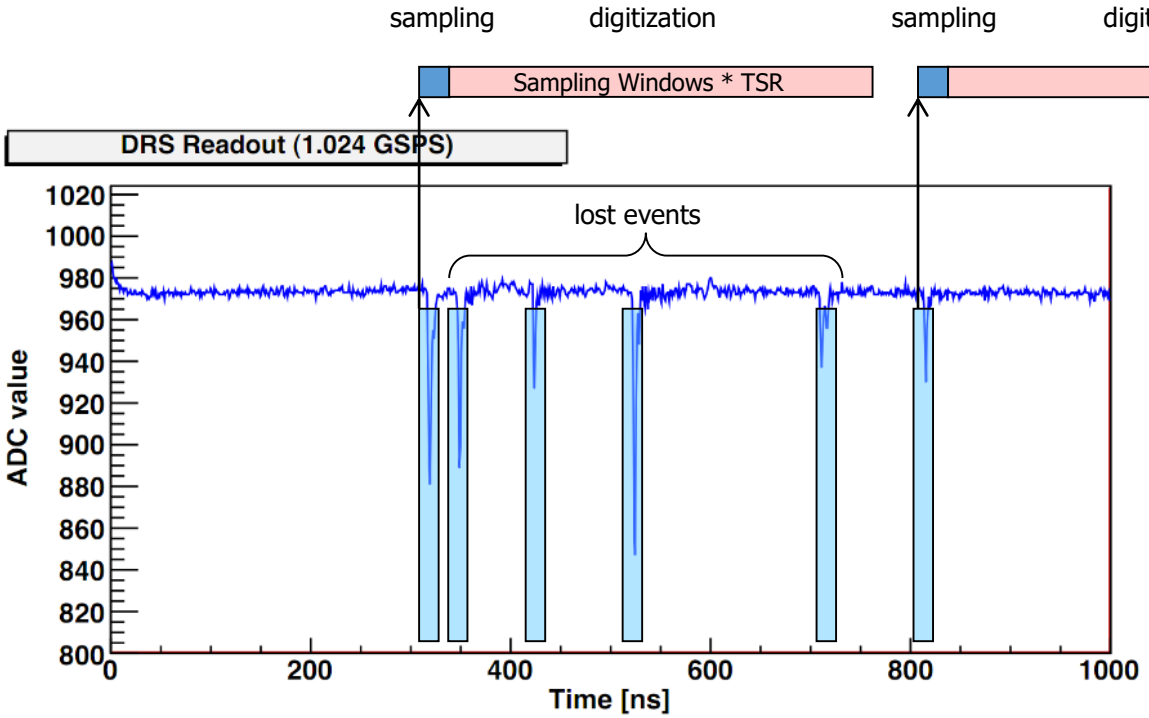
$\delta t_s$ = 0.5 ns (2 GSPS)

$\delta t_d$ = 30 ns (33 MHz)

→ TSR = 60

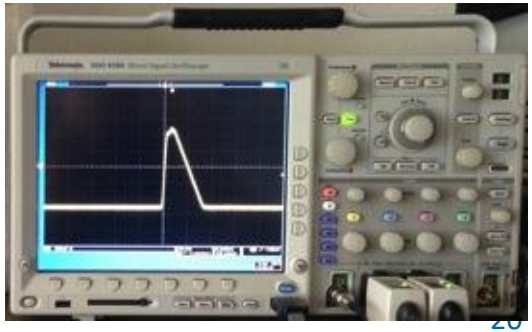


# Triggered Operation



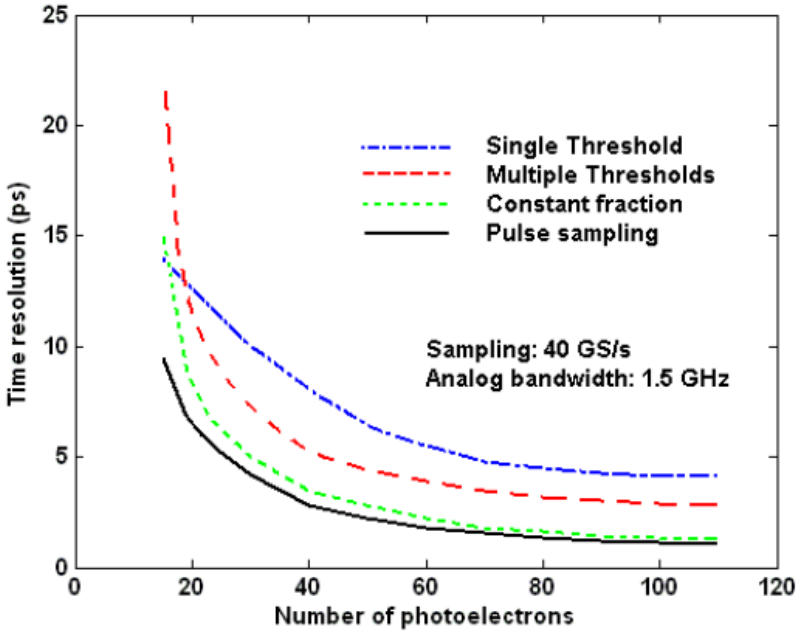

Dead time =
Sampling Window · *TSR*

(e.g. 100 ns · 60 = 6 μs)

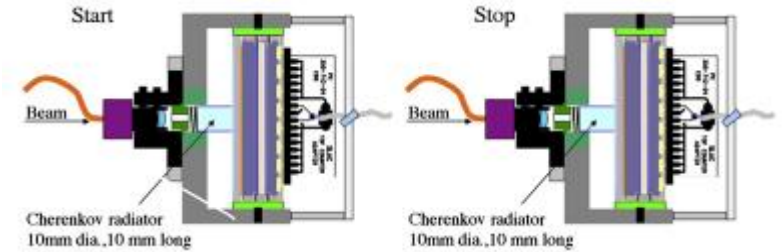


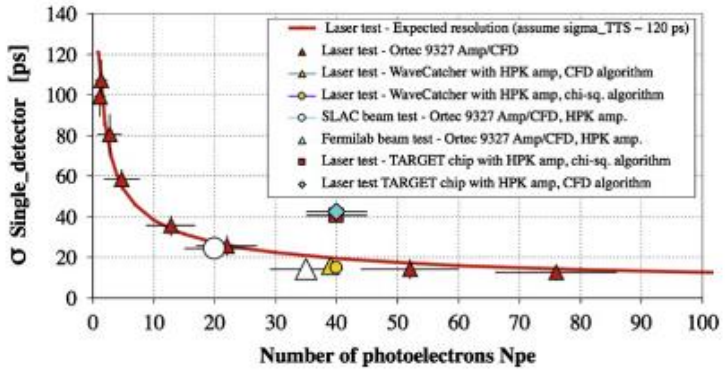
Chips usually cannot sample during readout ⇒ "**Dead Time**"
Technique only works for "**events**" and "**triggers**"

# How to measure timing best?



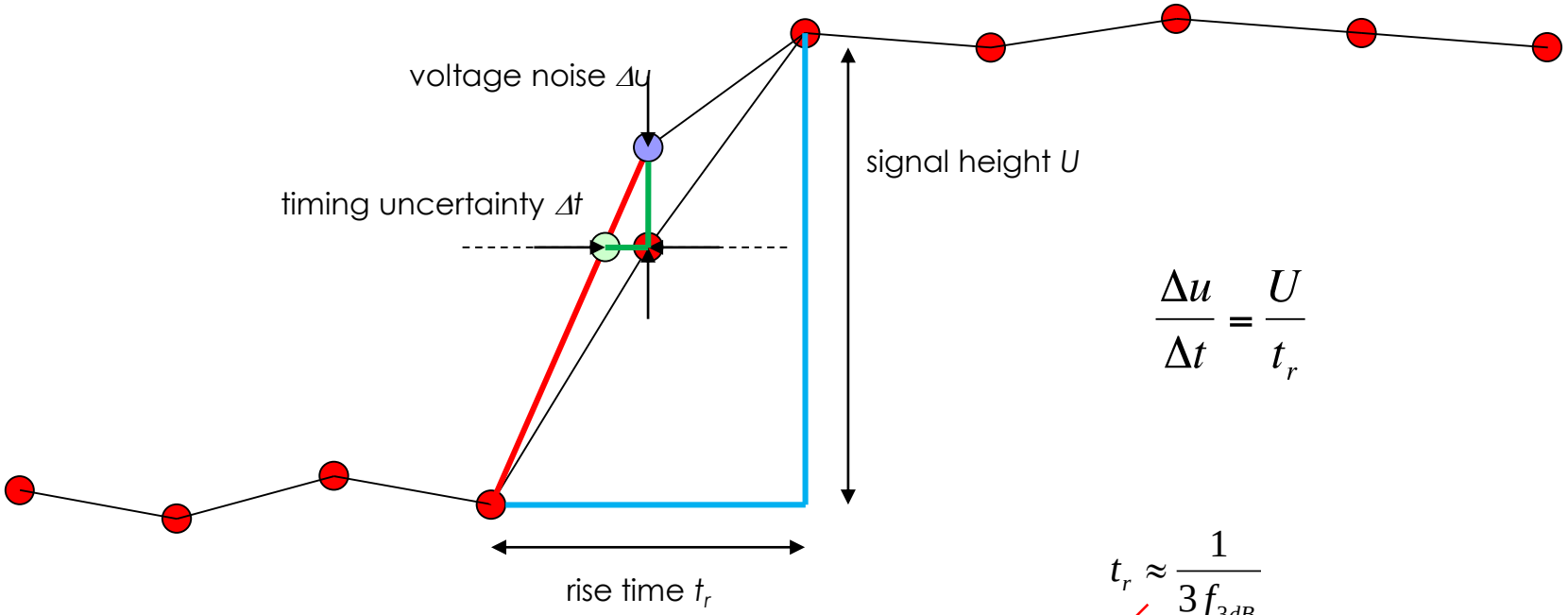

J.-F. Genat et al., arXiv:0810.5590 (2008)




D. Breton et al., NIM **A629**, 123 (2011)

# How is timing resolution affected




$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

number of samples on slope

# How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

| | $U$ | $\Delta u$ | $f_s$ | $f_{3db}$ | $\Delta$t |
|---|---|---|---|---|---|
| today: | 100 mV | 1 mV | 2 GSPS | 300 MHz | ~10 ps |
| optimized SNR: | 1 V | 1 mV | 2 GSPS | 300 MHz | 1 ps |
| next generation: | 1 V | 1 mV | 10 GSPS | 3 GHz | 0.1 ps |

↑

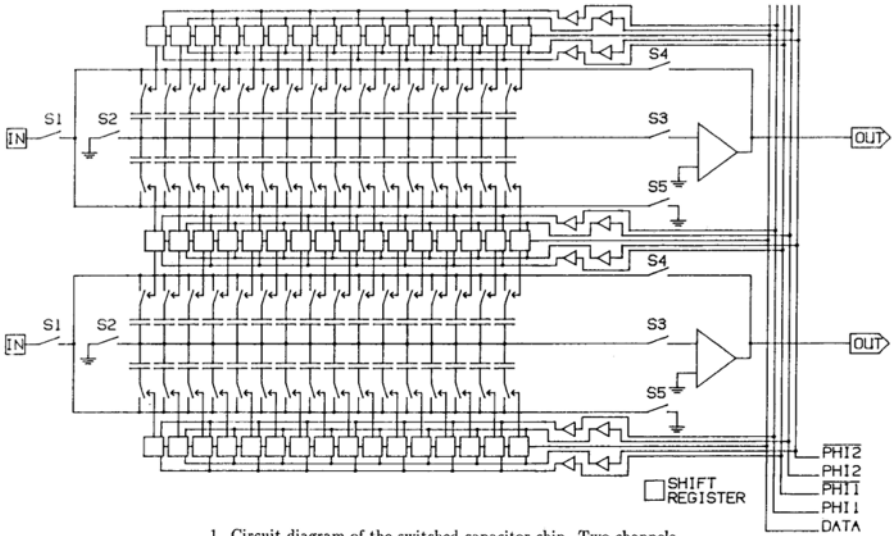
- high frequency noise
- quantization noise

# First Switched Capacitor Arrays

DEVELOPMENT OF A SWITCHED CAPACITOR BASED
MULTI-CHANNEL TRANSIENT WAVEFORM RECORDING
INTEGRATED CIRCUIT

Stuart A. Kleinfelder

Lawrence Berkeley Laboratory
Berkeley, California 94720




1. Circuit diagram of the switched capacitor chip. Two channels of 32 sample and hold cells per channel are shown. The I.C. contains 16 channels of 128 cells per channel.

IEEE Transactions on Nuclear Science,
Vol. 35, No. 1, Feb. 1988

50 MSPS in
3.5 μm CMOS process

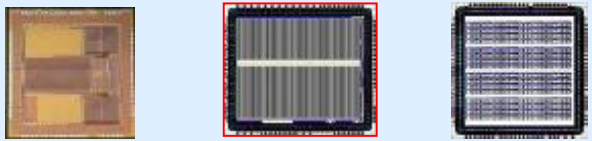
# Switched Capacitor Arrays for Particle Physics

G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

STRAW3 LABRADOR3 TARGET



- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

**www.phys.hawaii.edu/~idlab/**

AFTER SAM NECTAR0


- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

**matacq.free.fr**

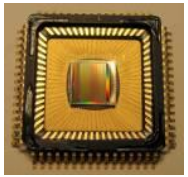
PSEC1 - PSEC4

- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

**psec.uchicago.edu**

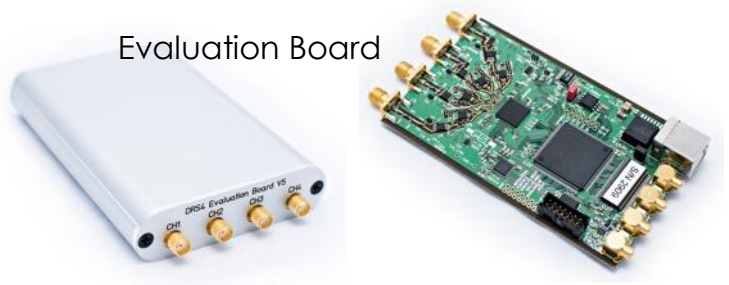
# DRS4 Chip

- Developed at PSI in **2008** together with R. Dinapoli
- **5 Gsamples/s**, 12 bits resolution, 8+1 channels, 17.5 mW/channel
- Time measurements down to **10 ps**



DRS4 Chip

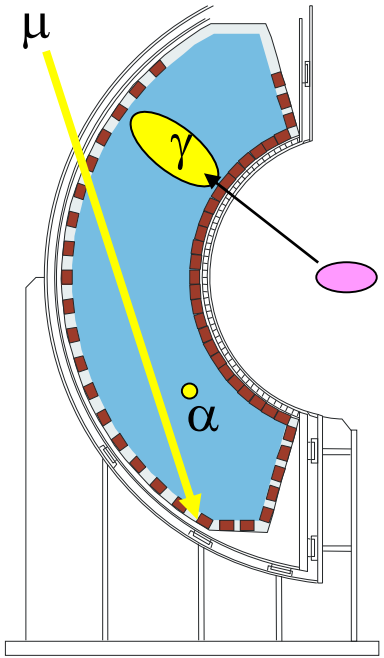
Evaluation Board



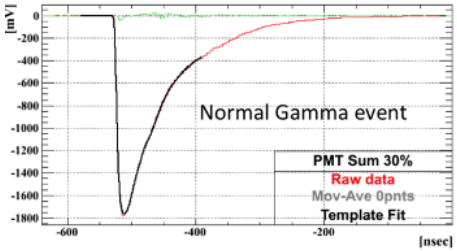
9000+ channels of MEG II, PSI

WaveDREAM Board

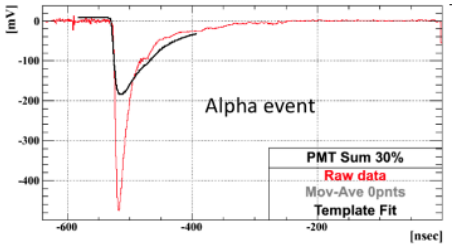
# Pulse shape discrimination



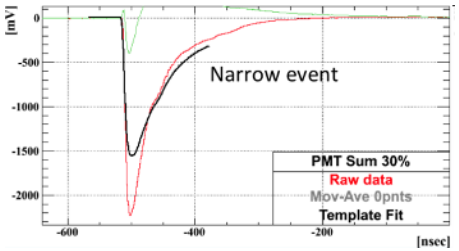

γ




α

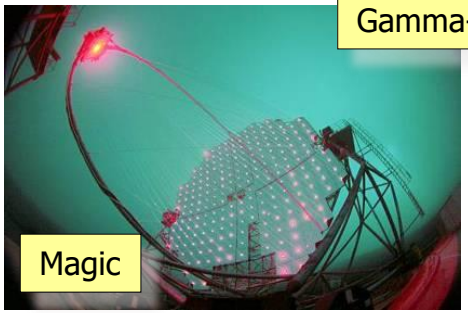


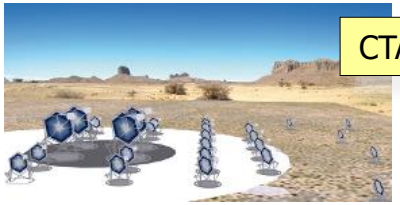

μ

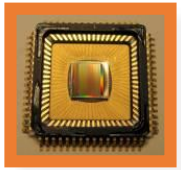


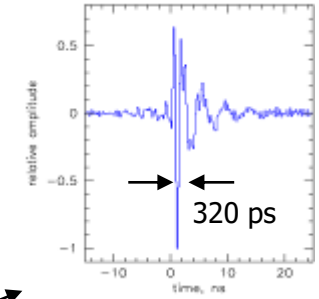

Events found and correctly processed
**2 years** (!) after the data has been taken

# Applications of SCA

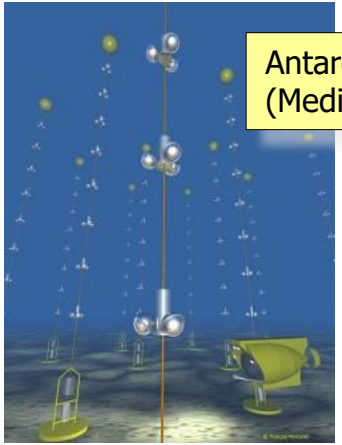


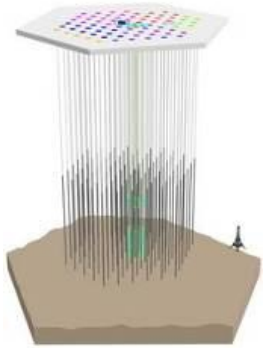



Antarctic Impulsive Transient Antenna (ANITA)



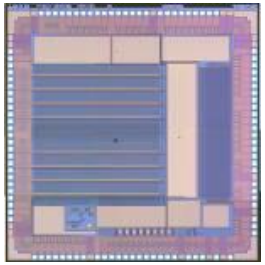
Antares (Mediterranian)

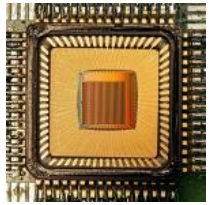
ToF PET (Siemens)



IceCube (Antarctica)

# Conclusions





- SCA technology offers tremendous opportunities
- Several chips and boards are on the market for evaluation
- New series of chips on the horizon might change front-end electronics significantly