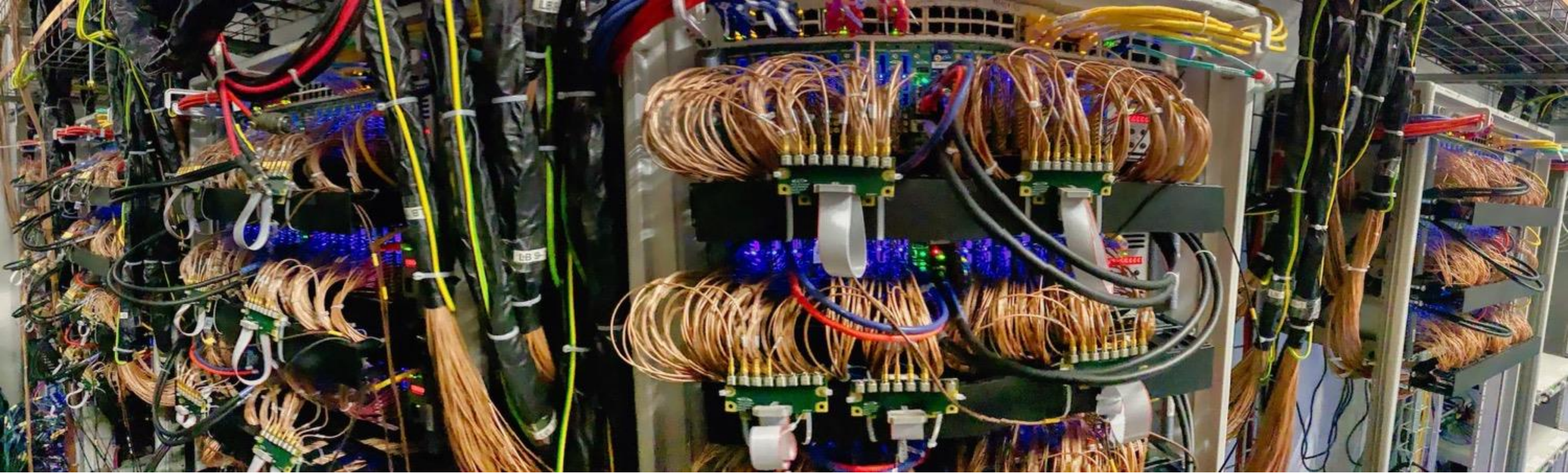


Electronics and DAQ

Stefan Ritt, Paul Scherrer Institute, Switzerland
IEEE NPSS Workshop on Applicatioins of Radiation Instrumentation
Nov. 14th, 2022, Dakar, Senegal

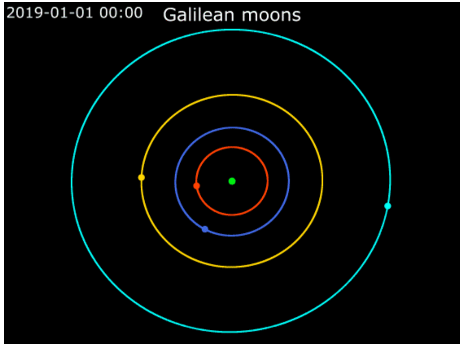
Stefan Ritt

- Studied in Karlsruhe, Germany
- Postdoc Univ. of Virginia, USA
- Head of muon physics group at PSI, Switzerland
  - Developer of MIDAS DAQ system https://midas.triumf.ca
  - Developer of DRS4 chip https://www.psi.ch/drs
  - Developer of ELOG electronic logbook https://elog.psi.ch/elog/
  - Co-spokesperson of Mu3e Experiment https://www.psi.ch/mu3e
  - Fellow of IEEE NPSS society https://ieee-npss.org
- Hobbies: Biking, Scuba diving, Drone flying, 3D printing

IEEE
NPSS
NUCLEAR & PLASMA SCIENCES SOCIETY

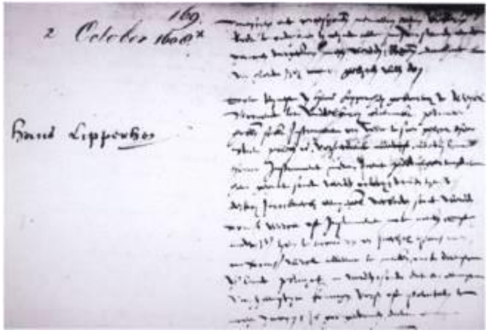
Discovery and Instrumentation

In 1610
Galileo Galilei
discovered four
Jupiter moons



Jean-Leon Huens, National Geographic

In 1608
Hans Lippershey
filed a patent for
a telescope



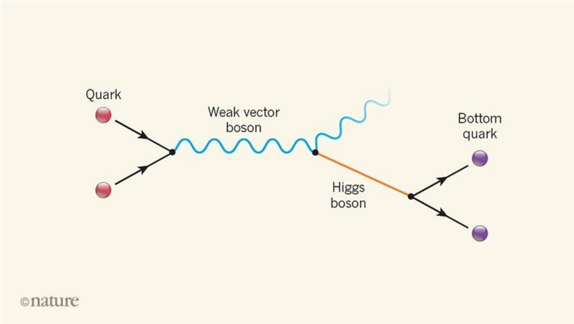
169.

2 October 1608

Hans Lipperhey

← what was more important? →

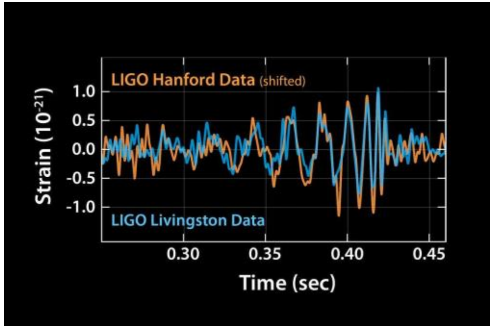
Recent discoveries



Higgs Boson

2013

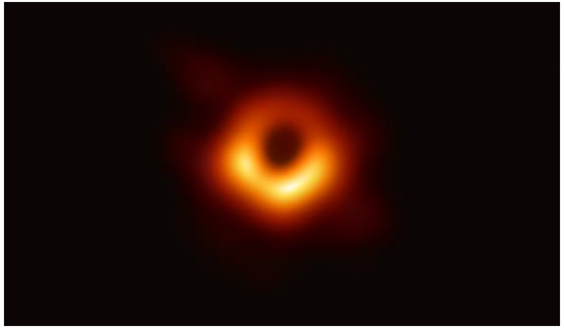
LHC Detector



Gravitational Wave

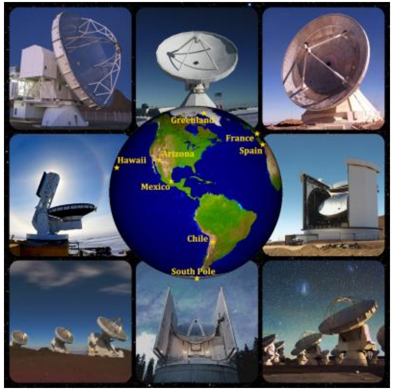
2017

Ligo Detector

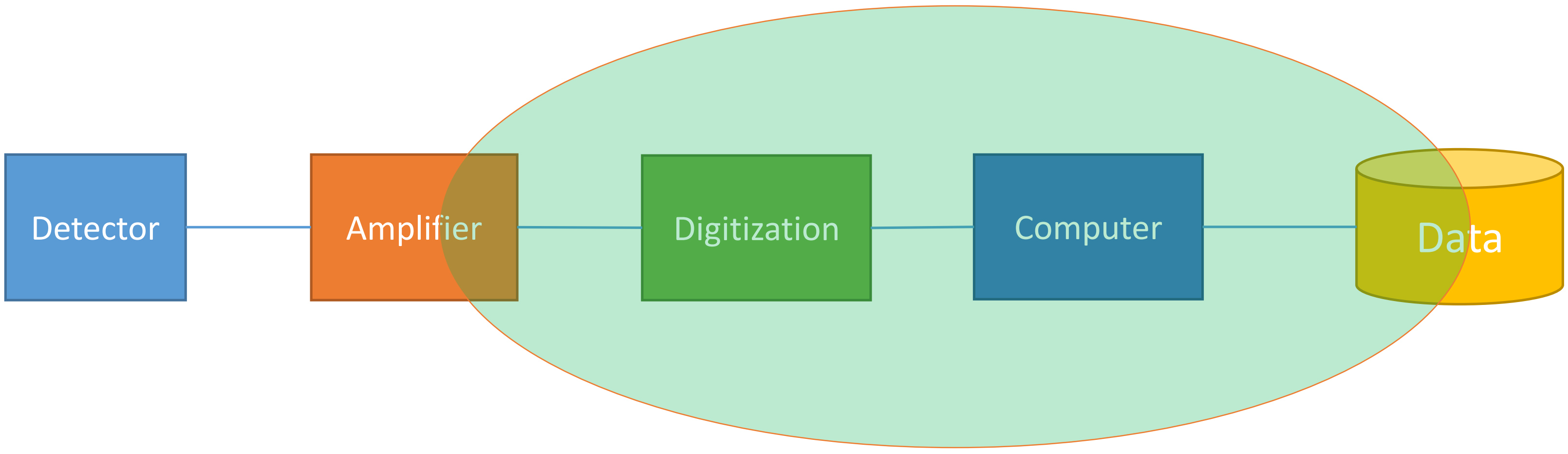


Black Hole

Event Horizon Detector Network



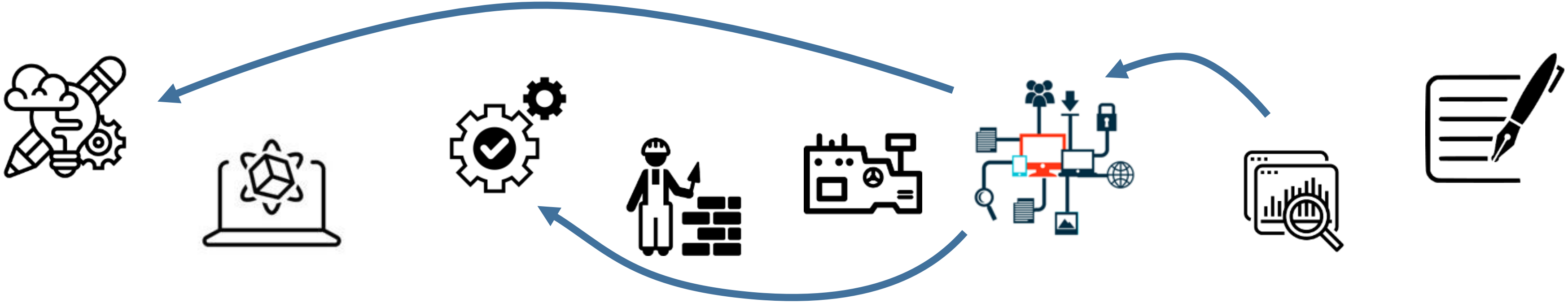
From Detectors to Data



This Talk

Data acquisition (DAQ) in the context of an experiment?

- DAQ **links** the **hardware** and the **data analysis**
- DAQ needs **consideration** in the **design** of the experiment
- DAQ provides **tools** for the **validation** of the experiment
- **Analysis** requires detailed **knowledge** of DAQ



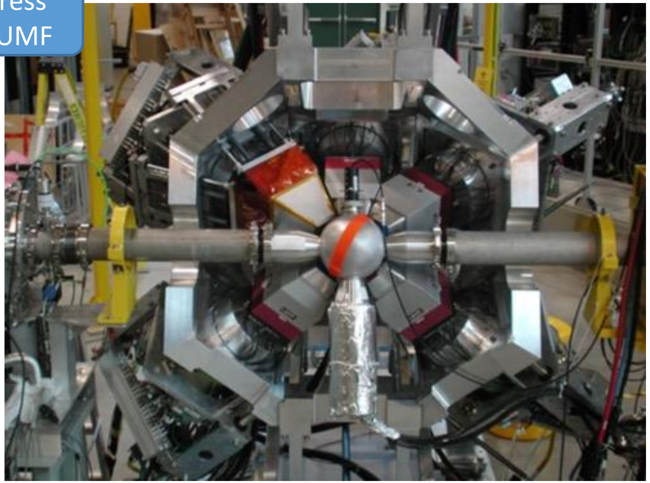
Design Prototyping Construction Data Acquisition Publication

Simulation Testing Implementation Analysis

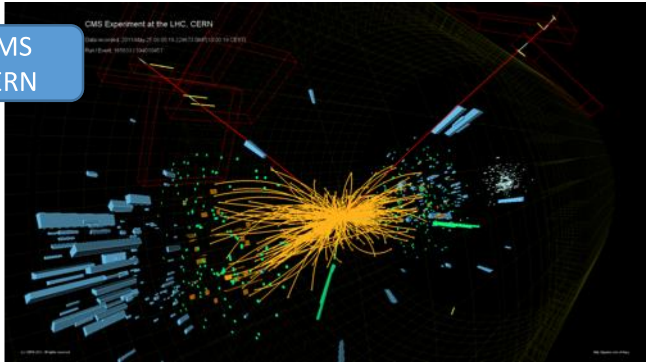
Measured quantities in Particle Physics

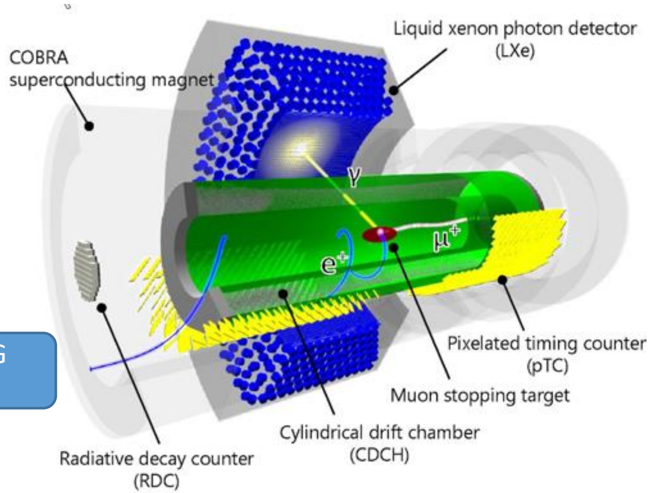
- **Position** → position sensitive detectors
- **Time** → resolutions down to ps
- **Energy** → calorimeter
- **Momentum**, **Charge** → curvature in B-field

Tigress
TRIUMF



CMS
CERN



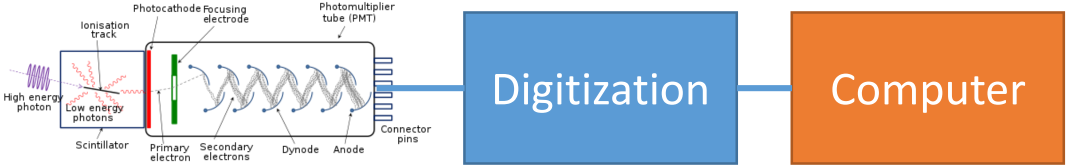


MEG
PSI

Particle Detection

- Old days: Looking **by eye** at scintillators

- Today: Converting detector signal into **electronic signals**



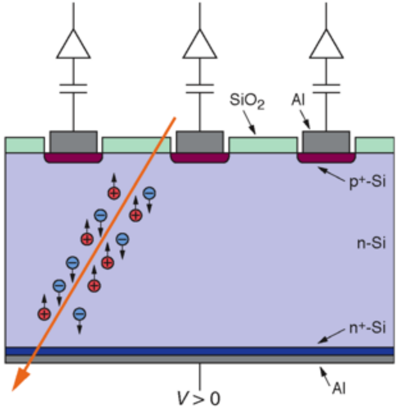
Digitization

Computer

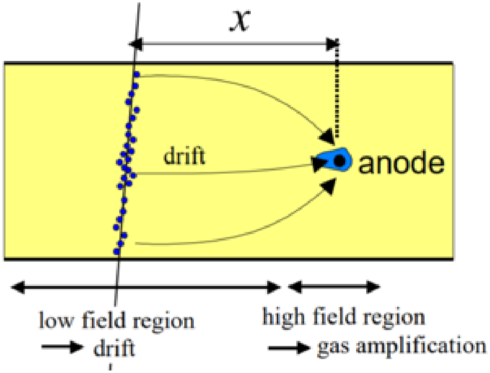
2 Principles of Detection of Ionizing Radiation

1. Detectors convert **property** to be measured directly into **electrical signal** → **position, time**
2. **Indirect** via light generation in scintillator → **energy, time**

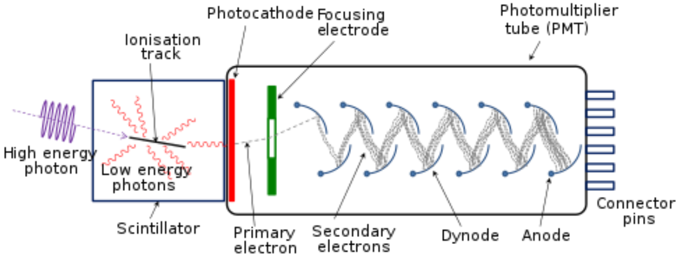
→ See other Lectures



Silicon detector



Wire chamber



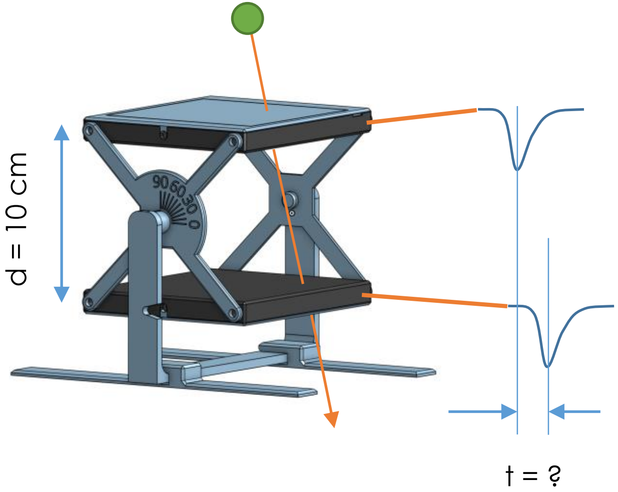
Photomultiplier

Signals and Electronics

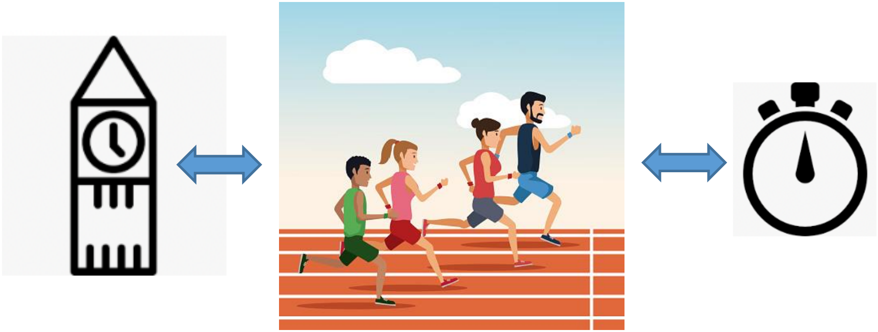
How we process the information from detectors

Signals are fast!

- Cosmic Muon with 90% speed of light hits two detectors 10 cm apart
- What is the time difference between the two signals?

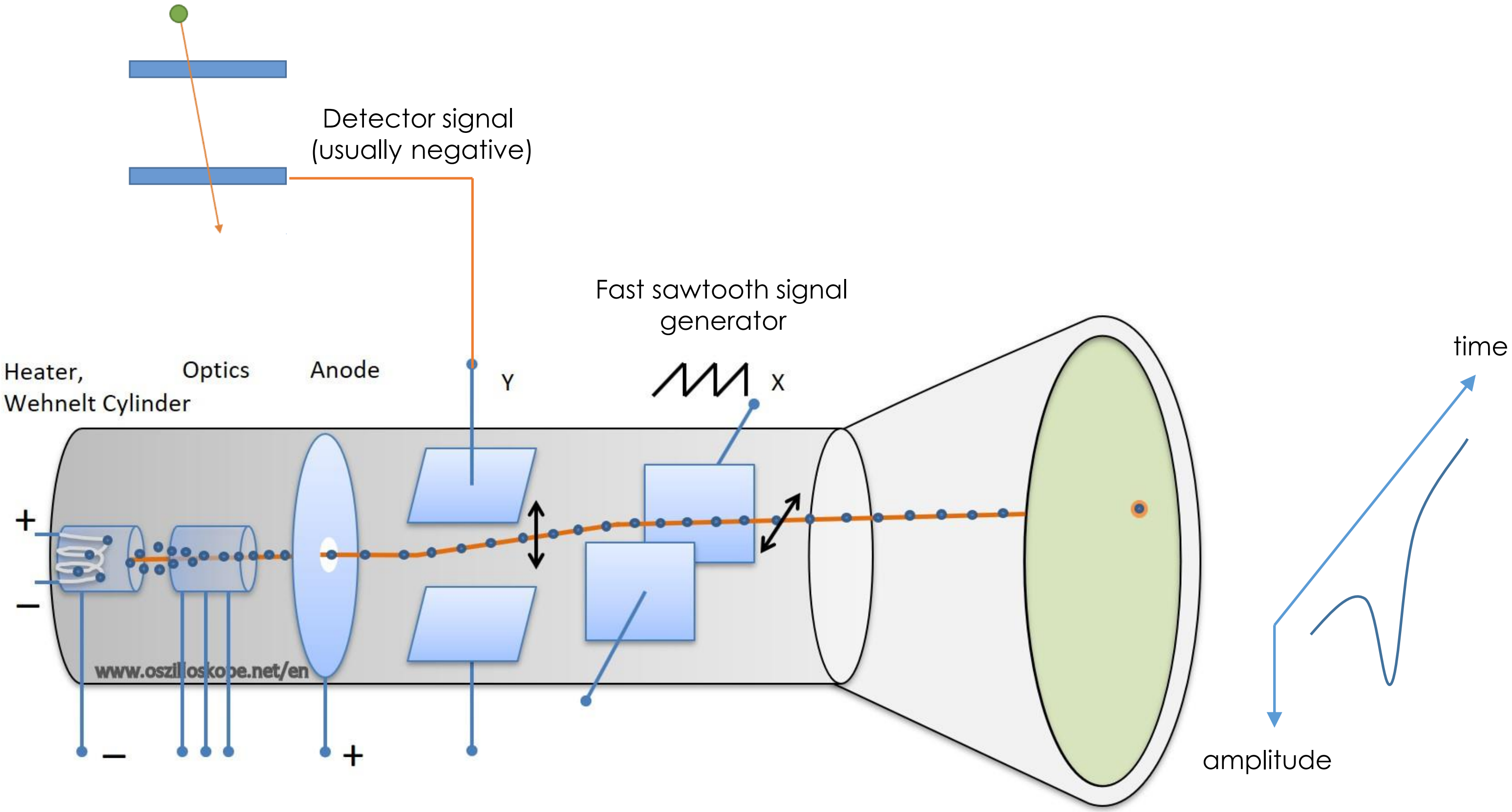


$$t = d / v = 0.1 \text{ m} / (0.9 * 3*10^8 \text{ m/s}) = 0.0000000004 \text{ s} = 0.4 \text{ ns}$$



You need a fast clock!

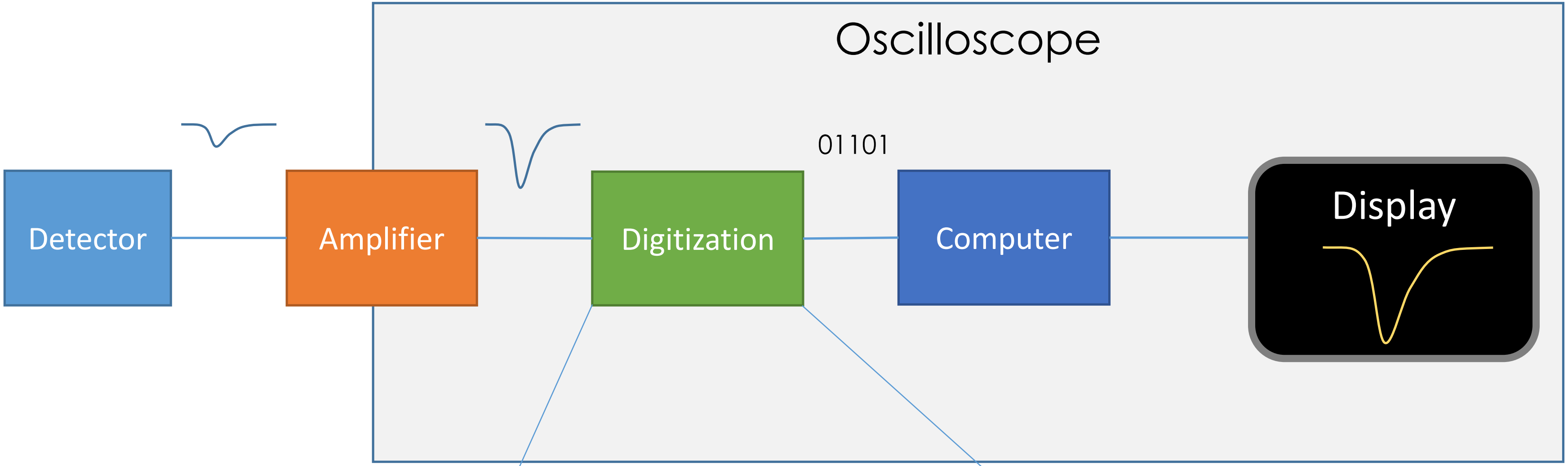
Principle of an oscilloscope

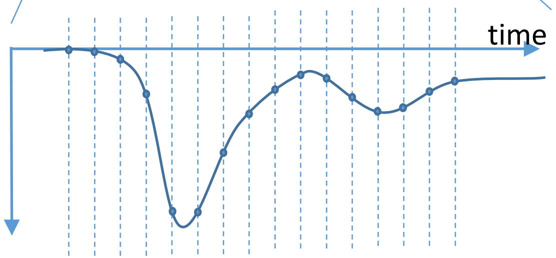


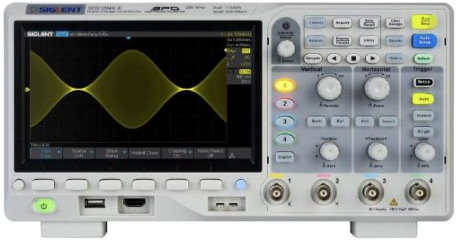
Detector signal
(usually negative)

Fast sawtooth signal
generator

Modern Digital Oscilloscopes





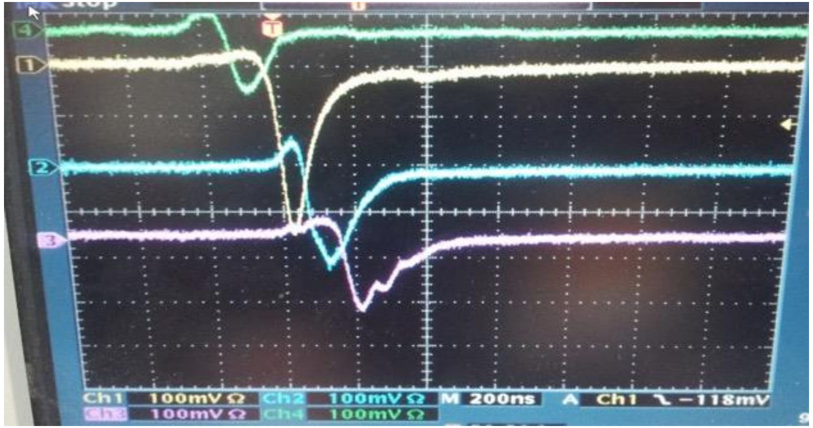


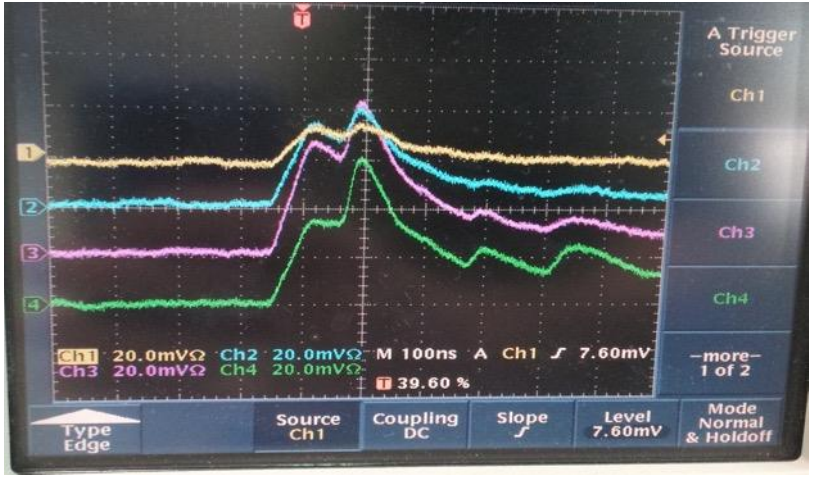
Electronic Signals

- **Electrical signals** are well suited for **transport**, **manipulation**, **digitization** and storage
- Signals can be easily amplified (typically $\mathbf{10^6}$ **-**$\mathbf{10^{10}}$)

  $Q_{e-} = 1.6 \times \mathbf{10^{-19}}\ \mathrm{C}$

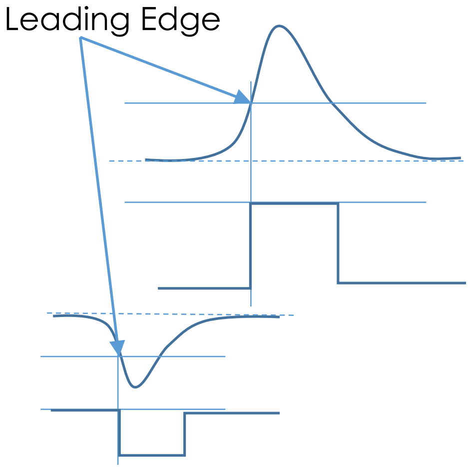
  $100\ \mathrm{mV} \times 10\ \mathrm{ns} = \mathbf{10^{-9}}\ \mathrm{C}$
- Electrical signals let you **discriminate** between signal and noise
- **Coincidence** between detectors can be made with AND gates



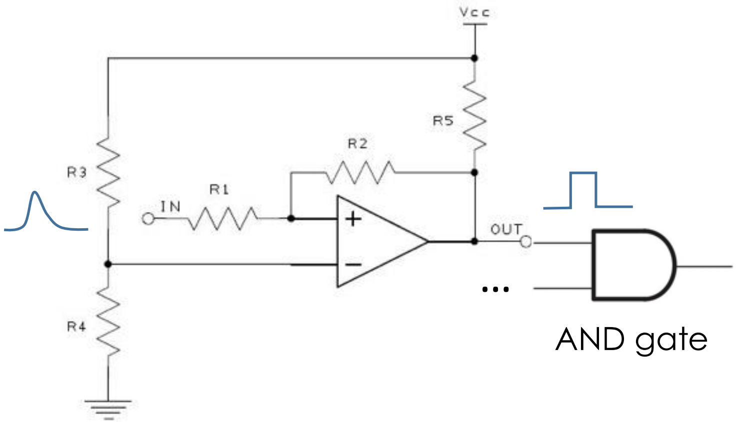


Signal Discrimination

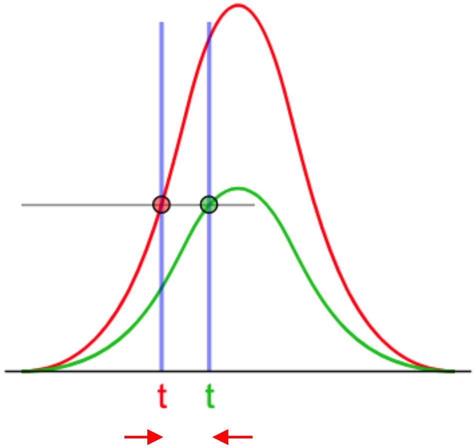
- Convert **analog** detector signal to **digital** signal
  - **Digital** signal can be processed in **logic** and **computers** ("0"/"1")
  - Good for **detection** and timing
  - Problem: "**Time-walk**" effect



Comparator



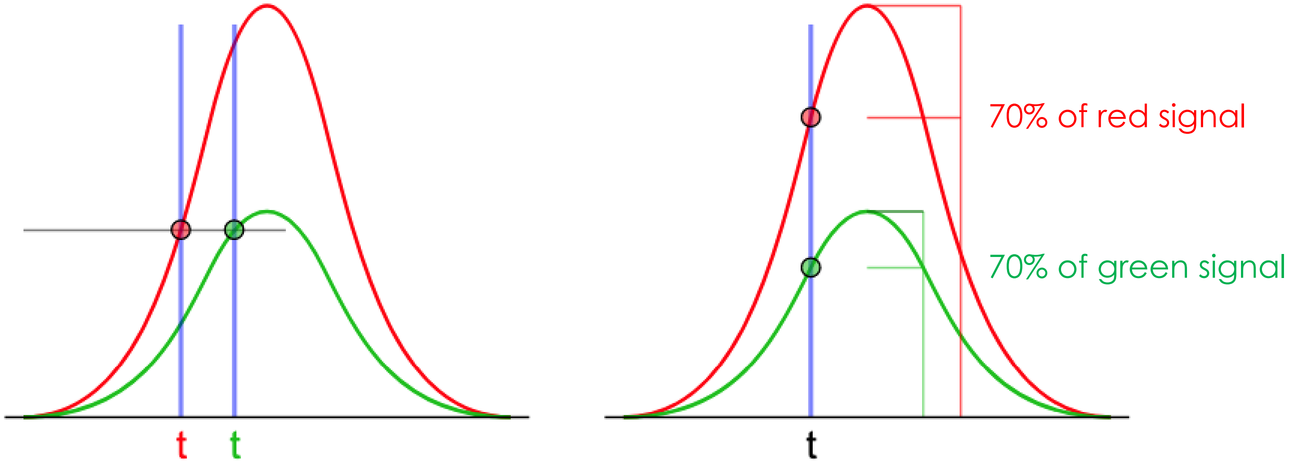
AND gate



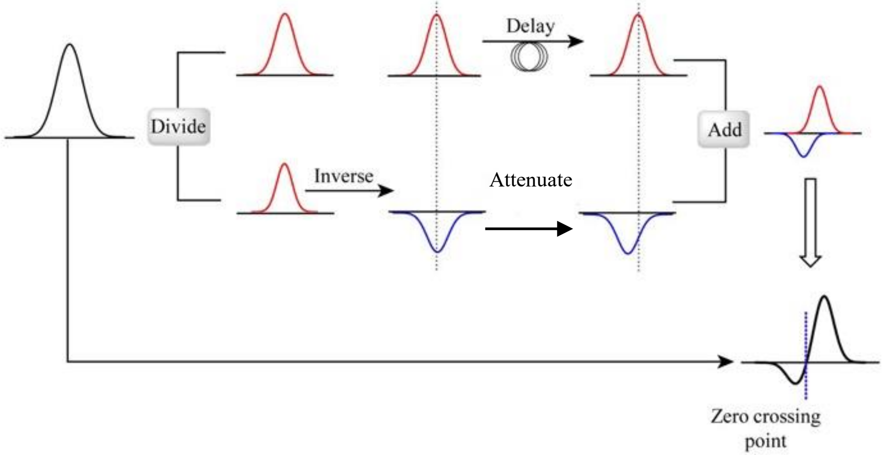
Time Walk

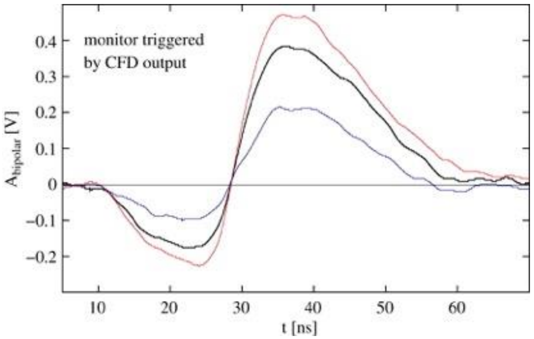
Signal Discrimination

- **Constant Fraction** Discriminator (CFD) triggers **independent** of signal amplitude
- Trick: do not trigger at constant threshold, but at **constant fraction** of signal amplitude

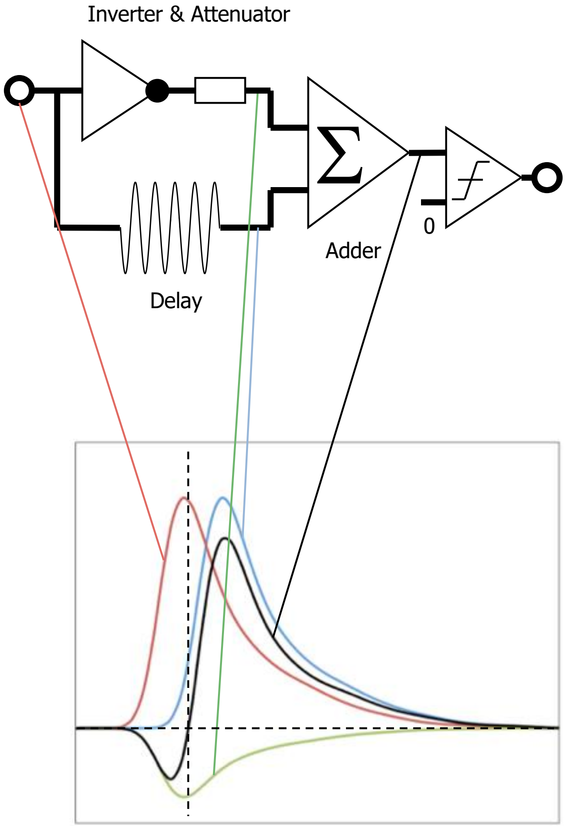


Implementation of a CFD



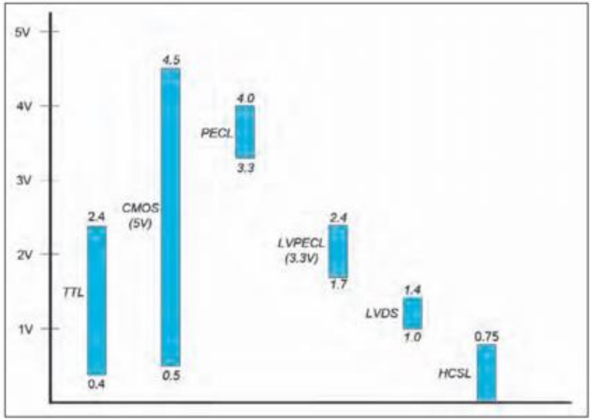


https://doi.org/10.1016/j.nima.2012.04.088



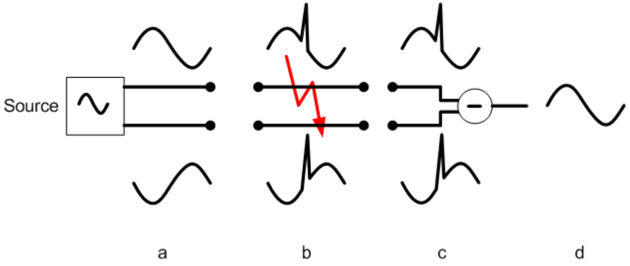
Digital Signal Levels

- Different signal levels **standards evolved** over time driven by
  - Available transistor **technology**
  - **Speed** of signals
  - **Noise** immunity
  - **Power** consumption



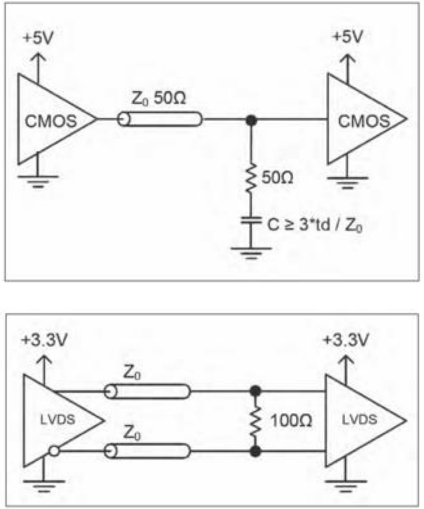
hf-praxis 6/2014

Voltage Levels



https://doi.org/10.1088/1742-6596/278/1/012039

Differential Signaling



Termination

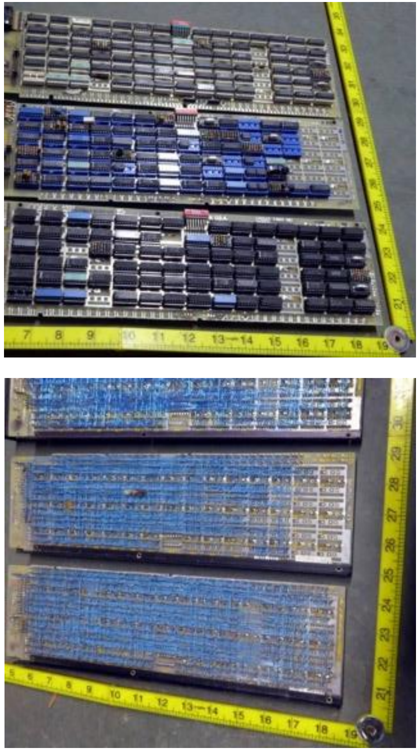
Analog-to-Digital Conversion

→ *Shifted to Nov. 25th lecture*

File Programmable Gate Arrays

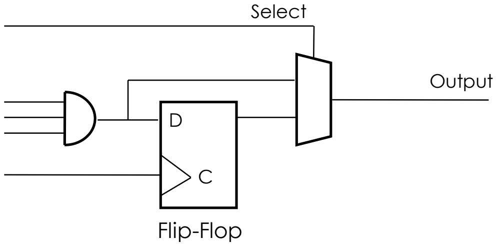
How to process digital data

Field Programmable Gate Array (FPGA)

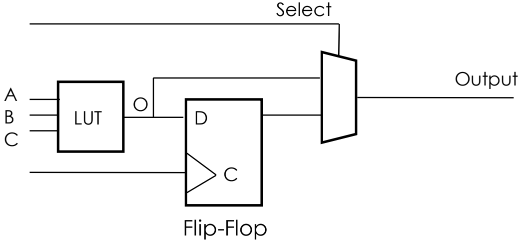


Wire-wrap technique 1960- (Apollo 11)

Basic Logic Block



Programmable Logic Block with LUT

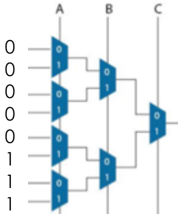


Memory Content

Memory Address

A	B	C	O
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	**1**	**1**	**1**

O = A and B and C

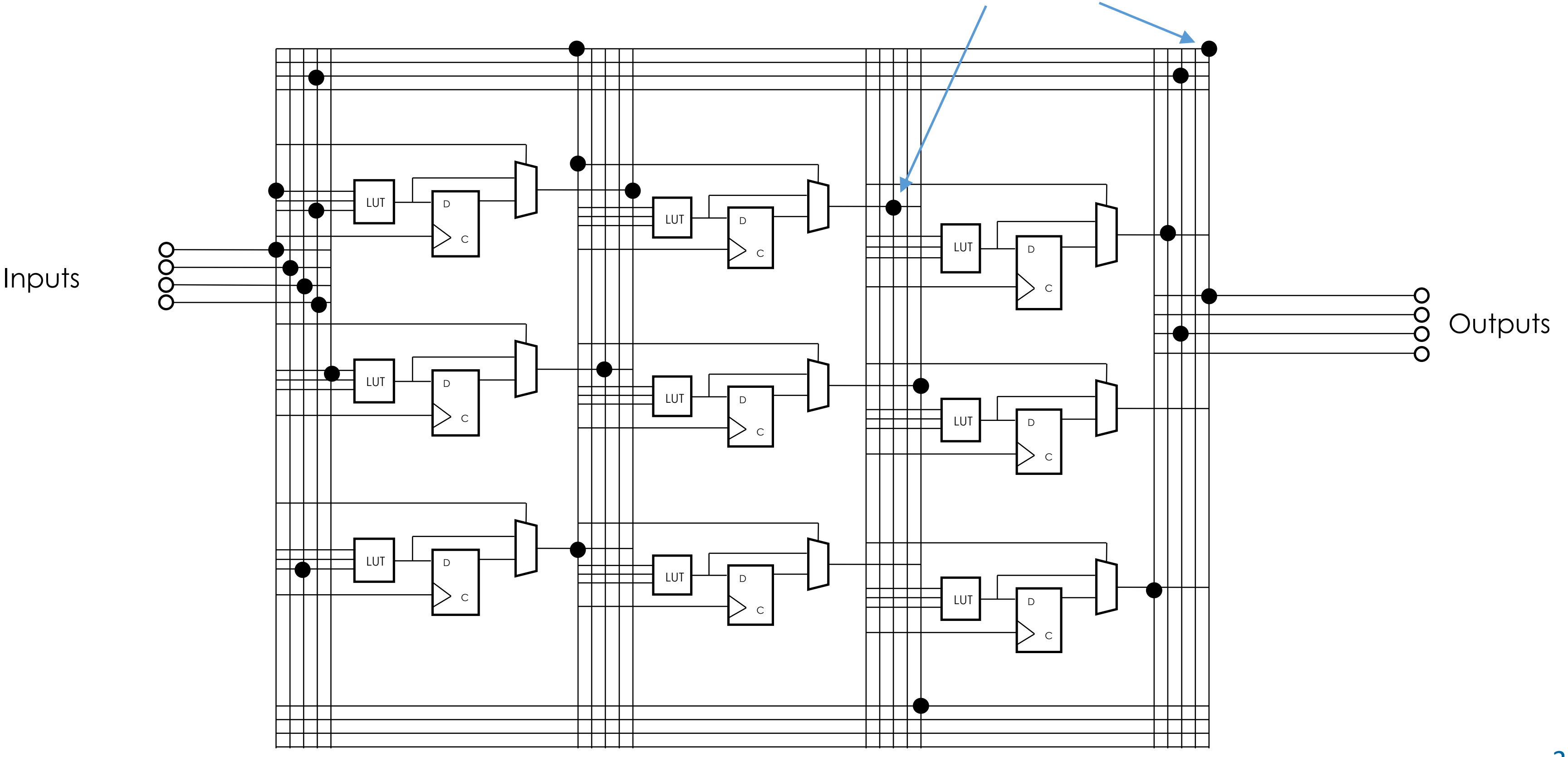


A	B	C	O
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	**1**	**1**
0	**1**	**1**	**1**
1	**1**	**1**	**1**

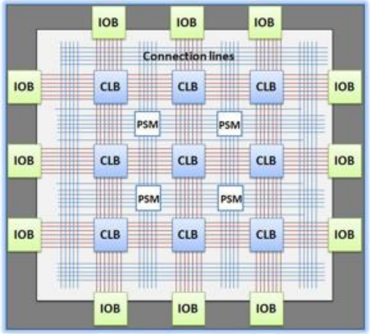
O = (A or B) and C

FPGA interconnects

Wire connections:
Fuse: Programmable Logic Device (PLD)
Switch+1-bit memory: Field Programmable Gate Array (FPGA)



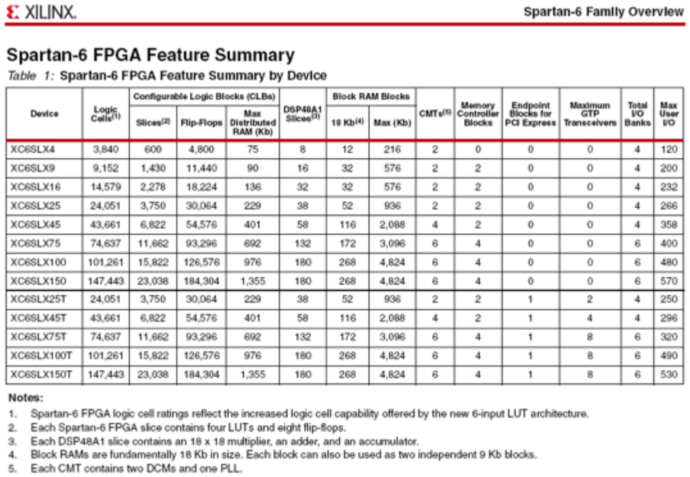
Modern FPGA



IOB
Input-Output Block

CLB
Configurable Logic Block

PSM
Programmable Switch Matrix



XILINX — Spartan-6 Family Overview

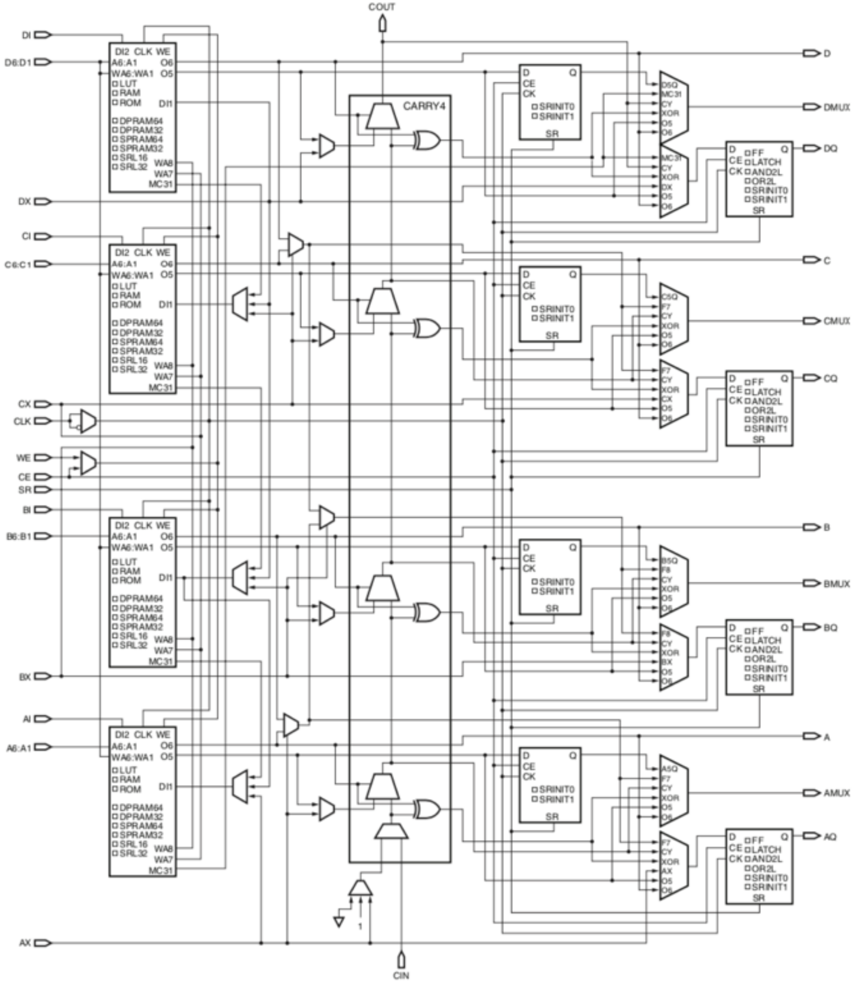
Spartan-6 FPGA Feature Summary

Table 1: **Spartan-6 FPGA Feature Summary by Device**

Device	Logic Cells(1)	Configurable Logic Blocks (CLBs)			DSP48A1 Slices(3)	Block RAM Blocks		CMTs(5)	Memory Controller Blocks	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices(2)	Flip-Flops	Max Distributed RAM (Kb)		18 Kb(4)	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	120
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,750	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	400
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	570
XC6SLX25T	24,051	3,750	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	320
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	490
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	530

Notes:

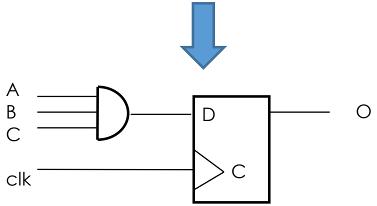
1. Spartan-6 FPGA logic cell ratings reflect the increased logic cell capability offered by the new 6-input LUT architecture.
2. Each Spartan-6 FPGA slice contains four LUTs and eight flip-flops.
3. Each DSP48A1 slice contains an 18 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.
5. Each CMT contains two DCMs and one PLL.



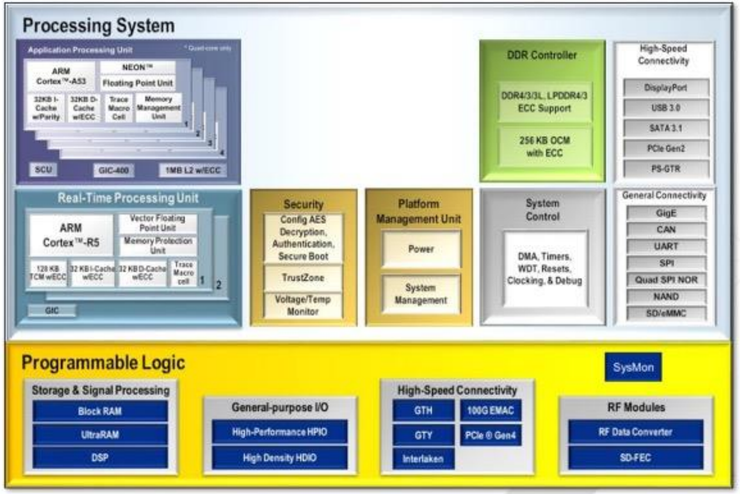
Xilinx Spartan 6 Configurable Logic Block

FPGA features

```
if rising_edge(clk) then
  O <= A & B & C;
end if
```



- Today almost all logic is done with FPGAs in particle physics
  - Programming via Hardware Definition Languages (**VHDL**, Verilog)
  - **Re-programmable even after installation**
  - High cost of FPAG ($10-$1000) not so important
- Modern FPGA (Xilinx, Altera, Lattice, …) have many features:
  - Digital Signal Processing Blocks (**DSP**)
  - Block **RAM**
  - Gigabit **serial links**
  - Connectivity (USB, Ethernet, …)
  - Soft/Hard-core **CPUs**
- Particle physics:
  - **Read** ADC/TDC
  - **Pre-process** data
  - **Send** data via high speed serial links



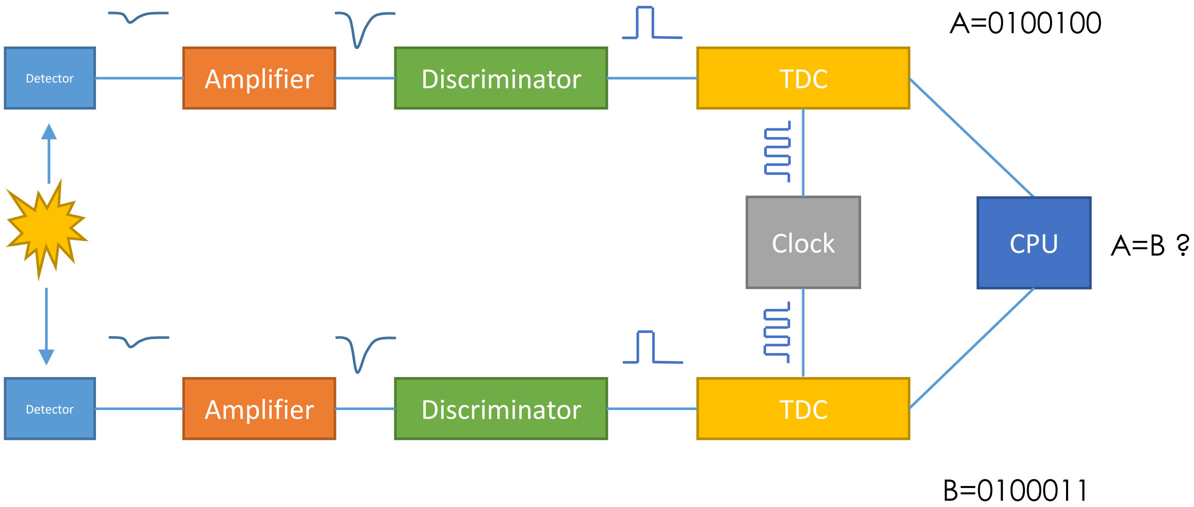
Xilinx Zync Ultrascale+

Time-To-Digital Conversion

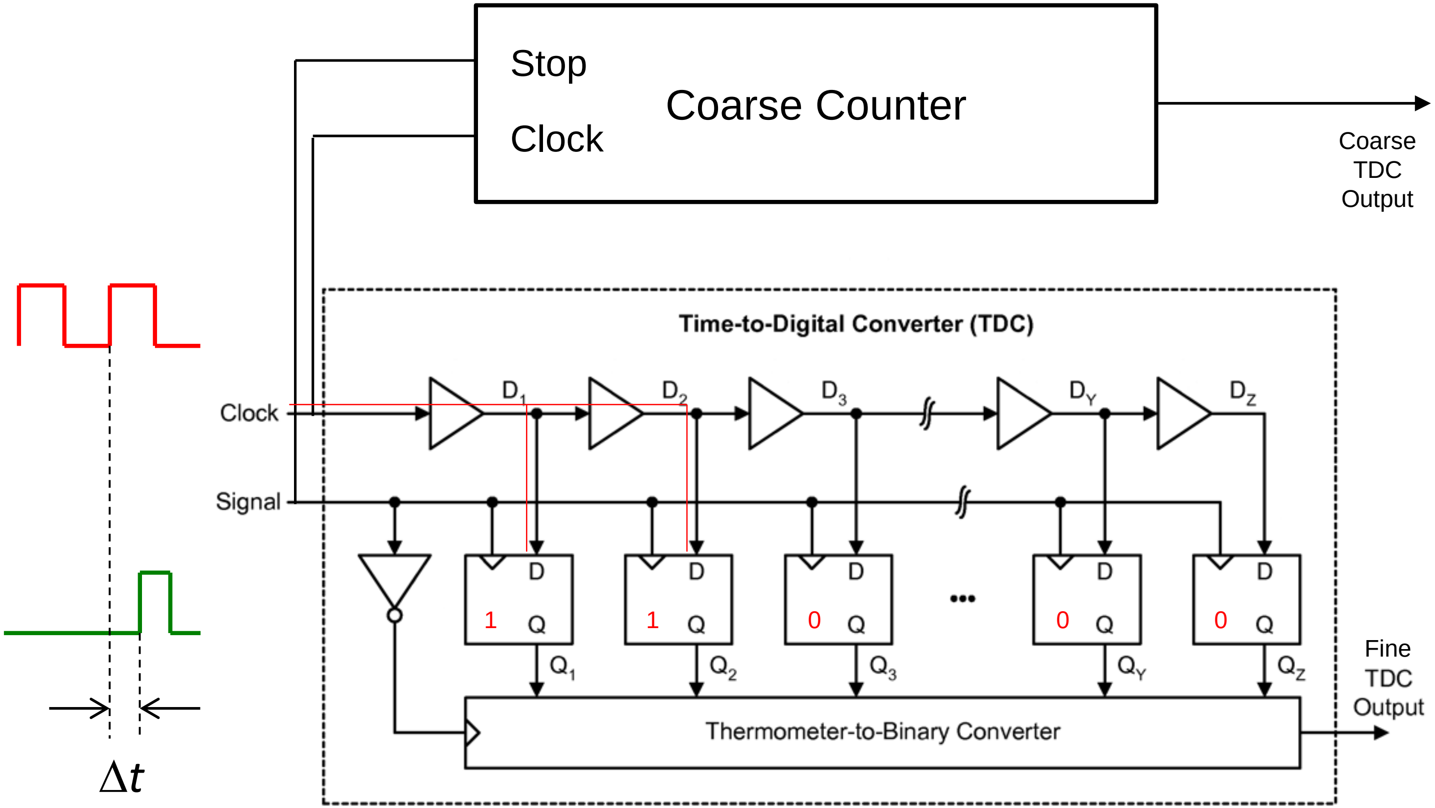
TDCs

TDCs

- Often it is enough to know **time** of event
- **Time-to-digital** converter to measure relative time



Digitization: Time-to-digital Converter



Examples of TDCs

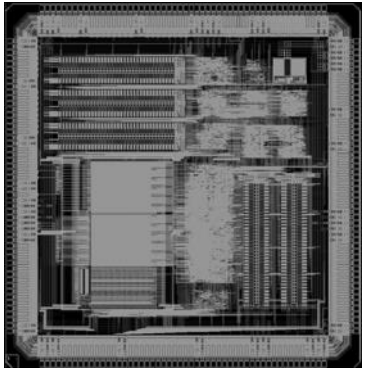
HPTDC (CERN)

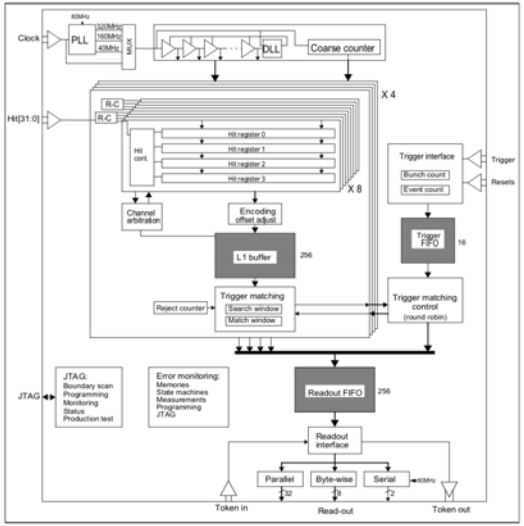
32 channels, 17 ps resolution

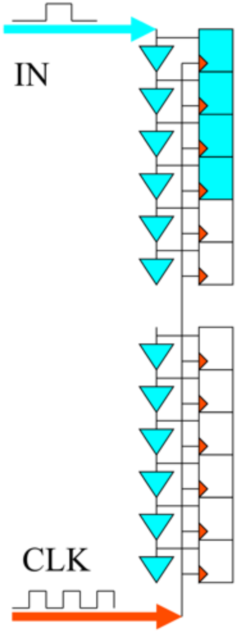
FPGA TDC

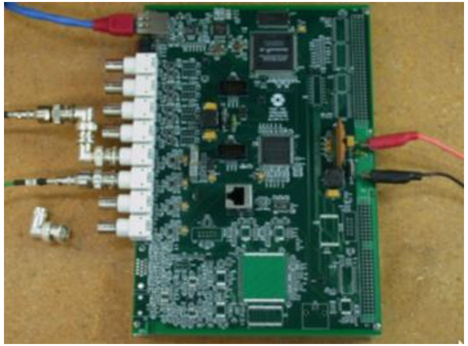
Jinyuan Wu (Fermilab): 32 channels, 10 ps resolution

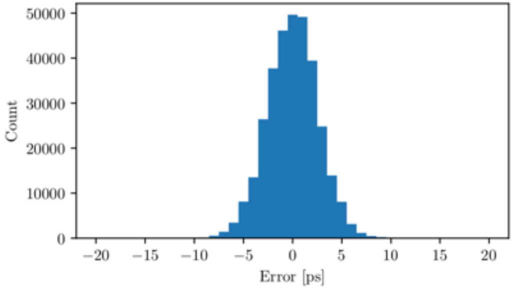
Sven Engström (Linköping Univ.): 1.8 ps resolution









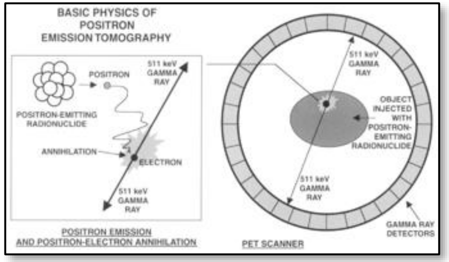


Triggering

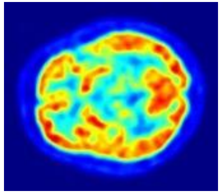
How to reduce your data to be recorded

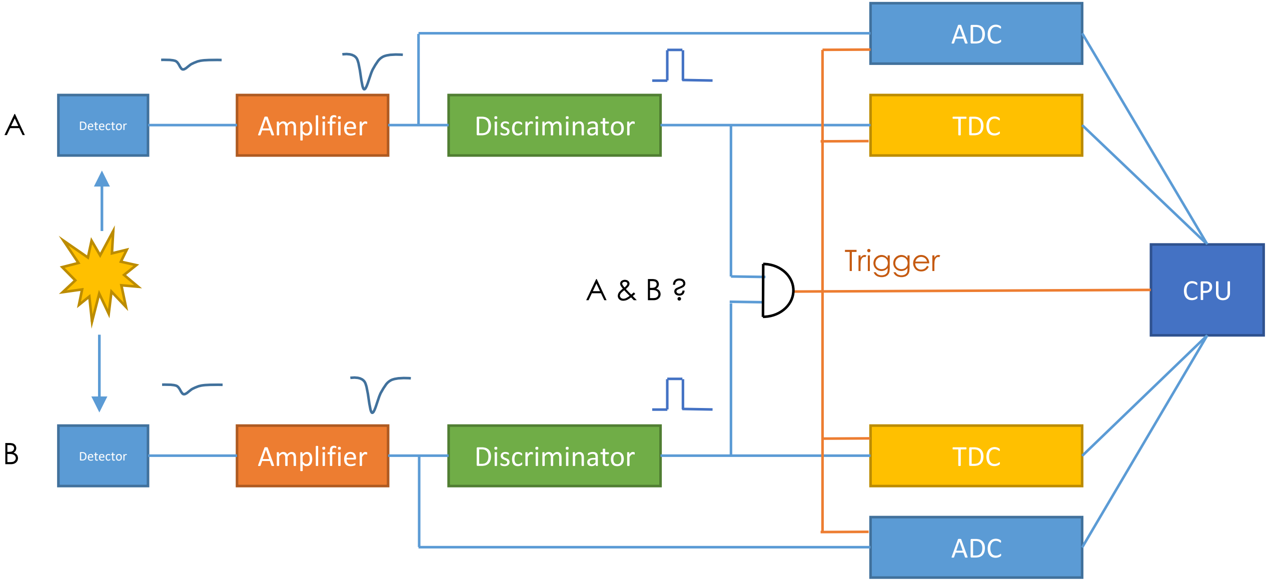
Triggering

- Detectors produce **continuous** electrical signal
- You might only be interested in “**events**”
- **Trigger** your readout electronic only if something “**happens**”
- Can **reduce** your **data rate** enormously



PET image of human brain



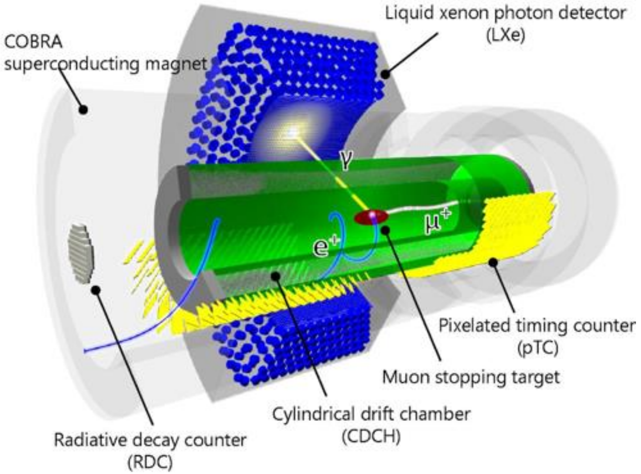


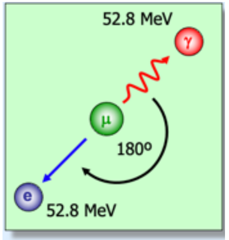
Trigger of MEG Experiment

- Event size: 3 MB
- Muon stop rate: **10^8** Hz
- LXe rate: **10^5** Hz

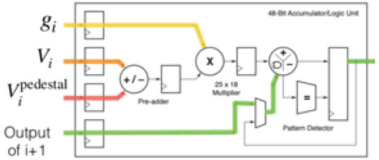
  → 300 GB/s
- Energy sum trigger → **10^3** Hz
- Time trigger → **10^2** Hz
- Direction match → **10** Hz

  → Data rate **30 MB/s**

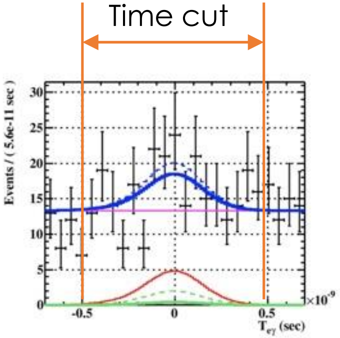


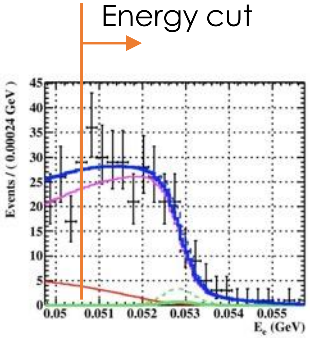


Goal: BR < ~ 10^{-13}



DSP Block in FPGA
to add weighted sum

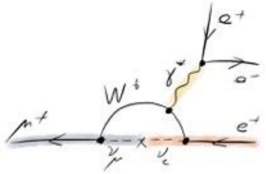


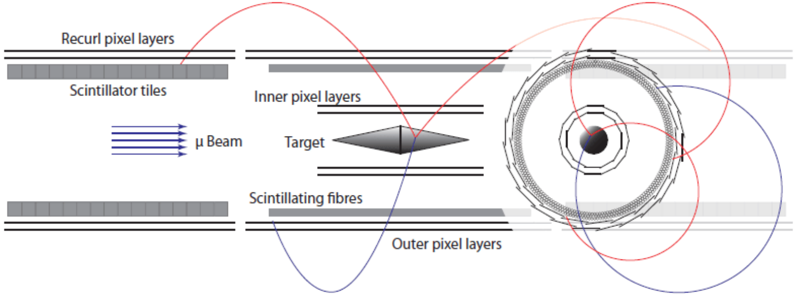


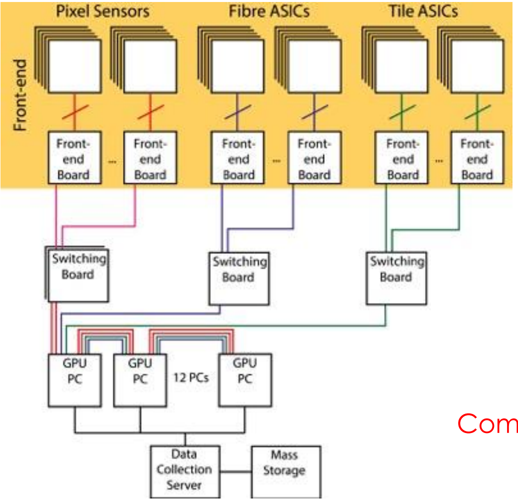
Trigger-less DAQ

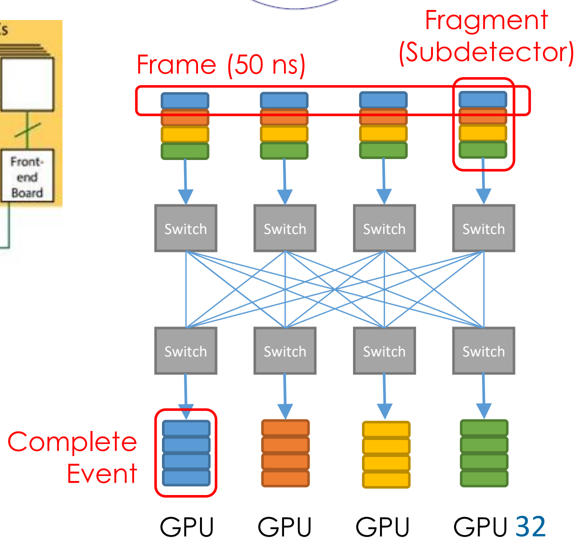
- **Mu3e** experiment at PSI searches for decay $\mu \rightarrow e^+e^-e^+$
- **200 M pixels** are very hard to trigger on
- **Trigger-less** DAQ:
  - **each** particle hit is sent out
  - **~100 GB/s**
    → 100's of high speed optical links
  - Switching boards for "**event building**"
  - Send full events in 50 ns "**frames**" to 12 GPUs
  - GPUs do full event reconstructing and can **reject 99.9%** of background

  → **100 MB/s** data rate









Bus Standards

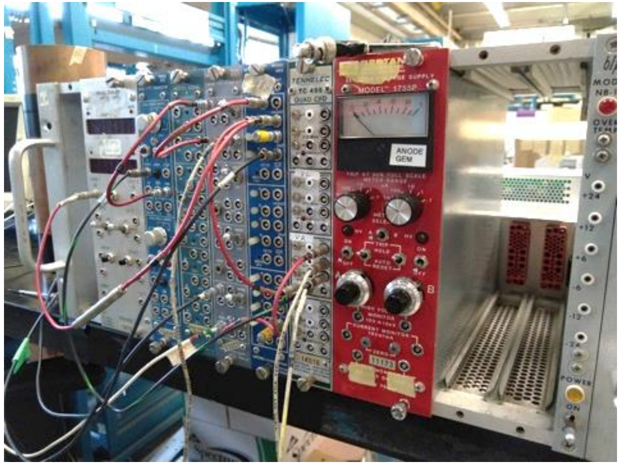
… used in particle physics over the years

Bus standards

- **NIM** (1968): Nuclear Instrument Module
  - Still in use for standard logic for workbench tests
- **CAMAC** (1972): Computer Automated Measurement and Control, use TTL parallel bus
  - Still in use in older system (Triumf/PSI Cyclotron Control)
- **VME** (1981): Vesa Module Europcard
  - Very much in use, as VME modules are still commercially available (parallel backplane bus).
- **FastBus** (1984): To replace CAMAC with ECL parallel bus
  - Dead
- **VXI** (2004): VME eXtensions for Instrumentation
  - Was an extension to fit a transition…
- **VXS** (2006): VMEBus Switched Serial
  - In use due to its serial bus backplane and slot configuration (Full mesh, Dual star). Redundant system (five-9 / max down time of 5.26 minutes per year.)
- **ATCA** (uTCA) (2003): Advanced Telecommunications Computing Architecture
  - PCI Industrial Computer Manufacturers Group (PICMG)
  - New trend for Physics applications, combines VXS, self-managed crate, Single -48V, fully differential connections.

Nuclear Instrument Module (NIM) 1968

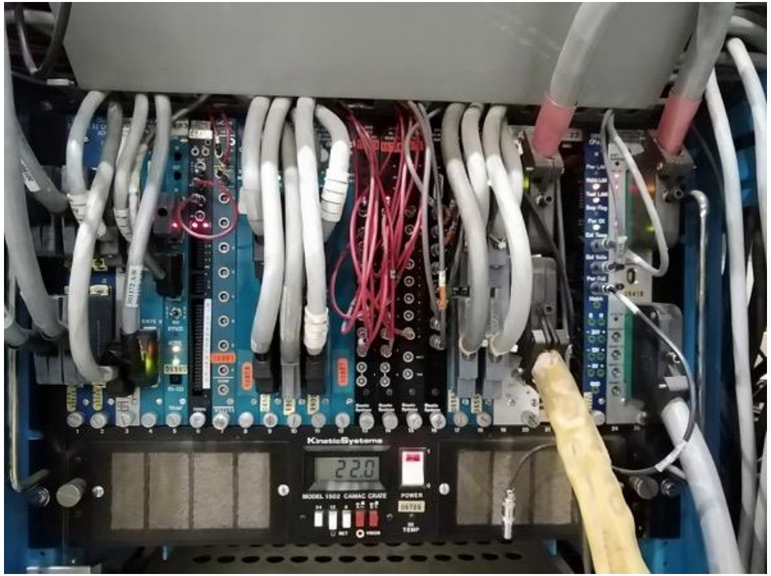
- Basic Analog Elements
  - Delay
  - Splitter
  - Discriminator
  - Attenuator
  - Amplifier/Shaper
- Basic Logic Elements
  - AND/OR
  - Latch
  - Timer
  - Scaler



Power:
+/- 6V
+/- 12V
+/- 24V

Computer Automated Measurement and Control (CAMAC) 1972

- ADC
- TDC
- Scaler
- Programmable…
  - Delays
  - Discriminators
  - Attenuators
  - I/Os



Power:
+/- 6V
+/- 12V
+/- 24V

Communication:
N Slot address (5 bit)
A Module address (4 bit)
F Function (5 bit)
Data bus (24 bit)

Vesa Module Eurocard (VME) 1981

- ADC
- TDC
- Scaler
- CPUs
- Programmable…
  - Delays
  - Discriminators
  - Attenuators
  - I/Os

VMEIO - 2009

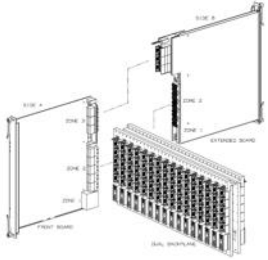
CAEN V1720 8ch, 12bits@250Msps

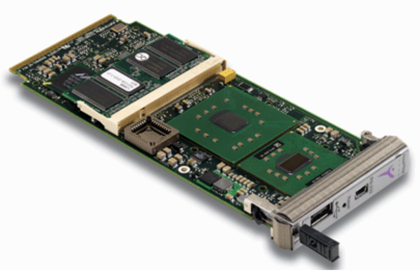
Power:
+/- 5V
+/- 12V
+/- 3.3V

Communication:
Address bus (32 bit)
Data bus (32 bit)
Control bus (IRQ, AM, …)

Advanced Telecommunication Computing Architecture (ATCA, uTCA)

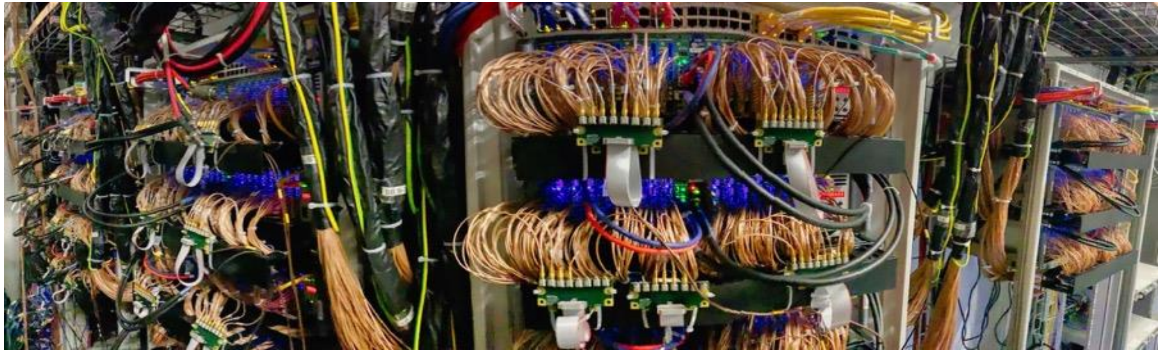
- Defined by PICMG.org
- High redundancy (99.999% availability) for telecommunication
- Redundant -48V Power
- Dual star serial links with 100 Gb Ethernet over backplane
- Read Transition Modules
- Shelf manager





WaveDAQ

- Developed at **PSI**
- 3HE full custom backplane with dual star **GBit links**
- Intelligent power supply with **shelf management**
- Used in **MEG** experiment with 9000+ channels 5 GSPS/12bit

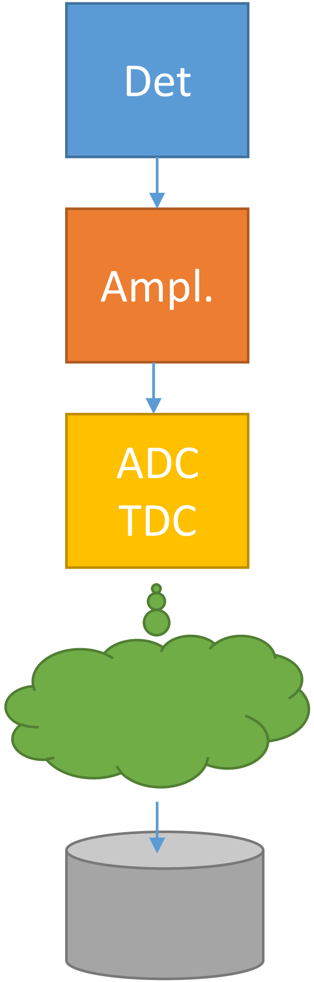


Data Acquisition Systems

Software Part between Digitizers and Storage

Data Acquisition (DAQ)

- We have
  - **Detectors** producing electrical signal
  - Analog **electronics** to condition/shape the signal
  - **Digitizers** for amplitude, charge, time
- We want
  - Define an "**event**" as a collection of data belonging to one physics process (e.g. particle decay)
  - **Read** digitized data from hardware
  - **Combine** data from several detectors
  - **Store** data on permanent medium (disk, tape)



Requirements for a DAQ system

- Experiment **independent**, read all types of hardware
- Typically **10-10,000** channels (will not cover LHC)
- Highly **configurable**
- **”Run concept”:** Data collected during defined experiment conditions
- **Robust**
- Should **not rely** on “trendy” hard- and software
  (will it run in 10 years?)
- Efficient and **performant**, typically 100-1000 MB/s
- Include “**slow control**” (temperatures, pressures, …) with plots over time (“History”)
- **Good features**: Central configuration, Alarms, Data monitoring,
  Single Event Display, Communication between shifters
- **Remote** (web) controllable

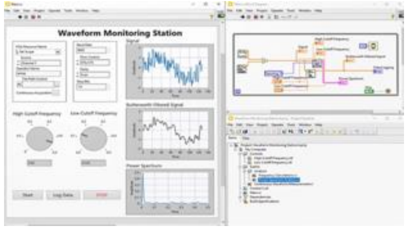
Writing **DAQ** software is orders of magnitude more **complicated** than writing simulation or analysis code

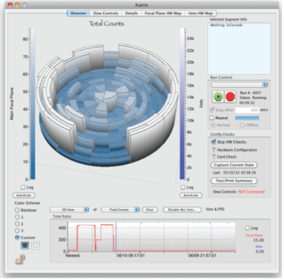
DAQ programming is the “**master discipline**” of coding

Overview of DAQ systems

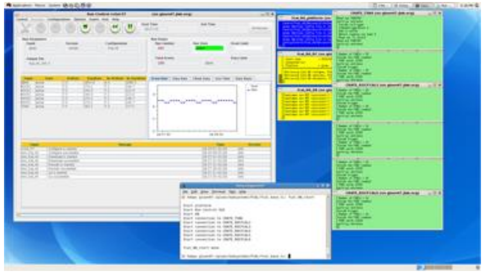
- Most physics lab have their own DAQ system and experts
- **Labview**
  - Commercial system from National Instruments Corp.
  - Works well for small setups
  - Drivers for many devices, NI hardware
  - Writing own drivers can be tricky
- **ORCA**
  - Developed at Univ. North Carolina
  - Runs only on MacOS
  - Experiments: KATRIN, MAJORANA, SNO+
- **Artdaq**
  - Developed by Fermilab
  - Based on art offline framework (originally form CMS)
  - Experiments: LARiAT, Darkside-50, Mu2e
- **Midas-UK**: Multi Instance Data Acquisition System (Rutherford – STFC)
- **CODA**
  - Developed at Jefferson Lab and used for experiments there
  - Relies on special readout controller
- And many more…

Labview





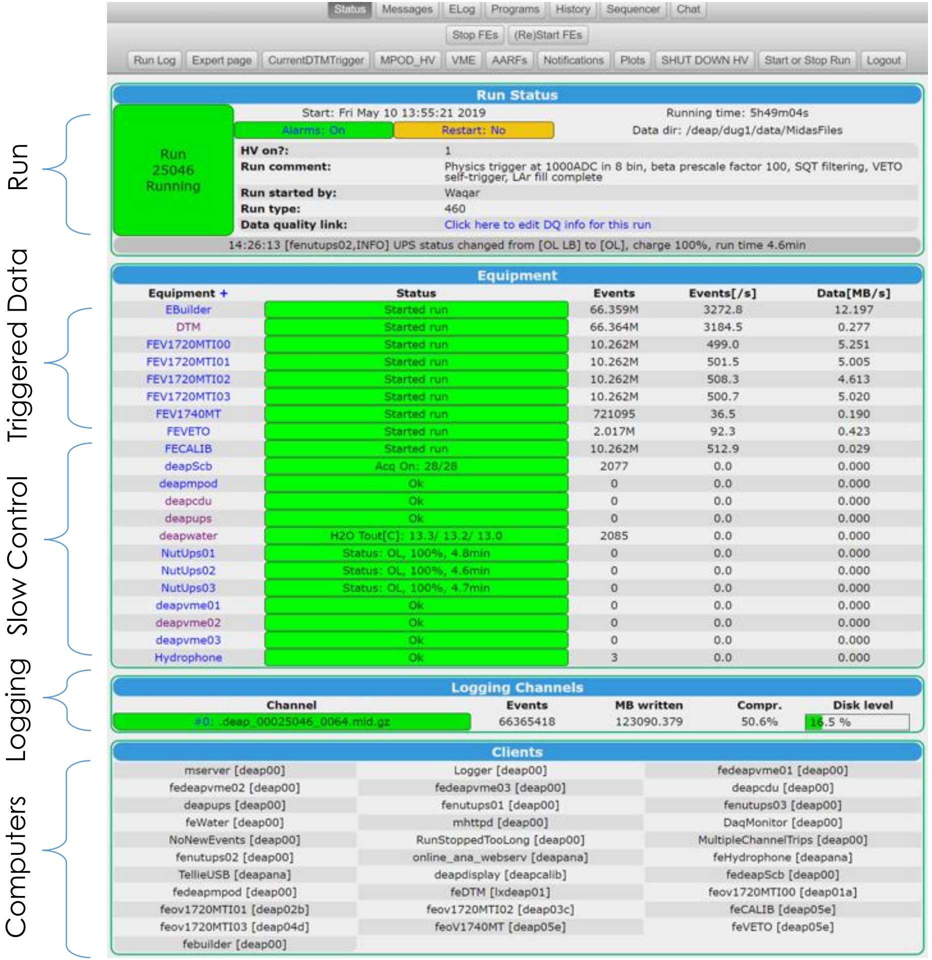
ORCA



CODA

MIDAS system

- Development started in **1993** at **PSI**, Switzerland joined by **TRIUMF**, CA in **1996**
- Today used at **PSI** and **TRIUMF** as the standard system, plus **CERN** (Alpha-g), **KEK** (T2K), **Fermilab** (g-2), …
- Maximum Integrated Data Acquisition System
  - Written in C++, JavaScript
  - Integrated **Slow Control**
  - Operating system / hardware **independent**
  - Quick installation
  - Easy customization
  - **Free** (GPL)
  - Good for 1-50 DAQ computers and **~1 GB/s** data rate
- https://midas.triumf.ca



Run Status

Run 25046 Running

Start: Fri May 10 13:55:21 2019

Running time: 5h49m04s

Alarms: On

Restart: No

Data dir: /deap/dug1/data/MidasFiles

HV on?: 1

Run comment: Physics trigger at 1000ADC in 8 bin, beta prescale factor 100, SQT filtering, VETO self-trigger, LAr fill complete

Run started by: Waqar

Run type: 460

Data quality link: Click here to edit DQ info for this run

14:26:13 [fenutups02,INFO] UPS status changed from [OL LB] to [OL], charge 100%, run time 4.6min

Equipment

Equipment +	Status	Events	Events[/s]	Data[MB/s]
EBuilder	Started run	66.359M	3272.8	12.197
DTM	Started run	66.364M	3184.5	0.277
FEV1720MTI00	Started run	10.262M	499.0	5.251
FEV1720MTI01	Started run	10.262M	501.5	5.005
FEV1720MTI02	Started run	10.262M	508.3	4.613
FEV1720MTI03	Started run	10.262M	500.7	5.020
FEV1740MT	Started run	721095	36.5	0.190
FEVETO	Started run	2.017M	92.3	0.423
FECALIB	Started run	10.262M	512.9	0.029
deapScb	Acq On: 28/28	2077	0.0	0.000
deapmpod	Ok	0	0.0	0.000
deapcdu	Ok	0	0.0	0.000
deapups	Ok	0	0.0	0.000
deapwater	H2O Tout[C]: 13.3/ 13.2/ 13.0	2085	0.0	0.000
NutUps01	Status: OL, 100%, 4.8min	0	0.0	0.000
NutUps02	Status: OL, 100%, 4.6min	0	0.0	0.000
NutUps03	Status: OL, 100%, 4.7min	0	0.0	0.000
deapvme01	Ok	0	0.0	0.000
deapvme02	Ok	0	0.0	0.000
deapvme03	Ok	0	0.0	0.000
Hydrophone	Ok	3	0.0	0.000

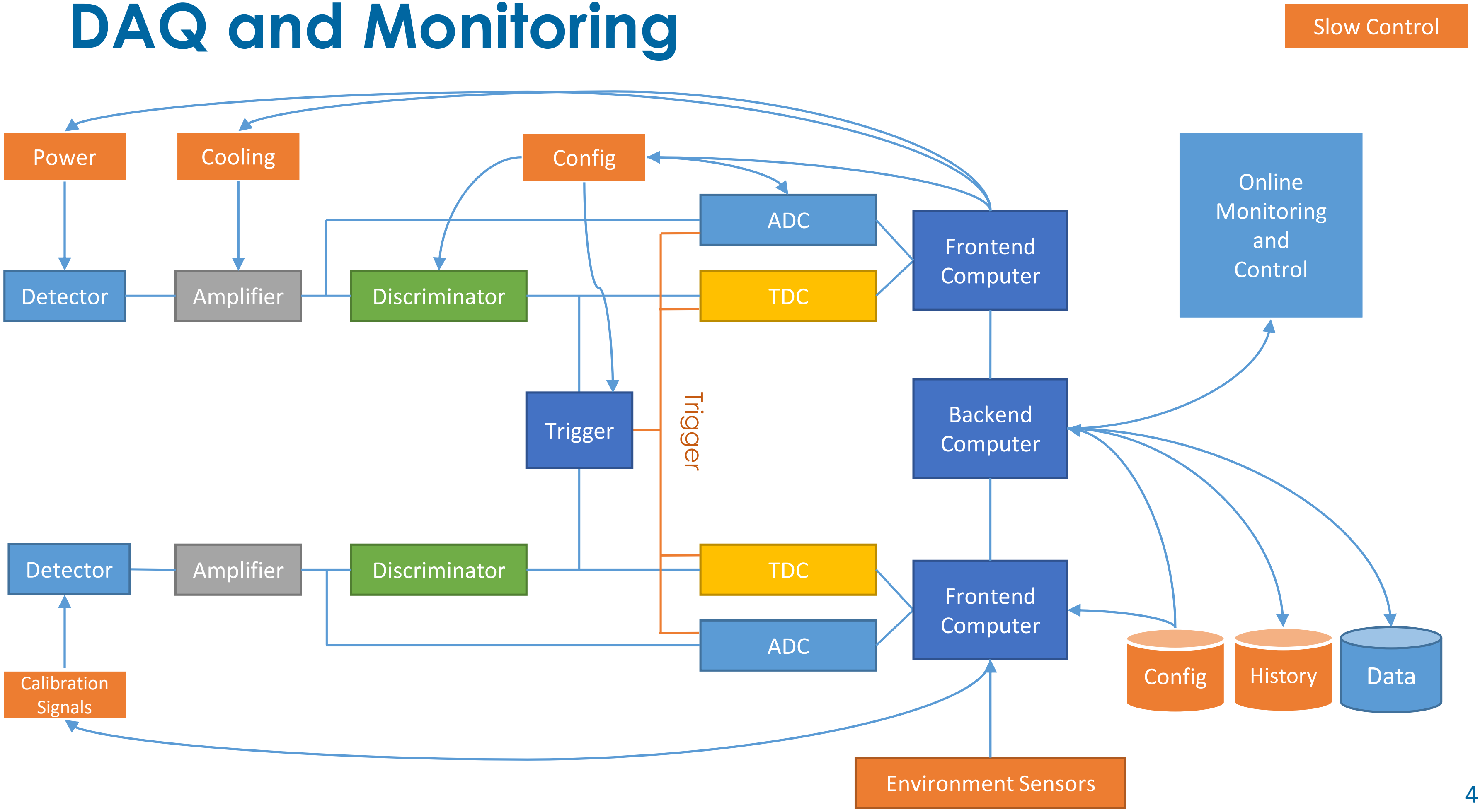
Logging Channels

Channel	Events	MB written	Compr.	Disk level
#0: .deap_00025046_0064.mid.gz	66365418	123090.379	50.6%	16.5 %

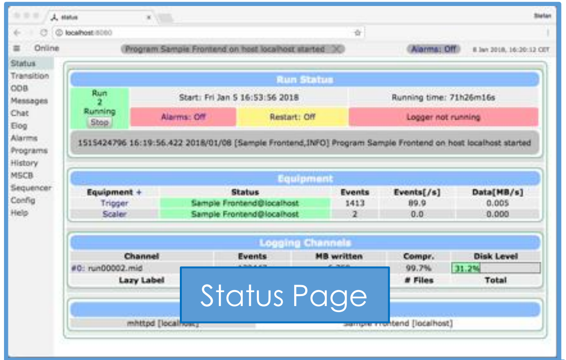
Clients

mserver [deap00]	Logger [deap00]	fedeapvme01 [deap00]
fedeapvme02 [deap00]	fedeapvme03 [deap00]	deapcdu [deap00]
deapups [deap00]	fenutups01 [deap00]	fenutups03 [deap00]
feWater [deap00]	mhttpd [deap00]	DaqMonitor [deap00]
NoNewEvents [deap00]	RunStoppedTooLong [deap00]	MultipleChannelTrips [deap00]
fenutups02 [deap00]	online_ana_webserv [deapana]	feHydrophone [deapana]
TellieUSB [deapana]	deapdisplay [deapcalib]	fedeapScb [deap00]
fedeapmpod [deap00]	feDTM [lxdeap01]	feov1720MTI00 [deap01a]
feov1720MTI01 [deap02b]	feov1720MTI02 [deap03c]	feCALIB [deap05e]
feov1720MTI03 [deap04d]	feoV1740MT [deap05e]	feVETO [deap05e]
febuilder [deap00]		

DAQ and Monitoring



MIDAS in a nutshell



Program Sample Frontend on host localhost started

Alarms: Off

8 Jan 2018, 16:20:12 CET

Run Status

Run 2 Running	Start: Fri Jan 5 16:53:56 2018		Running time: 71h26m16s
	Alarms: Off	Restart: Off	Logger not running

1515424796 16:19:56.422 2018/01/08 [Sample Frontend,INFO] Program Sample Frontend on host localhost started

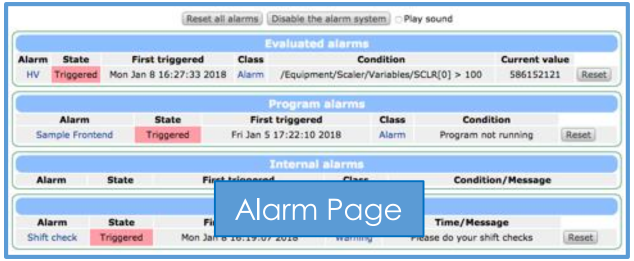
Equipment

Equipment +	Status	Events	Events[/s]	Data[MB/s]
Trigger	Sample Frontend@localhost	1413	89.9	0.005
Scaler	Sample Frontend@localhost	2	0.0	0.000

Logging Channels

Channel	Events	MB written	Compr.	Disk Level
#0: run00002.mid			99.7%	31.2%
Lazy Label			# Files	Total

Status Page



Evaluated alarms

Alarm	State	First triggered	Class	Condition	Current value
HV	Triggered	Mon Jan 8 16:27:33 2018	Alarm	/Equipment/Scaler/Variables/SCLR[0] > 100	586152121

Program alarms

Alarm	State	First triggered	Class	Condition
Sample Frontend	Triggered	Fri Jan 5 17:22:10 2018	Alarm	Program not running

Internal alarms

Alarm	State	First triggered	Class	Condition/Message

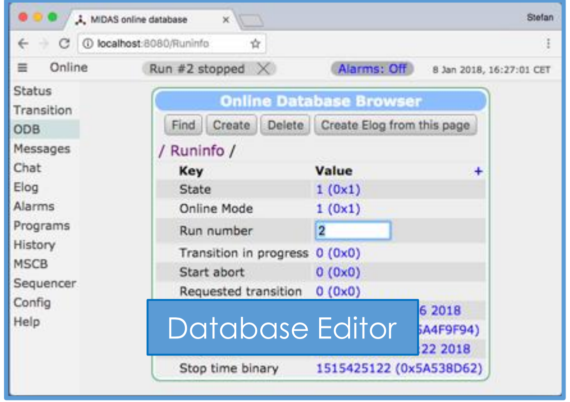
Alarm	State			Time/Message
Shift check	Triggered			Please do your shift checks

Alarm Page

History

Group: Xenon Panel: Xe pressures ☐ Keep horizontal axis when switching panels

History Display

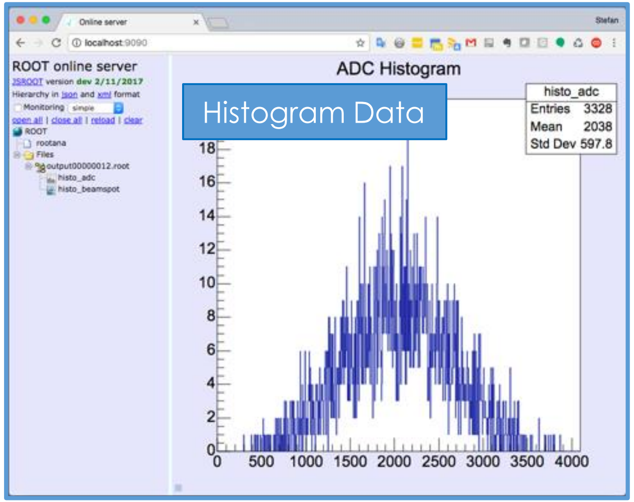


Online Database Browser

/ Runinfo /

Key	Value
State	1 (0x1)
Online Mode	1 (0x1)
Run number	2
Transition in progress	0 (0x0)
Start abort	0 (0x0)
Requested transition	0 (0x0)
	6 2018
	5A4F9F94)
	22 2018
Stop time binary	1515425122 (0x5A538D62)

Database Editor



ROOT online server

JSROOT version dev 2/11/2017

Hierarchy in json and xml format

☐ Monitoring simple

open all | close all | reload | clear

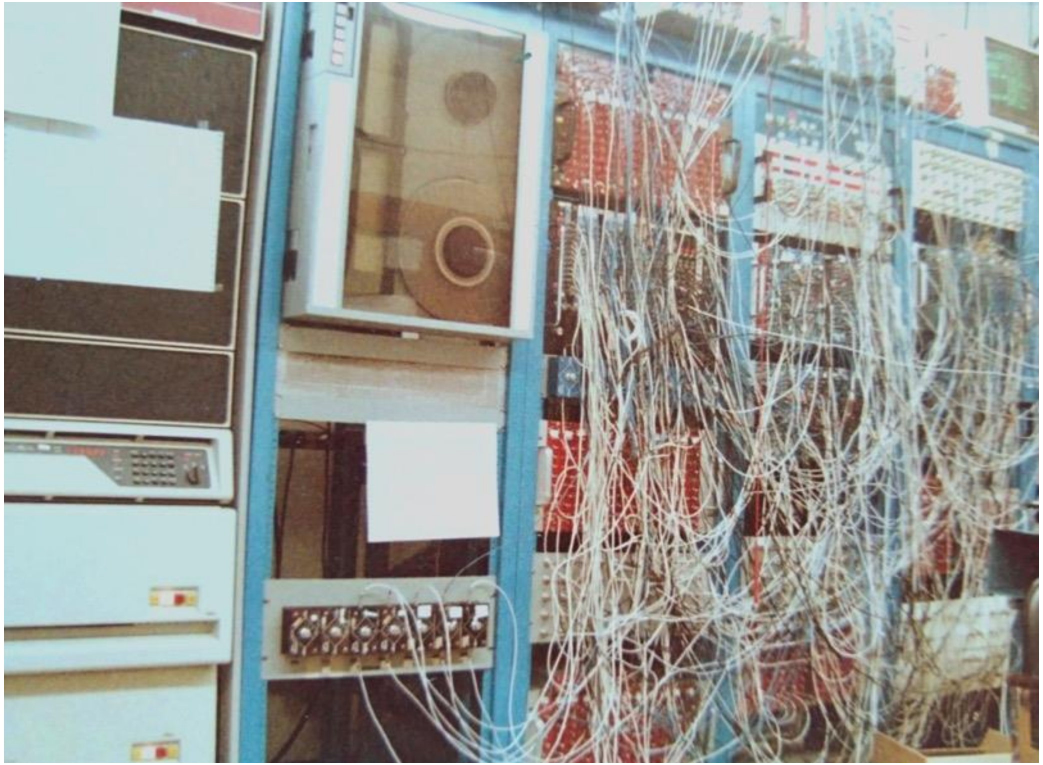
Histogram Data

!!!!! Please do not touch unless you are asked by an expert !!!!!

Custom Page

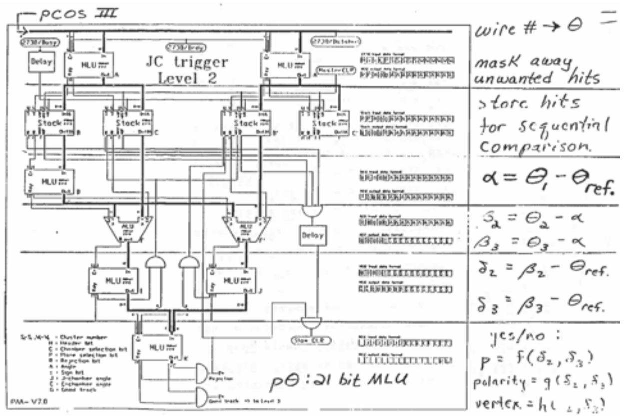
π-scat Experiment, TRIUMF

- Period: < **1985**
- Channel Count: <100
- DAQ Hardware: **NIM**, **CAMAC** [ADCs, TDCs, Scalers]
- Computer: **Digital PDP** 11/34
- Rates: 100 events/s
- Programming Language: FORTRAN
- Storage: Memorex MRX-V ½"x 10-¾"



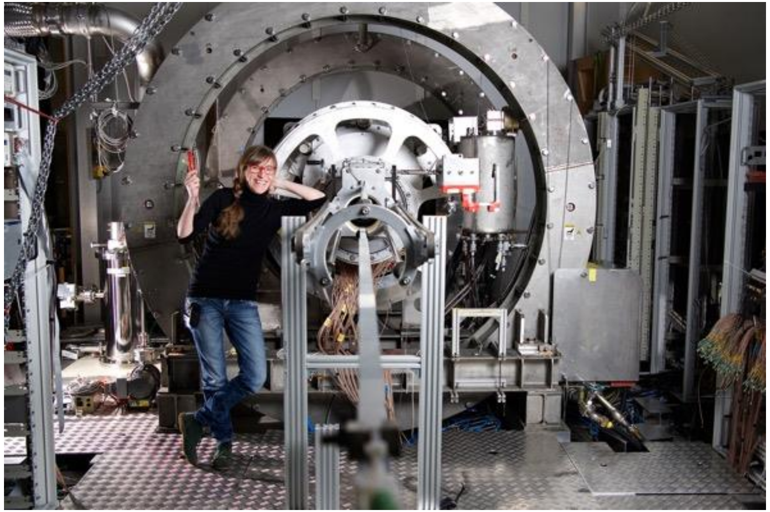
CHAOS Experiment, TRIUMF

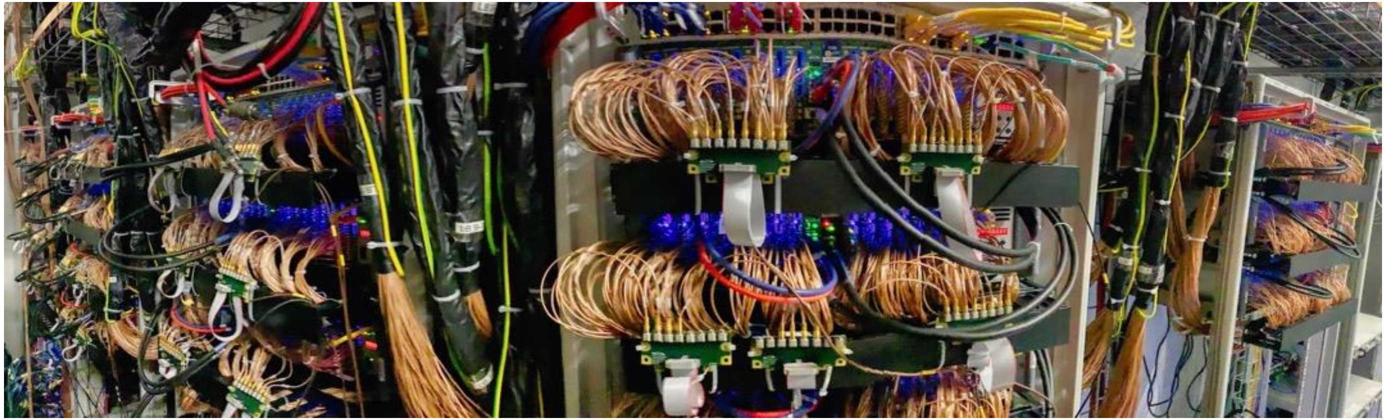
- Period: **1990 - 2000**
- Channel Count: ~2500
- DAQ Hardware: **NIM, CAMAC, VME, FastBus**
- Trigger **FPGA Precursor** in CAMAC
  (Added, Multiplier, Stack)
- Computer: Digital **µVax-3400**
- Rates: ~100 events/s
- Programming Language: FORTRAN
- Storage: DLTape IV 80GB (compressed)

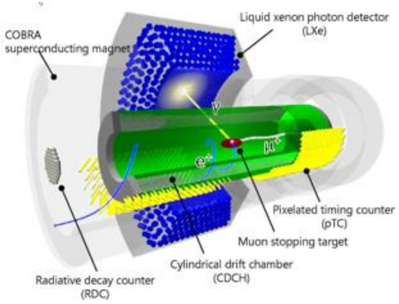


MEG II Experiment, PSI

- Period: **2008 -**
- Channel Count: ~9000
- DAQ Hardware: Custom **WaveDAQ crate** with DRS4 chip (5 GS/s, 12 bit)
- Sophisticated FPGA trigger
- Computer: FPGA Frontend (Xilinx Zynq), **40-core backend PC**
- Rates: 30 events/s, 3 MB events, ~100 MB/s
- Software: MIDAS, ROOT
- Storage: Local SDD (4TB), PSI cluster (1.5 PB)

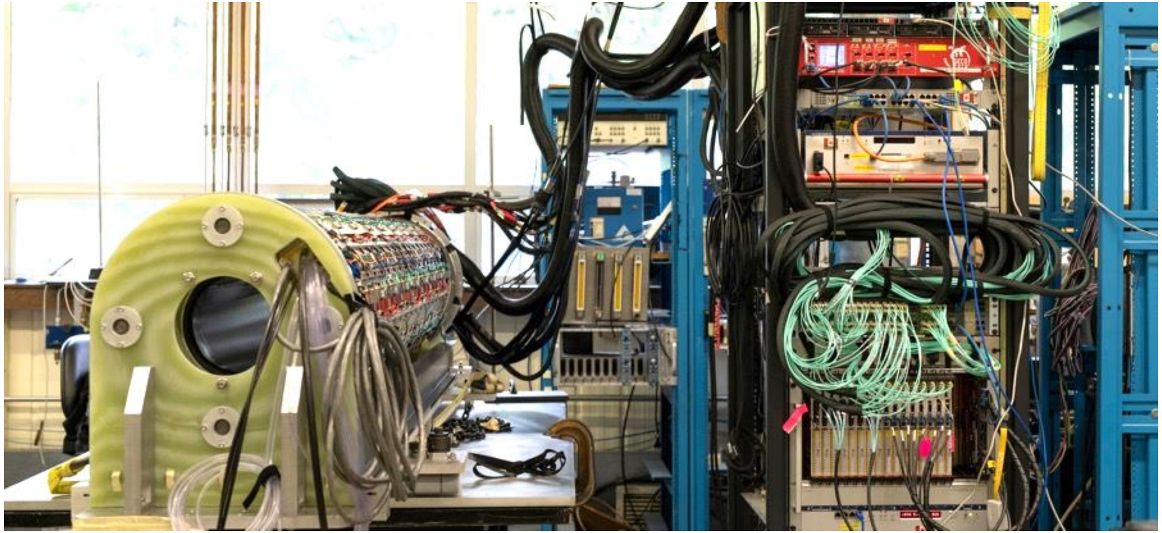






Alpha-g Experiment, CERN

- Period: **2016 -**
- Channel Count: ~19’000!
- DAQ Hardware: **VME** (for power only)
  Frontend Electronics **on detector** with Ethernet Optical Links
- Custom Build Hardware with FPGAs : WFDs, TDCs, Logic
- Computer: **PCs**
- Rates: ~1000 events/s, ~200 MB/s
- Software: MIDAS, C, C++, Web tools
- Storage: Local HDD, Cloud



- Electronics and DAQ are **essential** to make new **discoveries**
- To work on DAQ, a **broad** set of evolving **skills** is necessary
  - Detector Technology
  - Analog and Digital Electronics
  - FPGA programming
  - Serial Links, Networking
  - Multi-thread programming
  - Cluster computing
  - User Interfaces
  - …
- Skills can only be obtained in **hands-on environments**
- **Many thanks to**
  - Pierre-André Amaudruz for some slides
  - IEEE Nuclear and Plasma Sciences Society for sponsoring this lecture