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Design and testing of a reconfigurable AI ASIC for Front-end Data Compression at the HL-LHC

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We have designed and implemented a reconfigurable ASIC data encoder for low-power, low-latency hardware acceleration of an unsupervised machine learning data encoder. The implementation of a complex neural network algorithm demonstrates the effectiveness of a high-level synthesis-based design automation flow for building design IP for ASICs. The ECON-T ASIC, which includes the AI algorithm, enables specialized compute capability and has been optimized for data compression at 40\,MHz in the trigger path of the High-Granularity Endcap Calorimeter (HGCal), an upgrade for the Compact Muon Solenoid (CMS) experiement for the high-luminosity LHC (HL-LHC). The objective encoding can be reconfigured based on detector conditions and geometry by updating the trained weights. The design has been implemented in an LP CMOS 65˜nm process. It occupies a total area of 2.9\,mm2, consumes 48˜mW of power and is optimized to withstand approximately 200˜MRad ionizing radiation. This talk will present the design methodology and initial results from testing the algorithm in silicon.

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