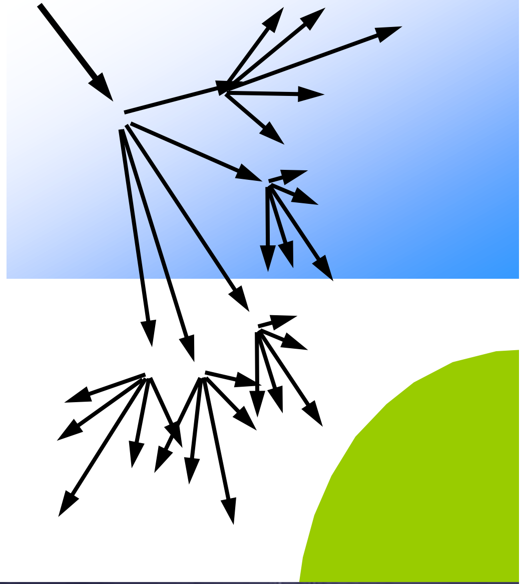

Atmospheric Neutron Effects in Advanced Microelectronics

An introduction and a Real-Time concern

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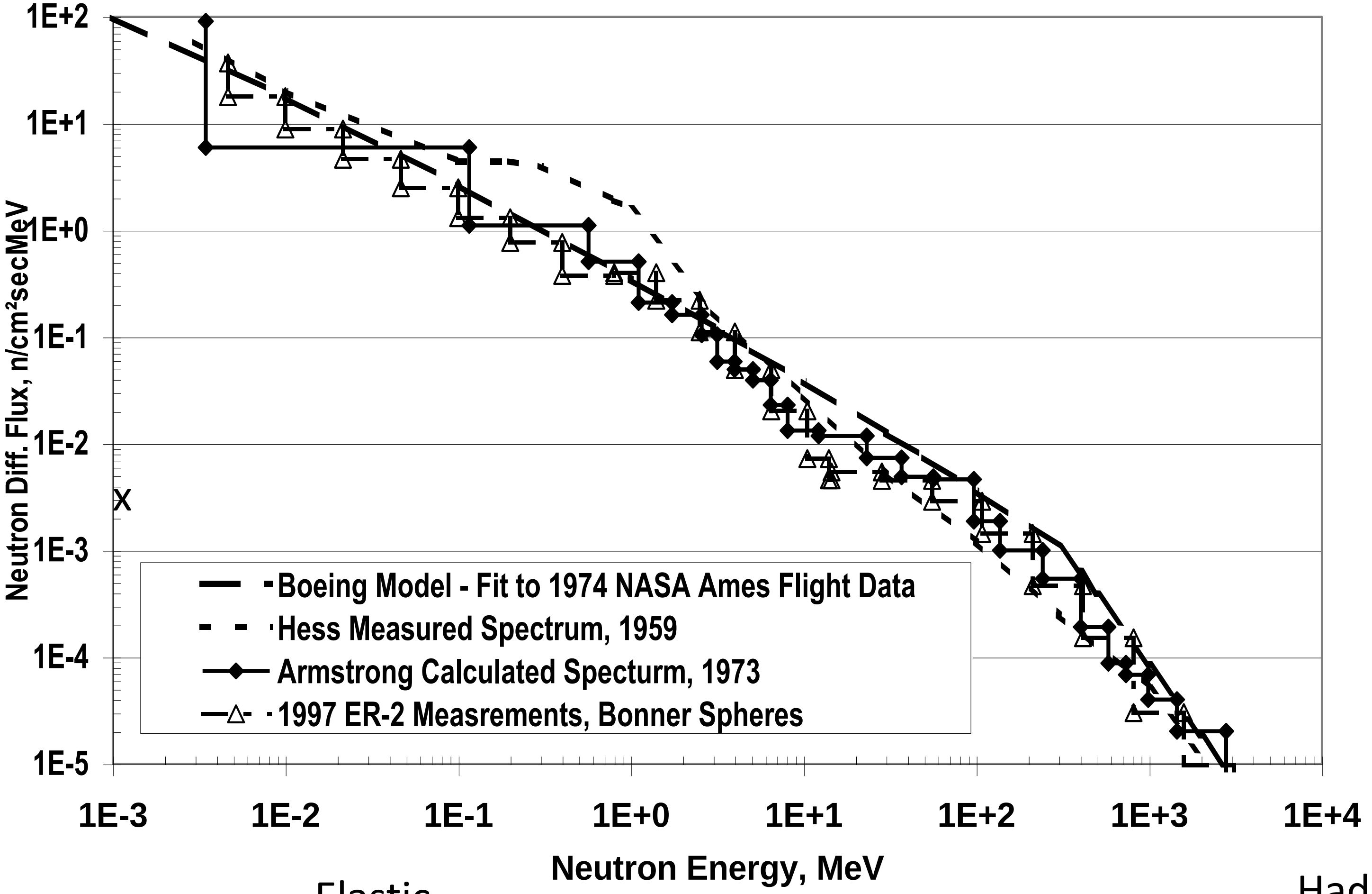
1st Aug. 2022

23rd Real Time Conference

Radiations are pervading everywhere!
Focus on particles with largest ionizing rate (dE/dx)

Nature	neutrons?	Or else..
Galactic Cosmic Rays	/	ions…
Solar Flares	/	p, e, light ions…
Radiation Belts	/	p and e
In large space stations as ISS	some, because of spacecraft structure mass	
Atmosphere	yes, peak at 18km	along with hadron, mesons, muons(-), ..
Ground	yes,	mostly with muons (-)
From underground (U and Th decay)	/	mostly alphas
Human made		
Radiotherapy/target areas	Yes	
Fission	Yes (usually confined in water-filled vessels)	
Fusion research	More or less/Heavy shield around plasma vessel	
HEP/Experimental areas/tunnels	Yes	

Natural atmospheric neutron flux spectrum at ground level after interactions in the atmosphere (O and N)



thermalisation ←

Elastic
collisions
1/E spectrum

Low energy
Nuclear physics ←

Spallation

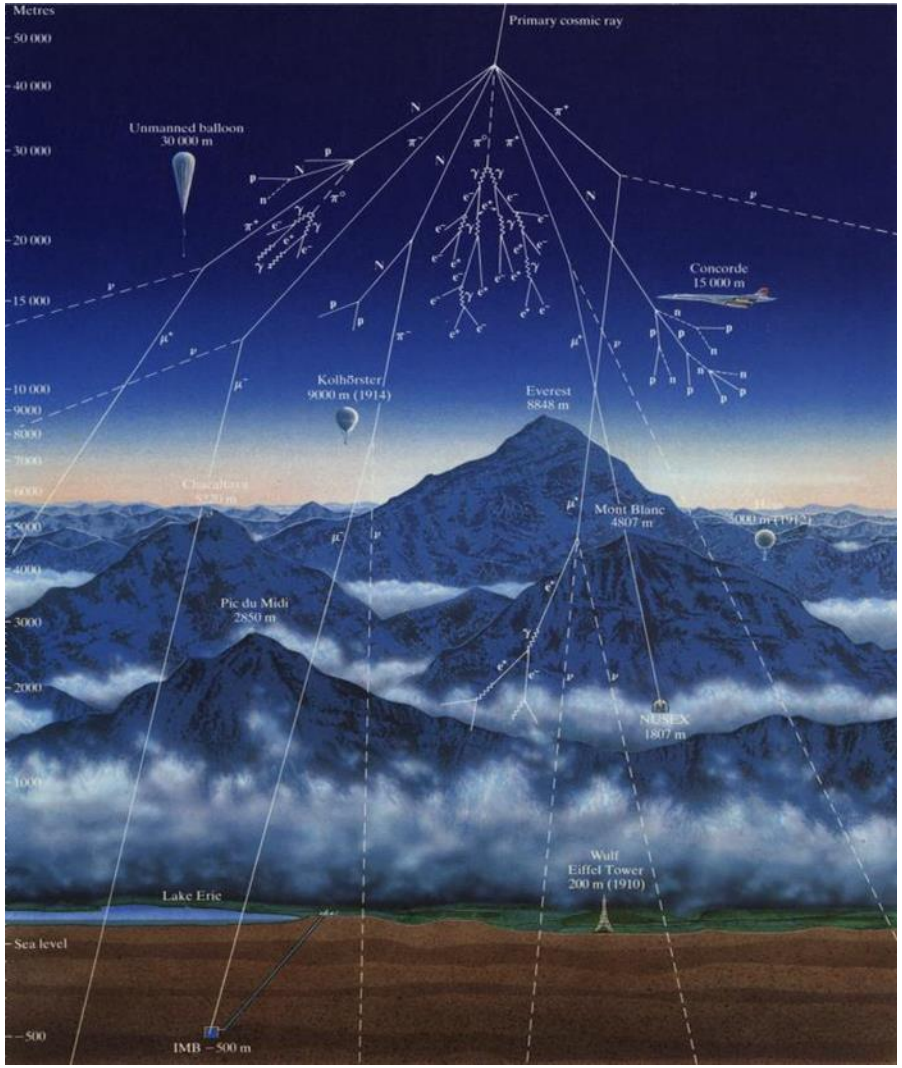
cascades ←

Hadronic
physics

Cosmic Rays
>> GeV ←

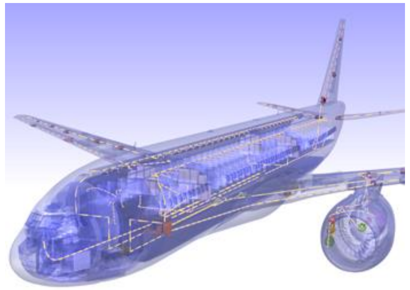
(reference JESD89A: standard

Geophysics of cosmic natural radiation in the atmosphere and at gound level

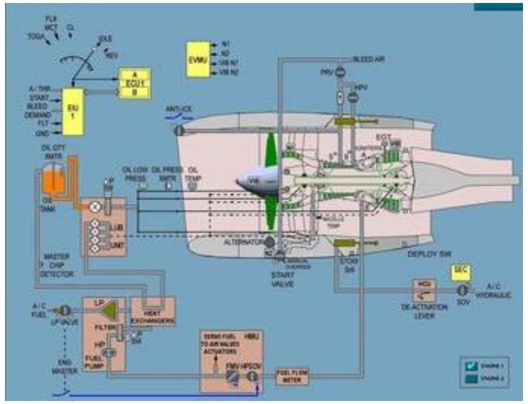


=> Concerns: Global safety of transportation

Atmospheric:



Aircraft builders
Reliability in time
Certification Authorities
Stingent safety specifications
Plane: < 1 event per 10^7 flightxhours



Main parts providers
Reliability in time
Certification Authorities
Stingent specification
Flight computer, Autopilot,
Engine Controlers
< 1 event per 10^7 flight hour
=> Electronic device < 1 event per 10^9 flightxhours

Other concerns at Ground level:

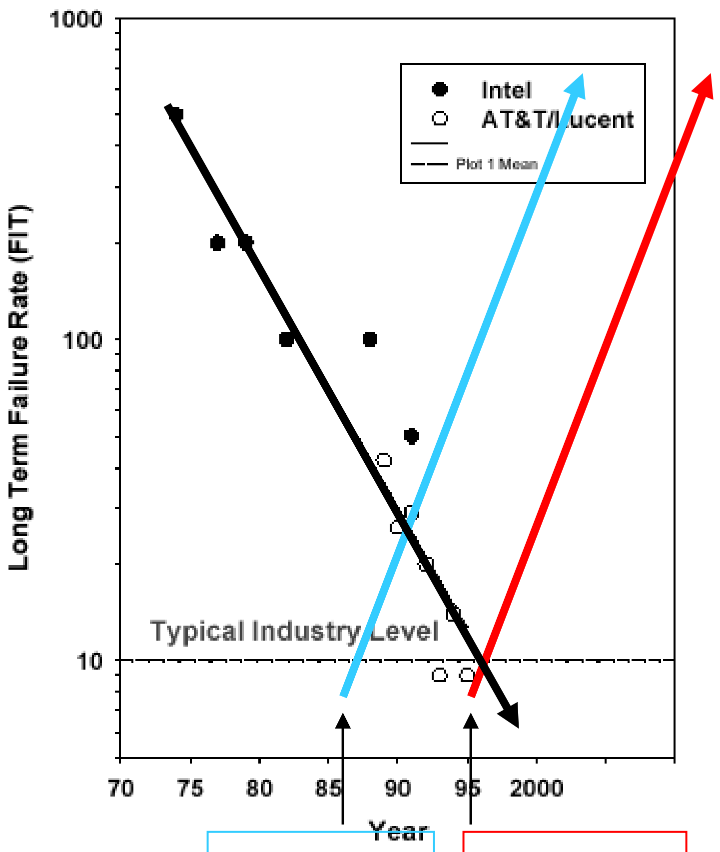
- **More electric automotive**
- **More Information Technology dependable systems**
  - **Internet backbone**
  - **high-end servers and computers**

CMOS reliability continously improved by manufacturing tremendous progress (if we disregard radiation radiation effects)

Conversely, the Effects of Additional Radiation Became clearly visible.

Process-Induced Reliability MTBF (long term "Failure in Time")

Historical IC Failure Rates



Airplane Altitude early 90's

Sea Level 2000's

BUT
due ever increasing circuit sensitivity to natural particle
environment

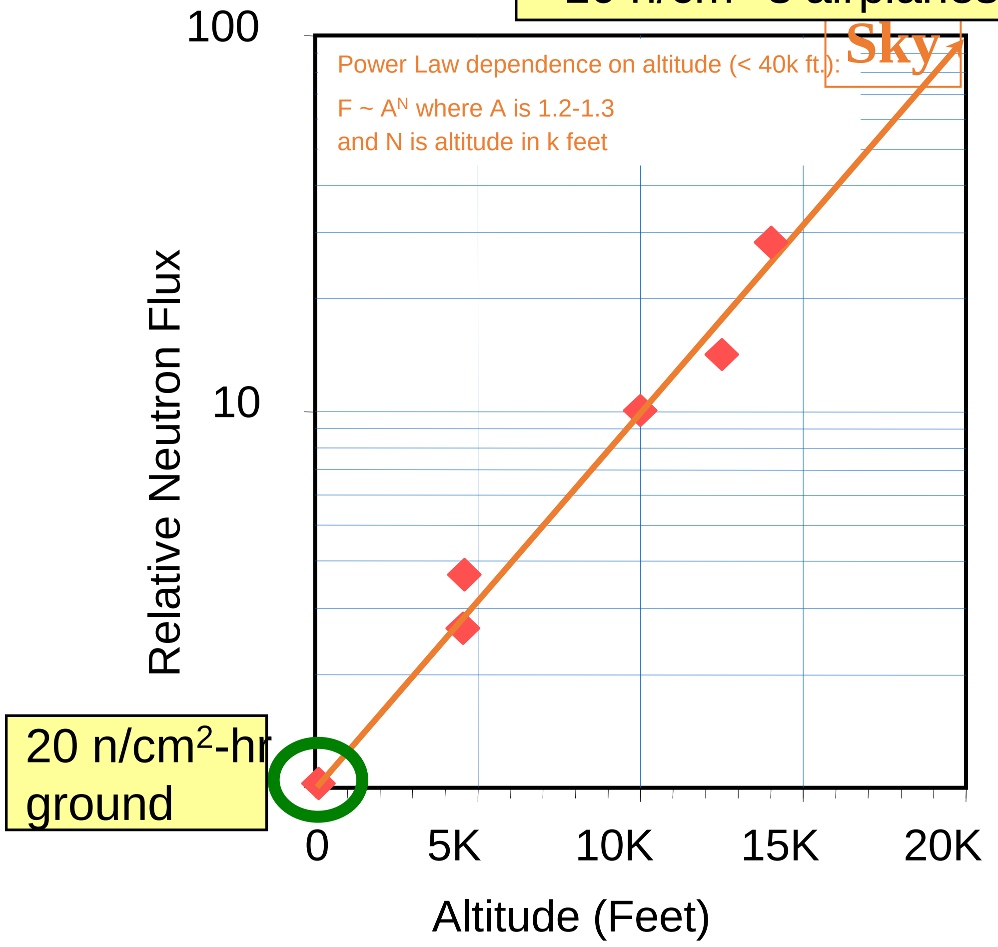
Especially visible in Everyday Vehicles or High Security Business (Airplanes, Automotives, Railways, Internet Routers..)

INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM 2002
Reliability Issues for Advanced
IC Technologies Anthony S. Oates

Atmospheric Neutron flux
at Ground level = where Consumer electronics runs and population is living

Neutron Flux vs. Altitude

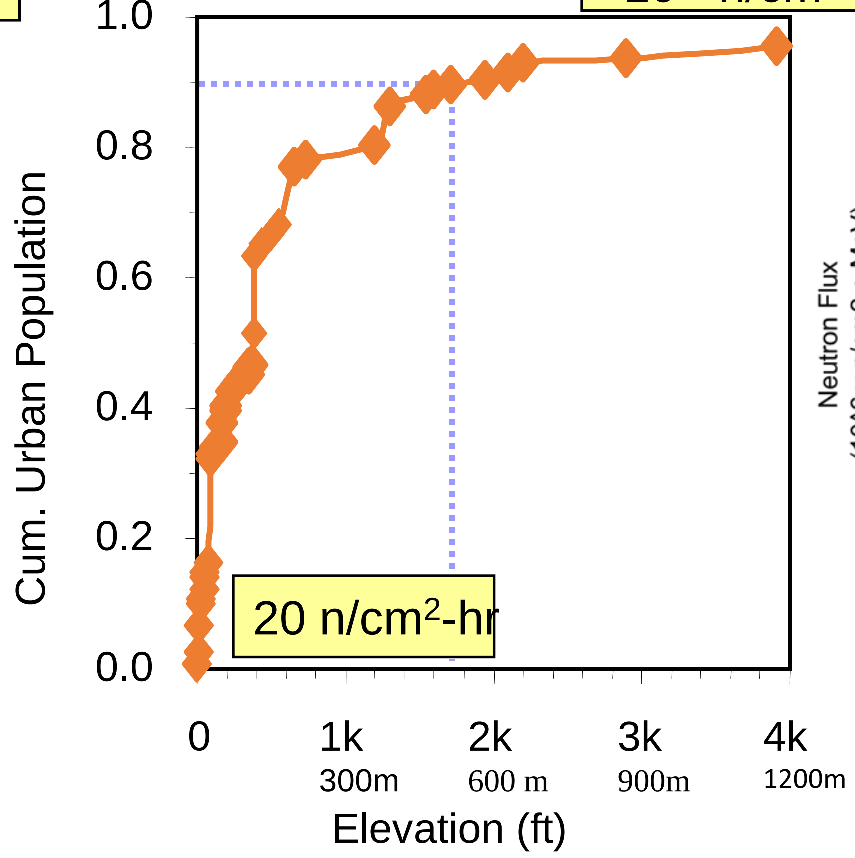
2000 to 3000 n/cm^2-hr
~10 n/cm^2-s airplanes



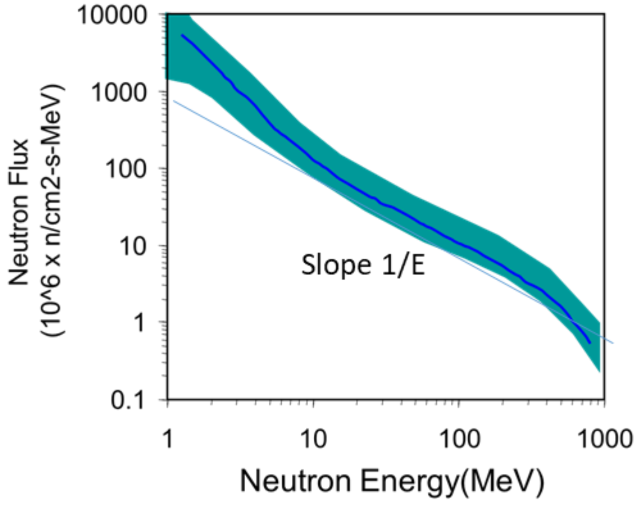
20 n/cm^2-hr
ground

Urban Pop. vs. Altitude

40 n/cm^2-hr
10^{-2} n/cm^2-s



20 n/cm^2-hr



> 1 MeV Neutron
flux @ sea-level
NY city

After Robert Bauman, Texas Instrument
RADECS CONFERENCE SHORT COURSE, Sept. 2001

Where in Real Time Effects in a detection chain ?

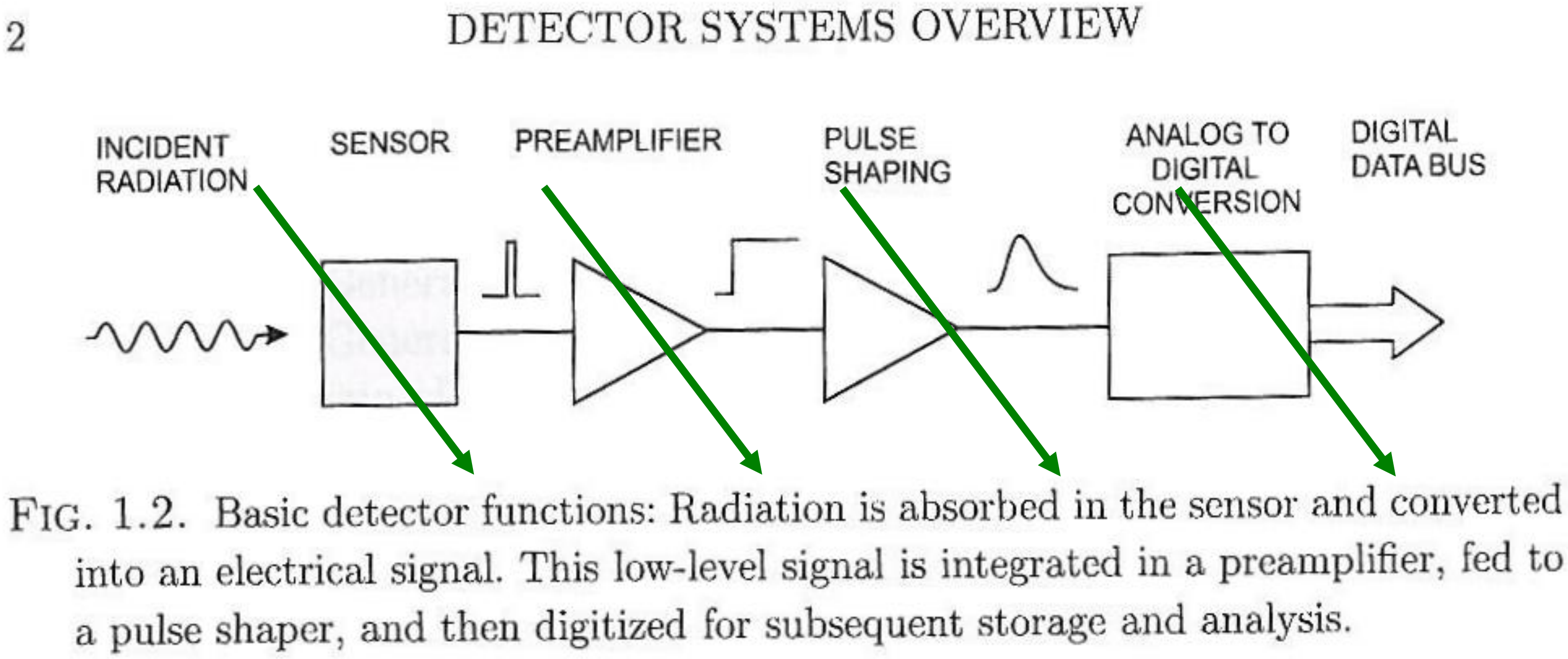


FIG. 1.2. Basic detector functions: Radiation is absorbed in the sensor and converted into an electrical signal. This low-level signal is integrated in a preamplifier, fed to a pulse shaper, and then digitized for subsequent storage and analysis.

SET

More digital and high bandwidth (Single Event Upsets, Single Event Rate, Single Event Functional Interupts)

SEU

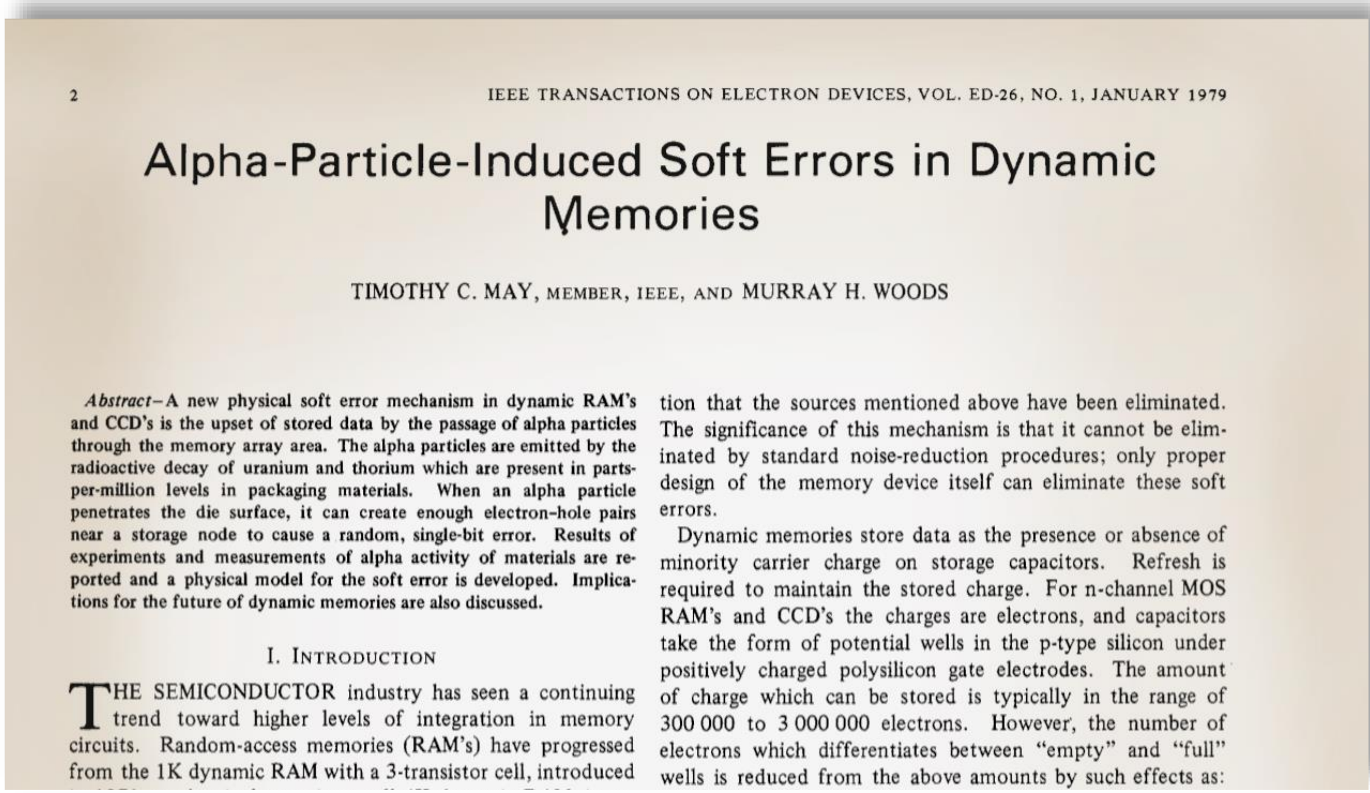
SER

SEFI

More analog and S/N ratio is critical (Single Event Transient)

First mention of a « Soft Error » 43 years ago (1979)

- In Dynamic Memory (1kb)
- Single bit at a time, random)
- Related to single alpha particle random emission from ceramic packaging
- Related to U and Th content (contaminants
- Anticipated to occur in arrays such as early SRAMS and CCDS's



2 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-26, NO. 1, JANUARY 1979

Alpha-Particle-Induced Soft Errors in Dynamic Memories

TIMOTHY C. MAY, MEMBER, IEEE, AND MURRAY H. WOODS

Abstract—A new physical soft error mechanism in dynamic RAM's and CCD's is the upset of stored data by the passage of alpha particles through the memory array area. The alpha particles are emitted by the radioactive decay of uranium and thorium which are present in parts-per-million levels in packaging materials. When an alpha particle penetrates the die surface, it can create enough electron-hole pairs near a storage node to cause a random, single-bit error. Results of experiments and measurements of alpha activity of materials are reported and a physical model for the soft error is developed. Implications for the future of dynamic memories are also discussed.

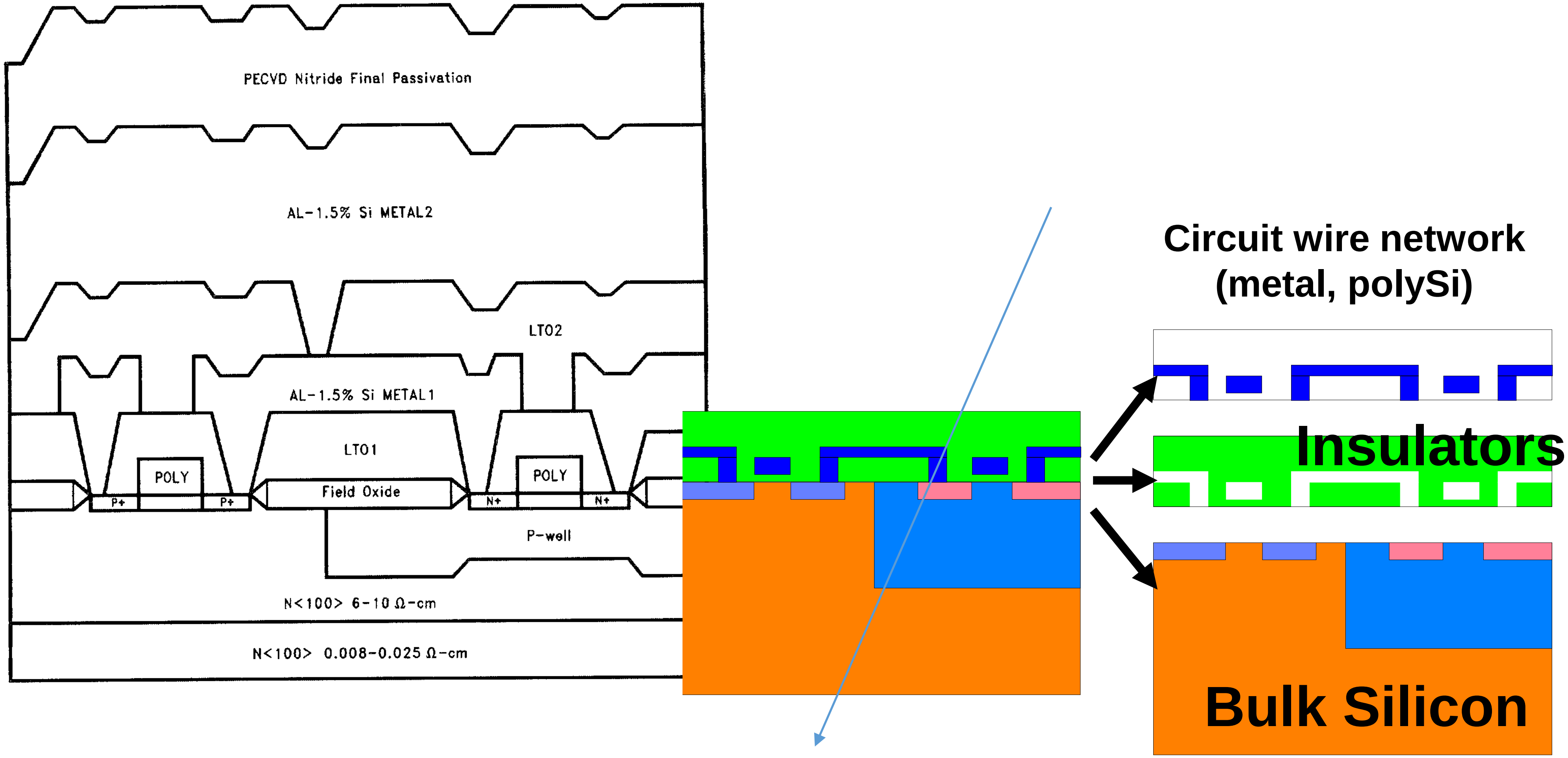
I. Introduction

THE SEMICONDUCTOR industry has seen a continuing trend toward higher levels of integration in memory circuits. Random-access memories (RAM's) have progressed from the 1K dynamic RAM with a 3-transistor cell, introduced

tion that the sources mentioned above have been eliminated. The significance of this mechanism is that it cannot be eliminated by standard noise-reduction procedures; only proper design of the memory device itself can eliminate these soft errors.

Dynamic memories store data as the presence or absence of minority carrier charge on storage capacitors. Refresh is required to maintain the stored charge. For n-channel MOS RAM's and CCD's the charges are electrons, and capacitors take the form of potential wells in the p-type silicon under positively charged polysilicon gate electrodes. The amount of charge which can be stored is typically in the range of 300 000 to 3 000 000 electrons. However, the number of electrons which differentiates between "empty" and "full" wells is reduced from the above amounts by such effects as:

Interactions in a typical IC in the 70's



Circuit wire network (metal, polySi)

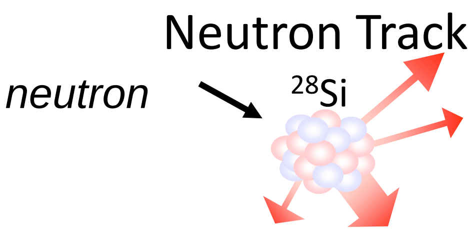
Insulators

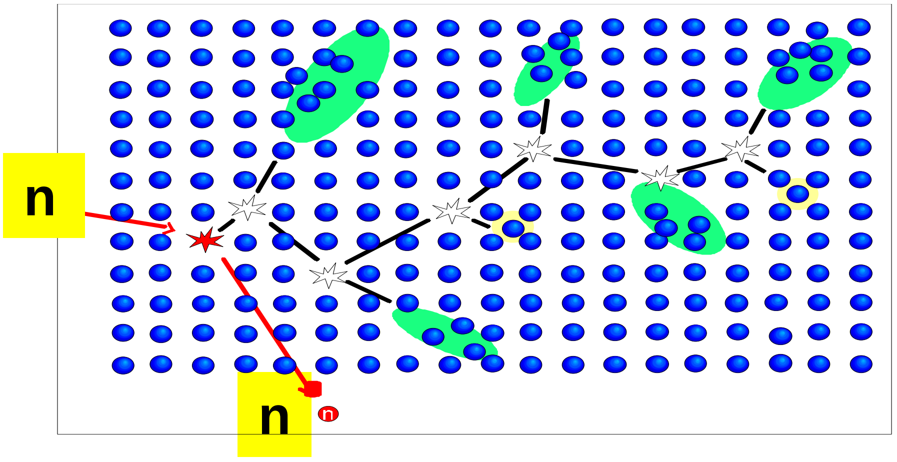
Bulk Silicon

FACT^{TM} 54ACxx 2 µm CMOS

Silicon Devices as Particle Detectors of neutrons

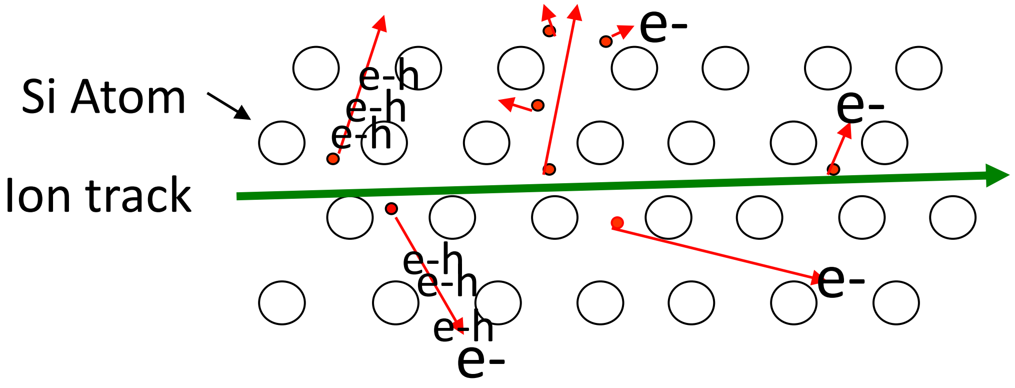
- Indirect Nuclear Process first
- Then Direct Coulombic Process due to “recoil” ions liberated





Secondary Ion Tracks

(« recoils »)

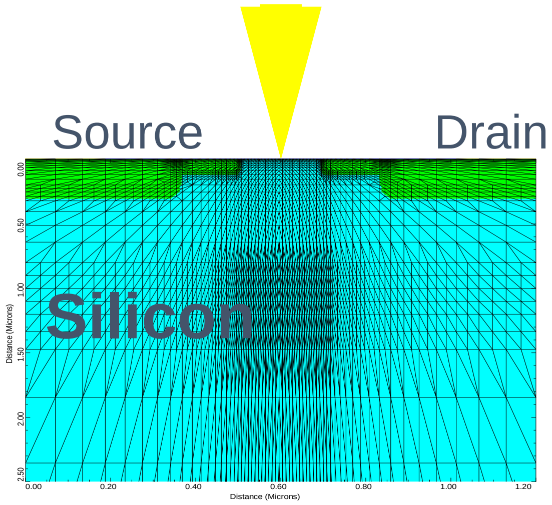


e-h = electron hole pair

=> Ioniziation: up to 10 fC/µm along the track

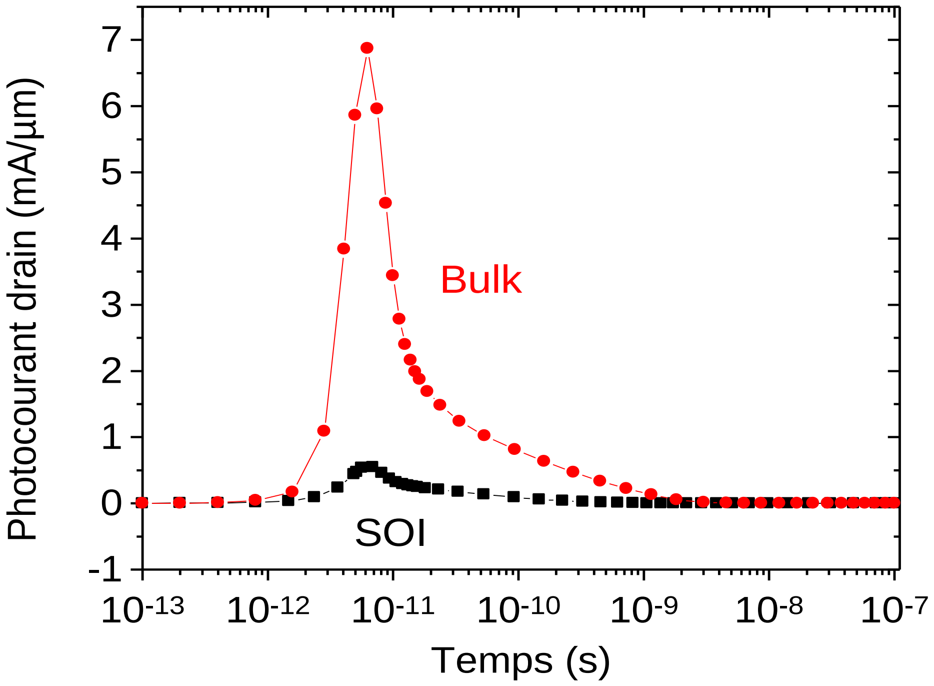
We go back of the basic of a transistor

Bulk Silicon



Mostly a ΔE mode detector

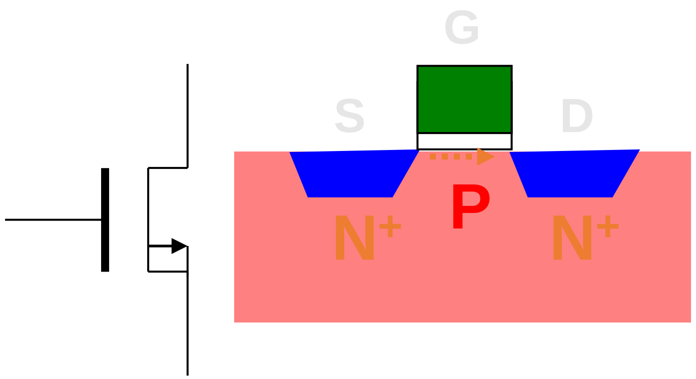
Vastly sort of pixelized in a 2D if not 3D array

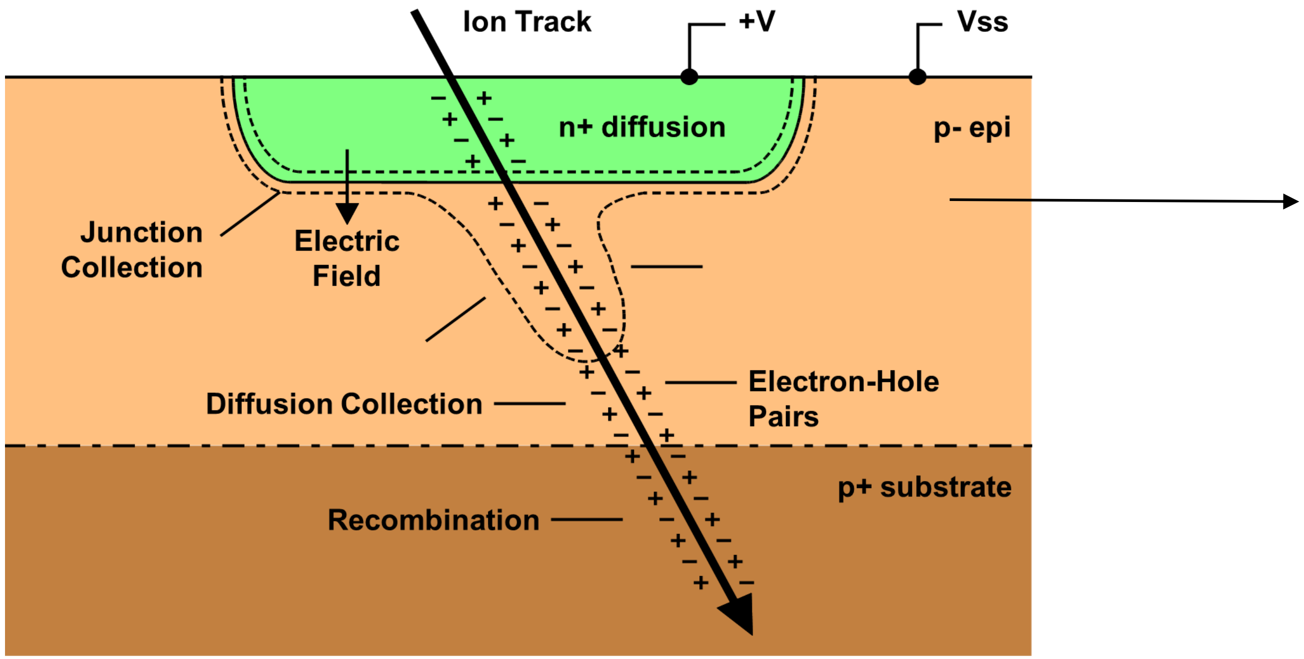


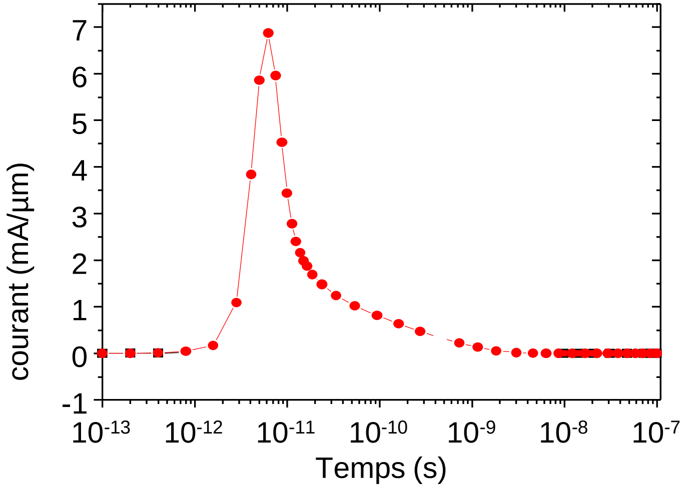
Bulk Silicon
vs.
Thin Silicon on Insulator

Effect of one charged particle
Radiation and Hard or Soft Errors

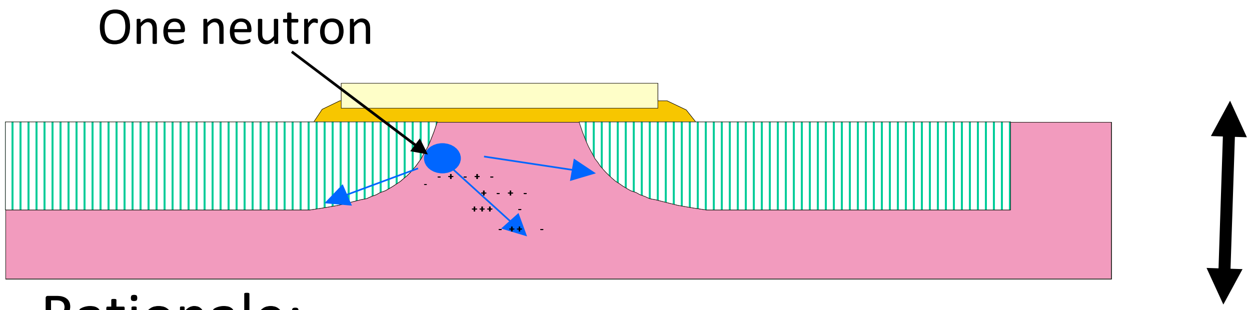
A single particle hit excites between
1 000 and 100 000 electrons and holes
/micron in a typical semiconductor
= 0.16 to 16 1^{E}-15 coulomb/µm







SCALING - Orders of magnitude in case of atmospheric neutrons



Sensitive Layer 1 µm approx

Rationale:

- Probability that a neutron hit a silicon atom near a transistor and randomly generate recoils witch trigger a signal
- Assumptions
  - $\sigma_{nuclear}$, order of magnitude 1 barn ;
  - 28Si (10B as a dopant to silicon also is of concern for thermal neutrons)
  - Active layer in silicon wafer ~ a layer of 1 µm where the transistors stan

=> Probability of a signal ~ approx. 10^{-5} per incoming neutron

<u>Consequence, a</u> serious Reliability Issue..

- **at sea level: 10 neutron/cm^2/hour**

  $\Rightarrow$10 x 10^{-5} = 10^{-4} transient per hour per cm^2 of circuit

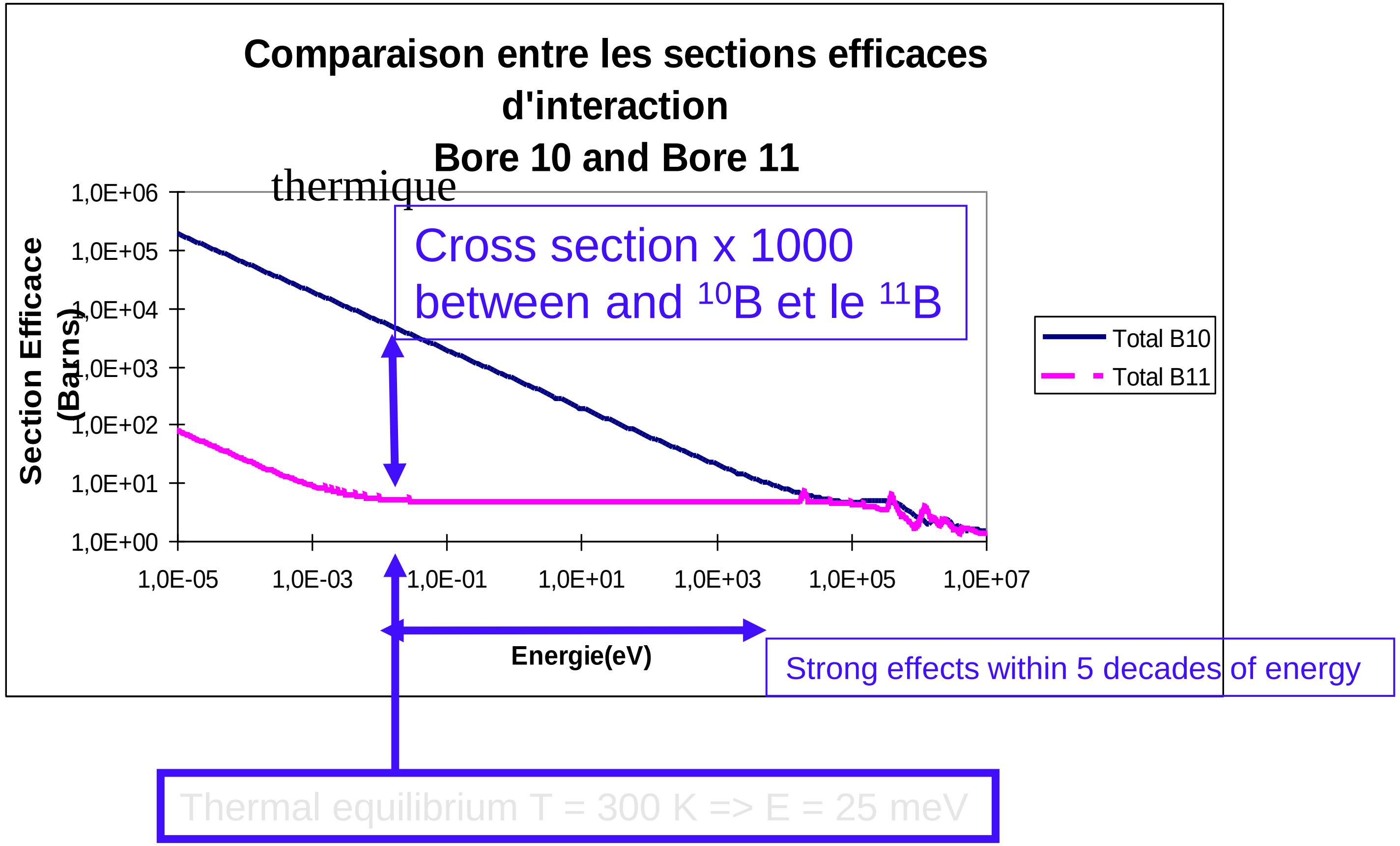
- **at airplane Altitude: 10 000 neutron/cm^2/hour**

  upper limit of one transient per 10 hours of flight per cm^2 of circuit

10B isotope in electronic devices

Boron is a commonly used as dopant or softener of glass oxide in silicon devices. Its content and repartition near sensitive volumes is generally unknown. It may be absent.

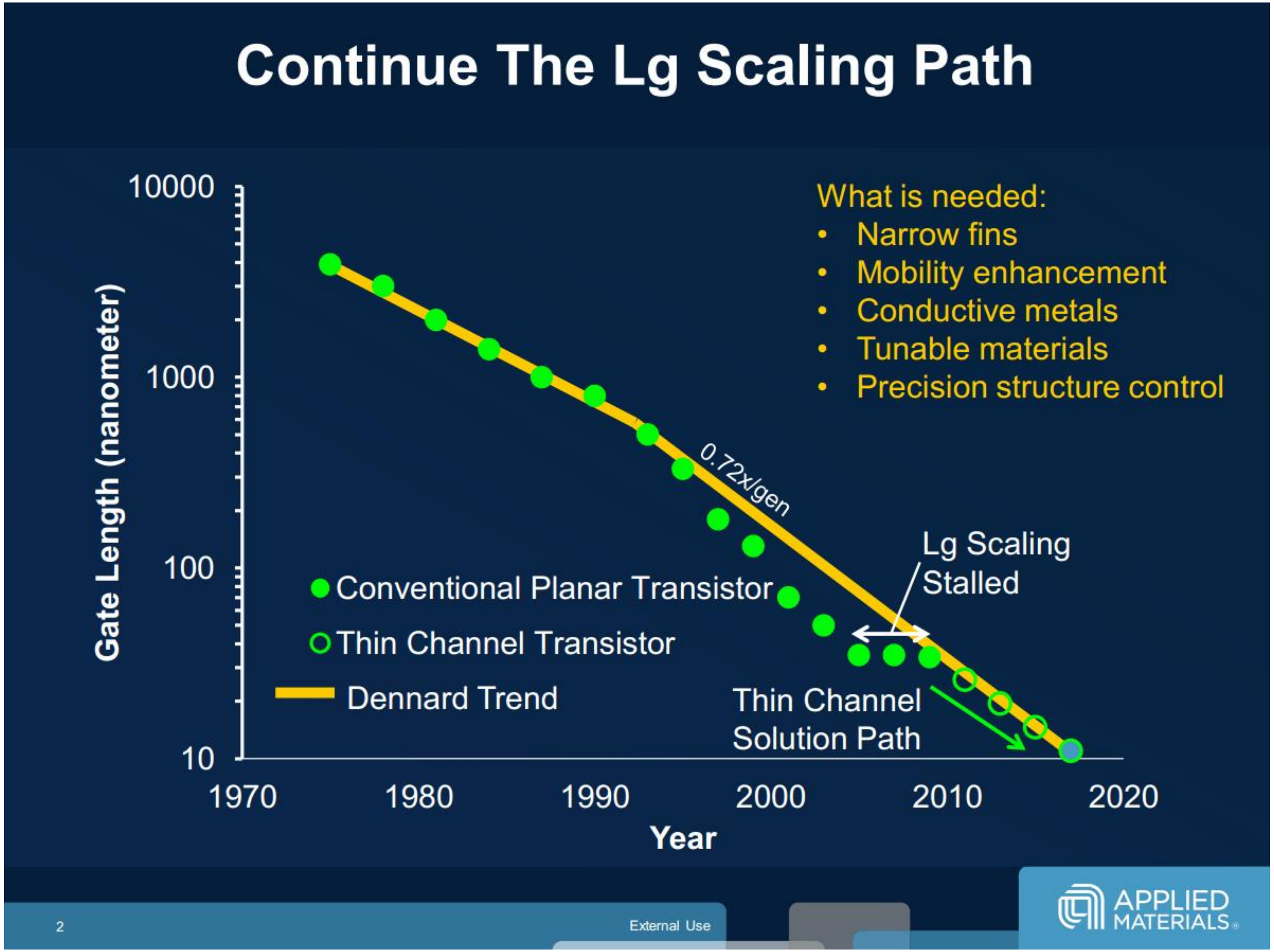
Nuclear capture breaks 10B and gives highly ionizing alpha particle recoils of single energy 1.5 MeV



Cross section x 1000 between and ^{10}B et le ^{11}B

Strong effects within 5 decades of energy

Thermal equilibrium T = 300 K => E = 25 meV



Continue The Lg Scaling Path

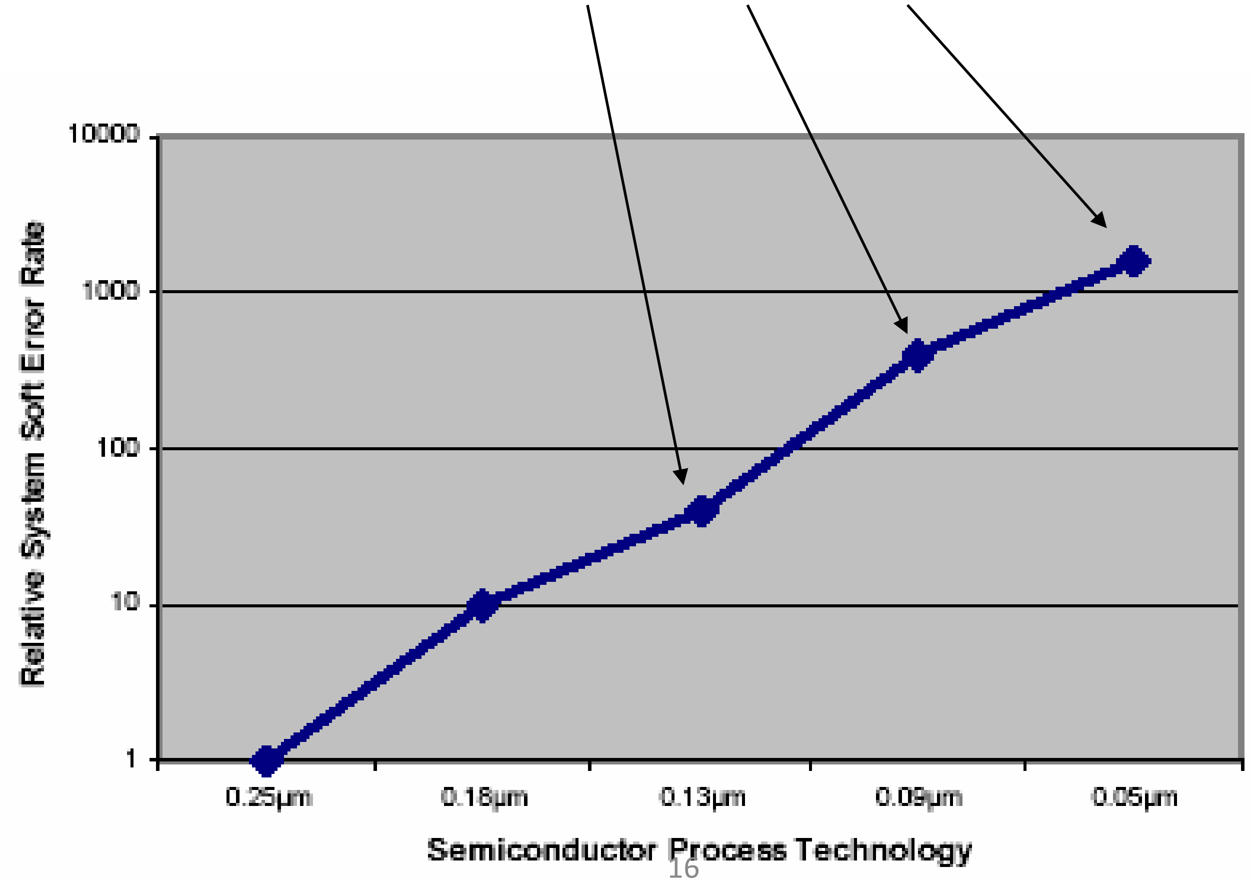
What is needed:
- Narrow fins
- Mobility enhancement
- Conductive metals
- Tunable materials
- Precision structure control

External Use

APPLIED MATERIALS

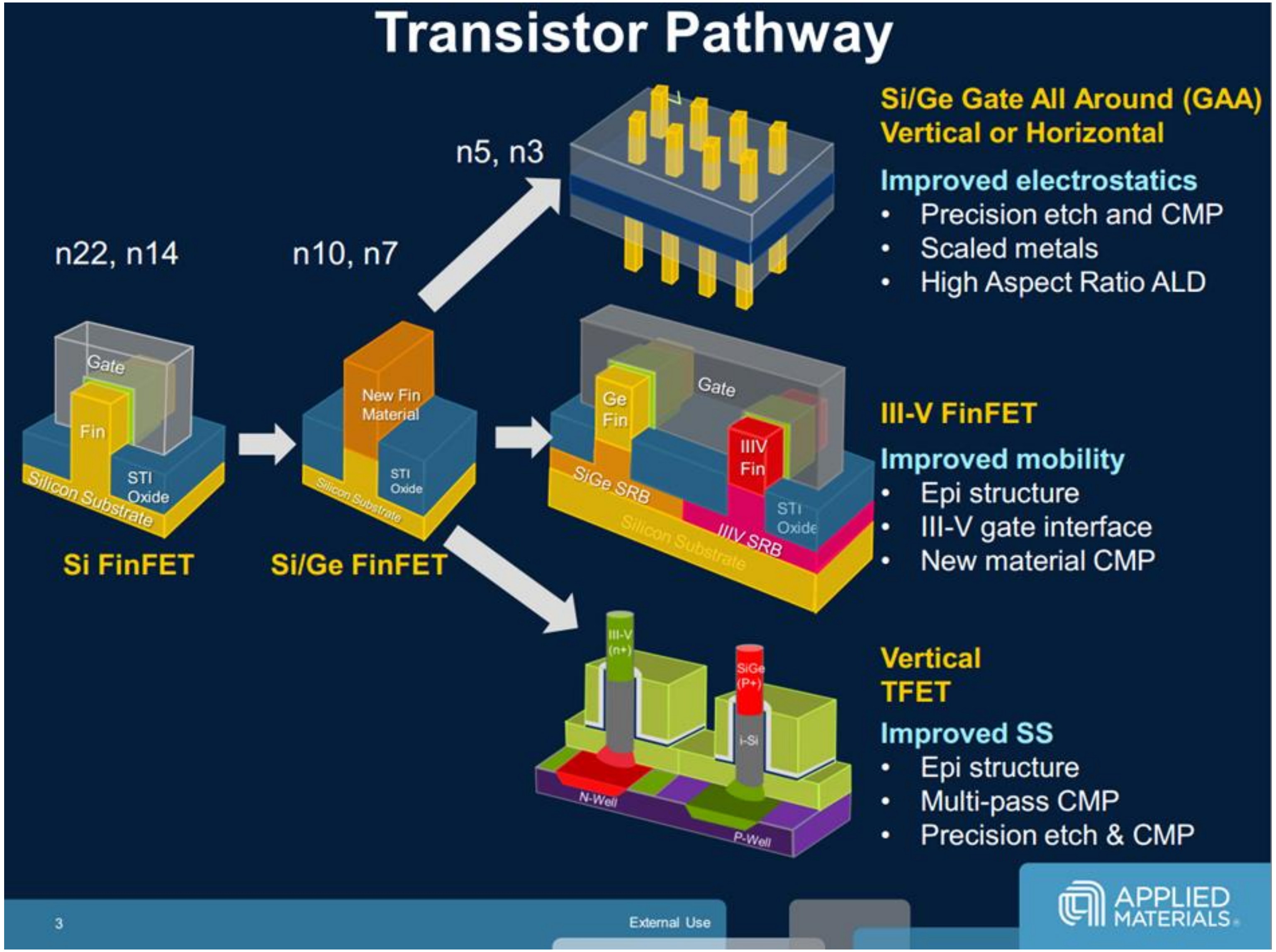
Soft Error Rate trends – Linked to the stored Charge in a bit Cell

Year	2001	2004	2007	2010	2013	2016
Litho CD (nm)	130	90	65	45	32	22
Supply Voltage (V)	1.3	1.0	0.7	0.6	0.5	0.4
Nodal Capacitance (fF)	2.00	*1.38*	*1.00*	*0.69*	*0.49*	*0.34*
Nodal Charge (fC)	*2.60*	*1.38*	*0.70*	*0.42*	*0.25*	*0.14*
Nodal Charge (electrons)	*16250*	*8654*	*4375*	*2596*	*1538*	*846*



Actel - Effects of Neutrons on Programmable Logic, IEEE Trans Nucl Sci, 12, 2003

Planar Electronics is becoming 3D with a stratospheric number of transistors on one cm2



Transistor Pathway

n22, n14

Si FinFET

n10, n7

Si/Ge FinFET

n5, n3

Si/Ge Gate All Around (GAA) Vertical or Horizontal

Improved electrostatics
- Precision etch and CMP
- Scaled metals
- High Aspect Ratio ALD

III-V FinFET

Improved mobility
- Epi structure
- III-V gate interface
- New material CMP

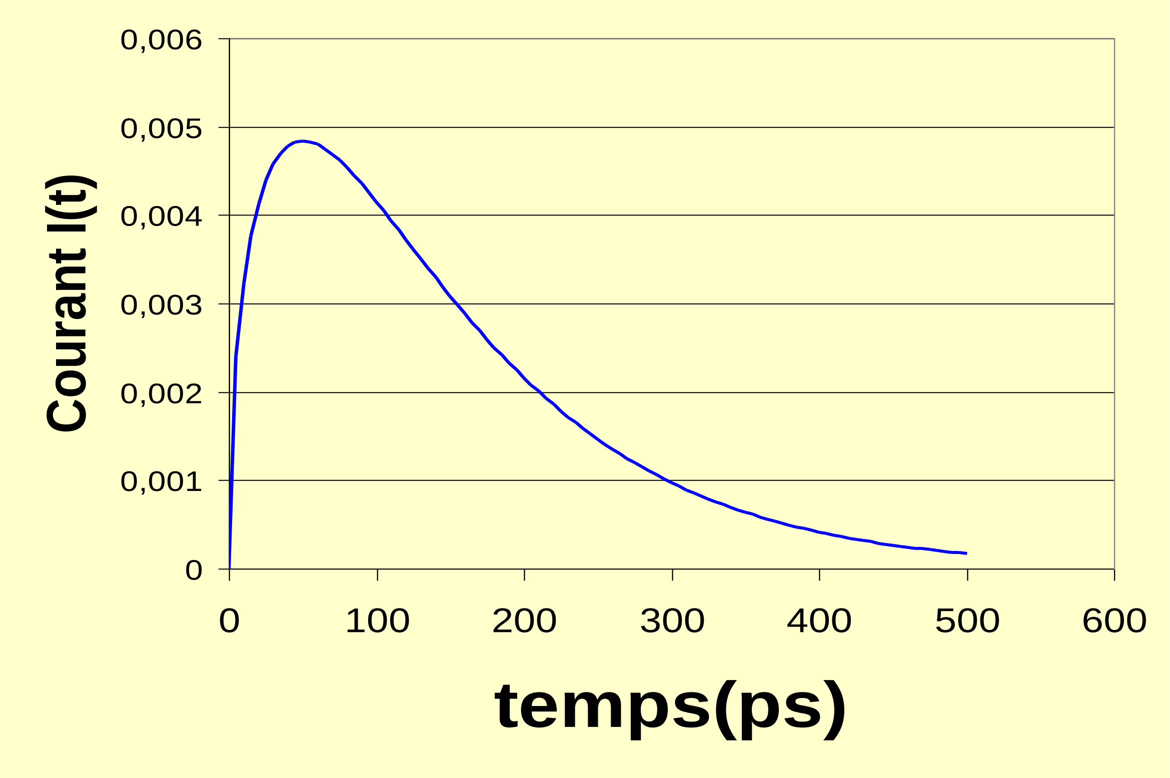
Vertical TFET

Improved SS
- Epi structure
- Multi-pass CMP
- Precision etch & CMP

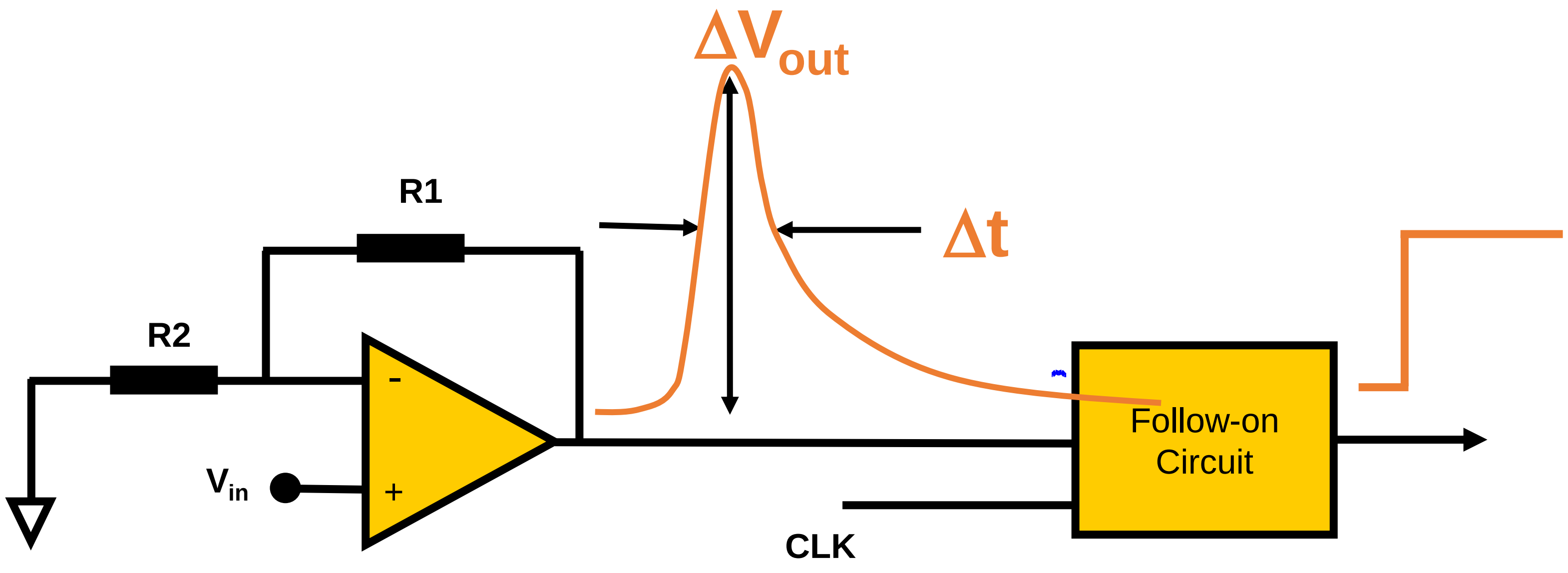
APPLIED MATERIALS

Current shape

$$I(t) = \frac{2}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp(-\frac{t}{T})$$

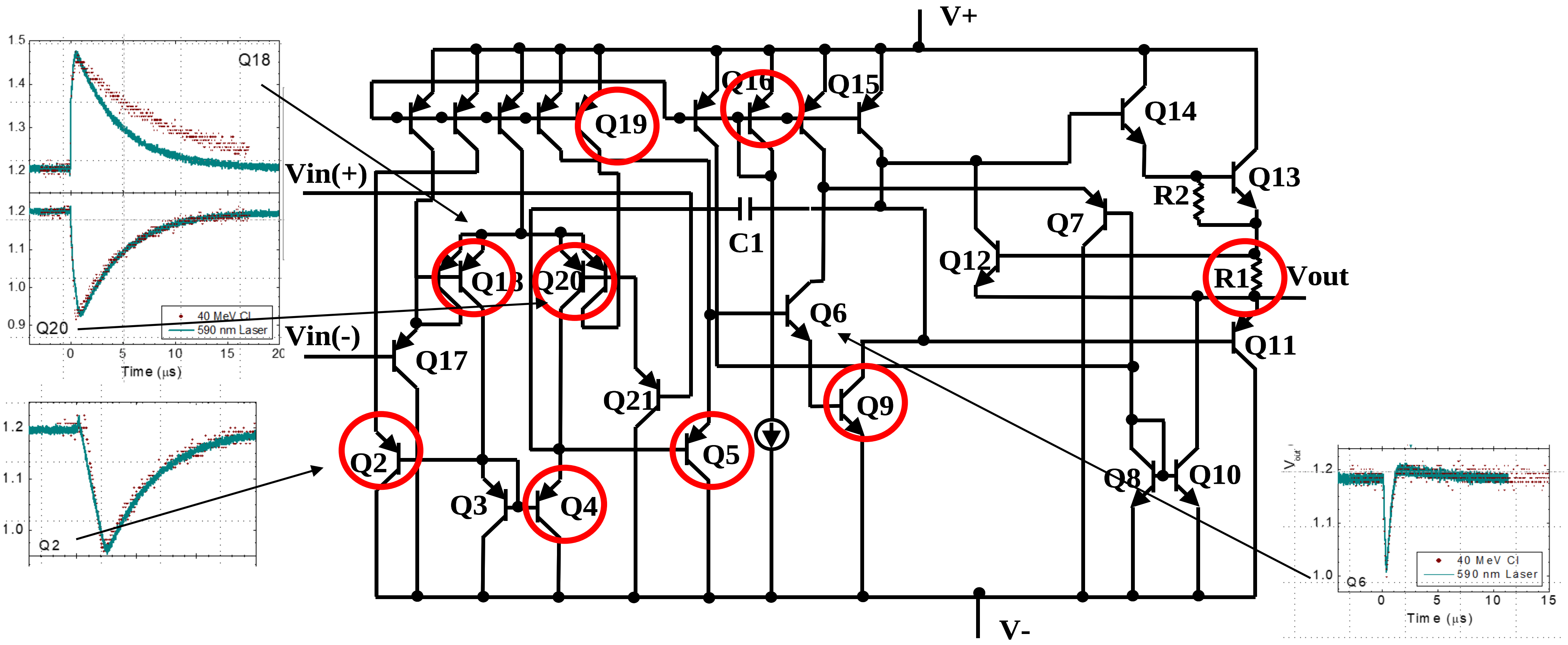


Single Event in an analog circuit



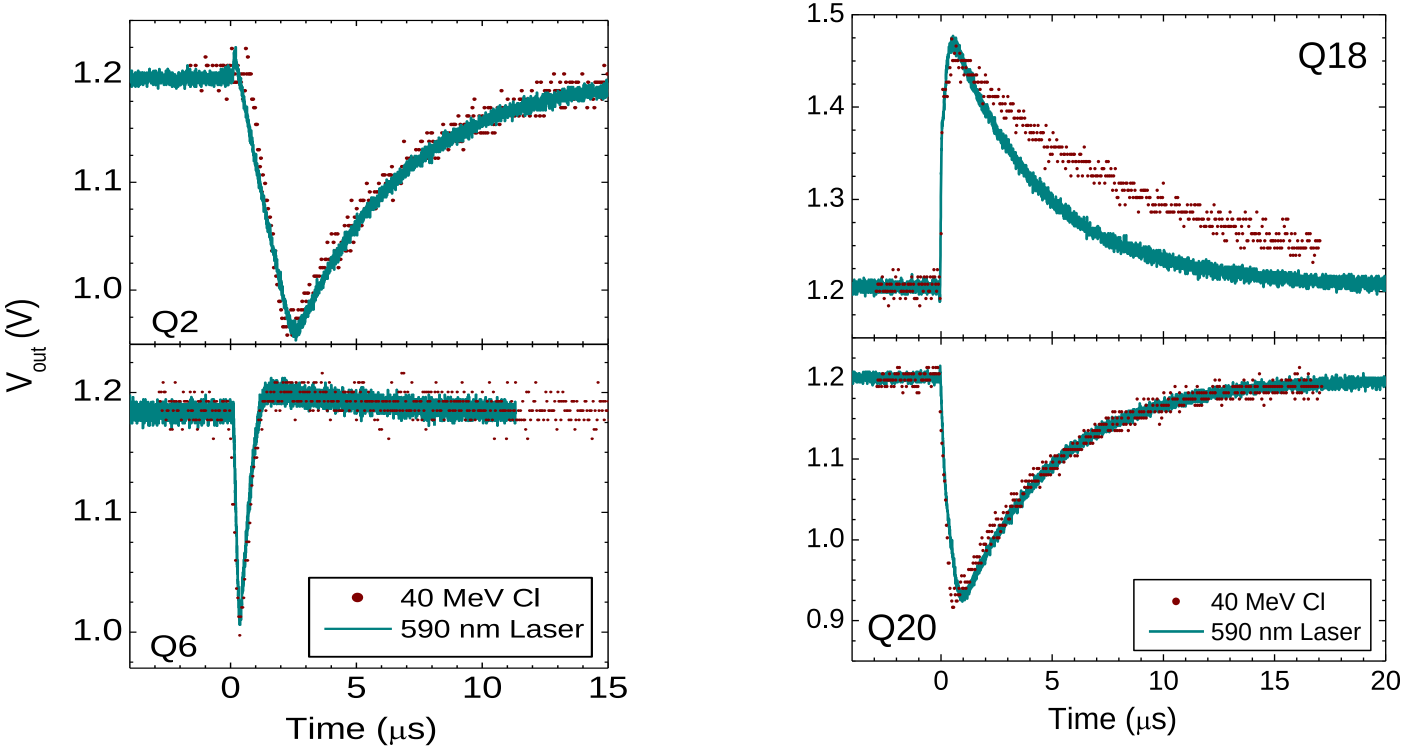
Example on an amplifier (LM124), various strike location

Bipolar transistors are particularly sensitive because of current gain In CMOS technology



Dale McMorrow, NRL, USA

Single Event Transients

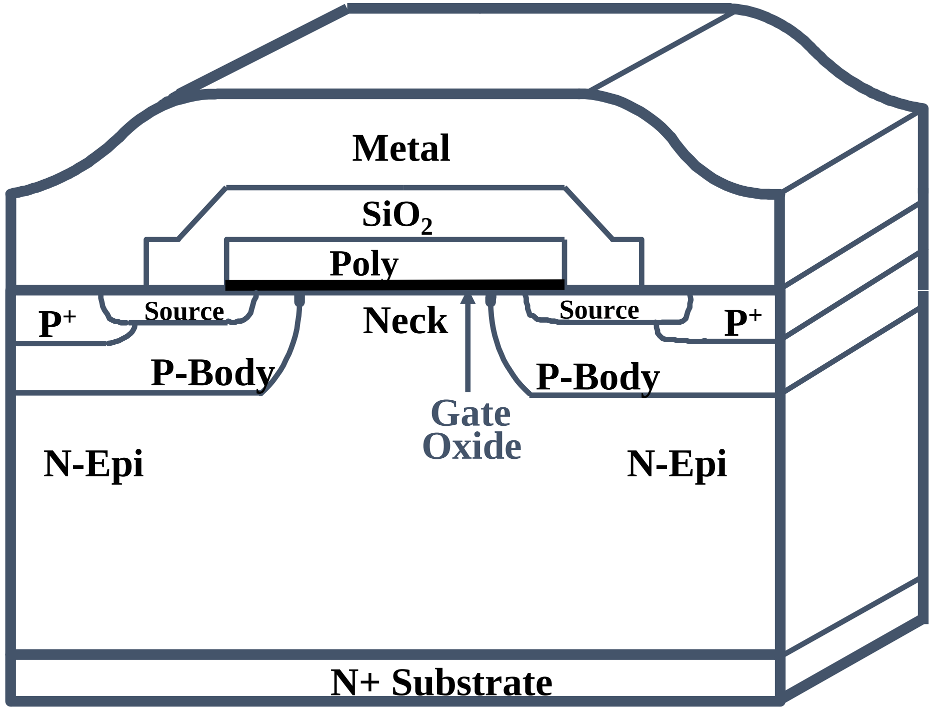


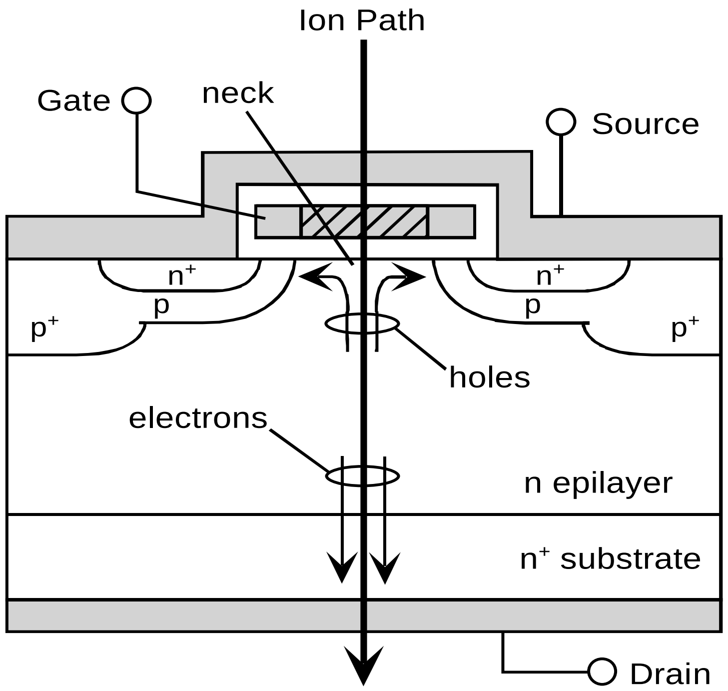
LM124
Inverting
Configuration:
V_{dd} = +/-6 V
V_{in} = 60 mV

MOREOVER, in a CMOS circuit, any NPN and PNP are hiden in the mesh of N and P doping. They are used in isolation and are supposed to be off, but they are not mute under radiation. They can lock (latch a CMOS device supposed without bipolar:

*Buchner, et al., **50**, IEEE Trans on Nucl. Science, Dec. 2003*

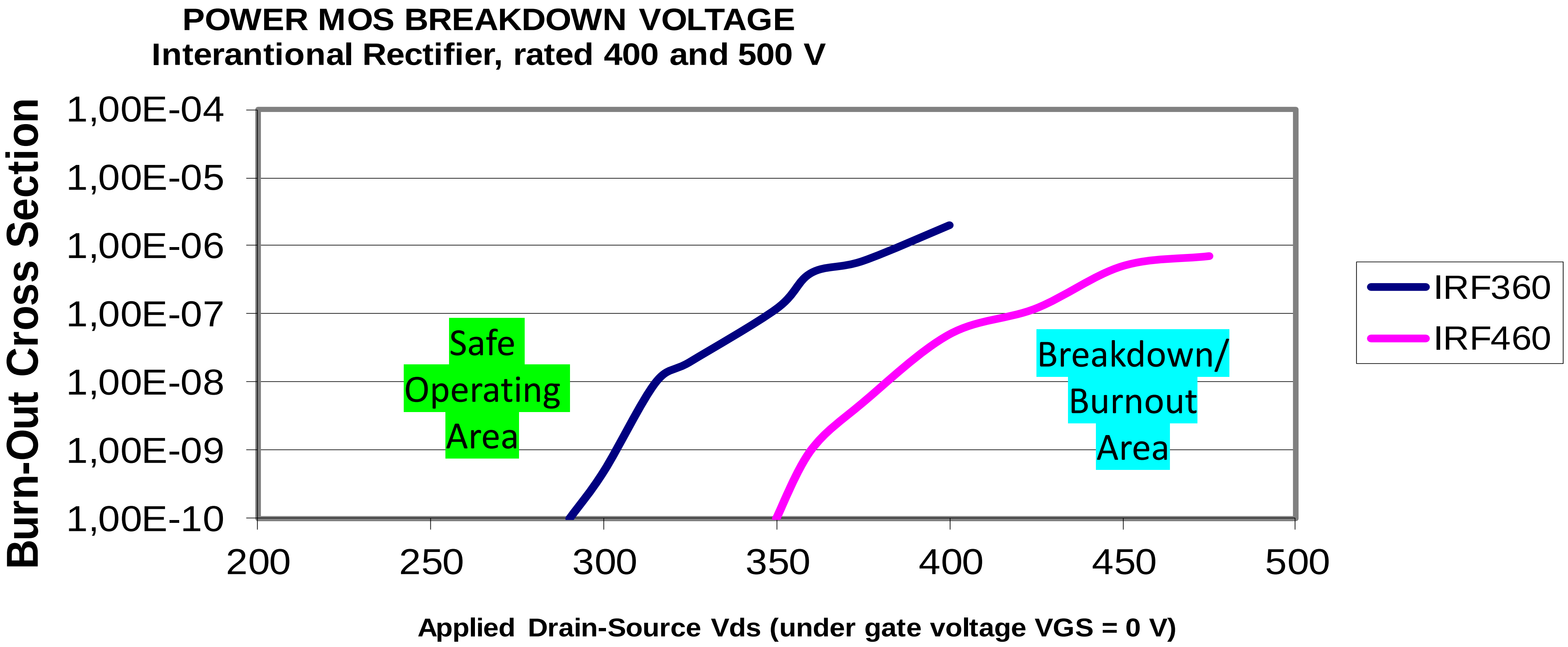
Power electronics (from 50V to 5kV in silicon)
Single Event Breakdown
depending on gate and drain to source voltages





Here displayed : typical of space applications,
dE/dx between 1 and 100 fC/µm)
~ 50.000 e-h pair per µm

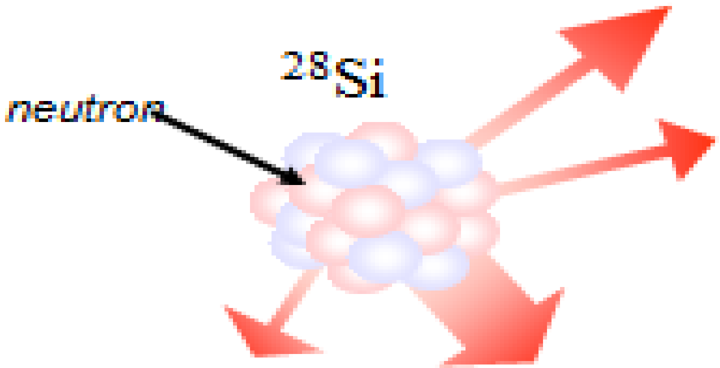
Safe Operation Area may need a derating of 50 to 70% of the max service drain voltage



TYPE	Breakdown voltage threshold
IRF360 (400V)	280V
IRF460 (500V)	330V

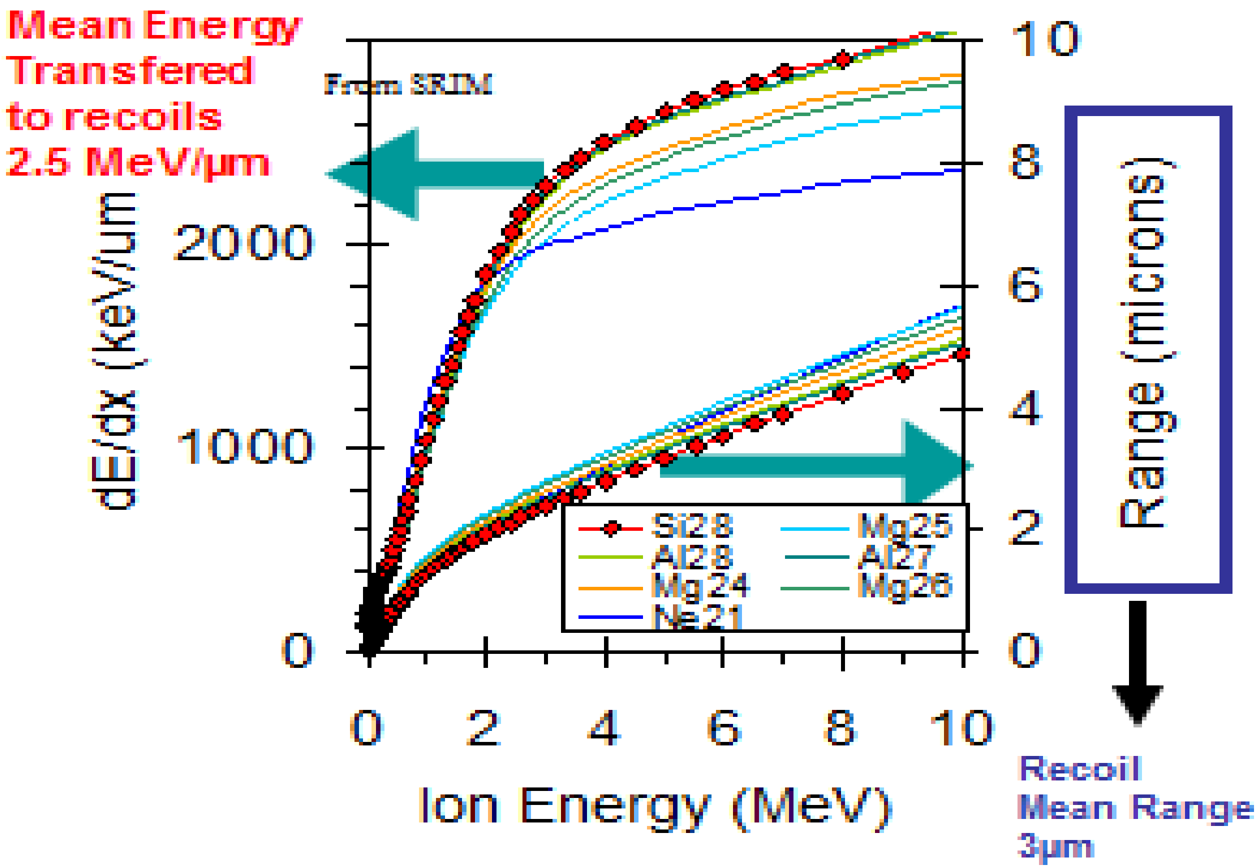
Back to the basic of Neutron => Silicon

Neutron => Silicon Recoil Range = 10µm



Products	Thresholds
^{25}Mg + α	2.75 MeV
^{28}Al + p	4.00 MeV
^{27}Al + d	9.70 MeV
^{24}Mg + n + α	10.34 MeV
^{27}Al + n + p	12.00 MeV
^{26}Mg + ^{3}He	12.58 MeV
^{21}Ne + 2α	12.99 MeV

Reaction table from F. Wrobel et al., IEEE Trans. Nucl. Phys., Vol. 47, No. 6, Dec. 2000



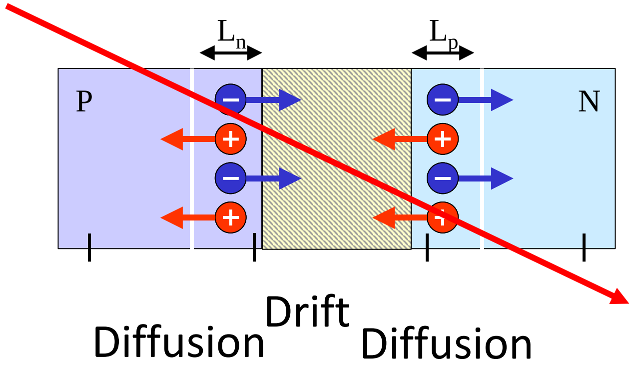
Mean Energy Transfered to recoils 2.5 MeV/µm

Recoil Mean Range 3µm

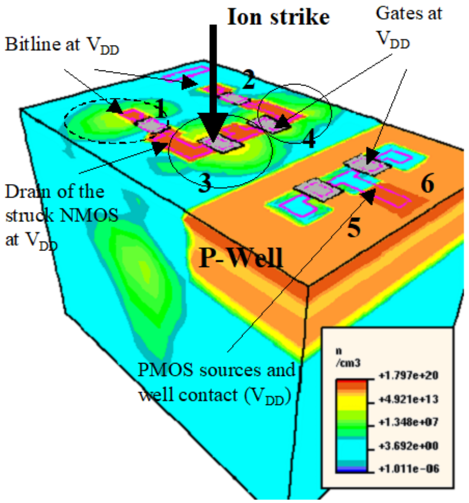
After Bauman, RADECS Short Course 2001

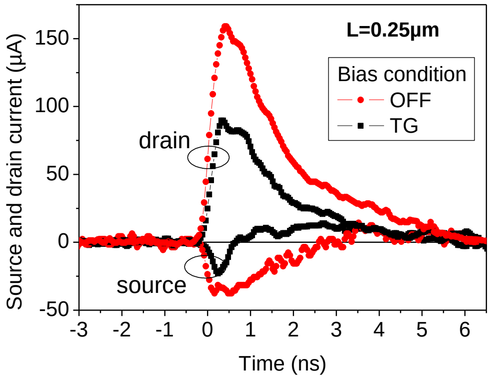
COMPLEX CMOS CIRCUITS

1. Diode, ion path across a single junction



2. MOS Transistors, 2 or more junctions

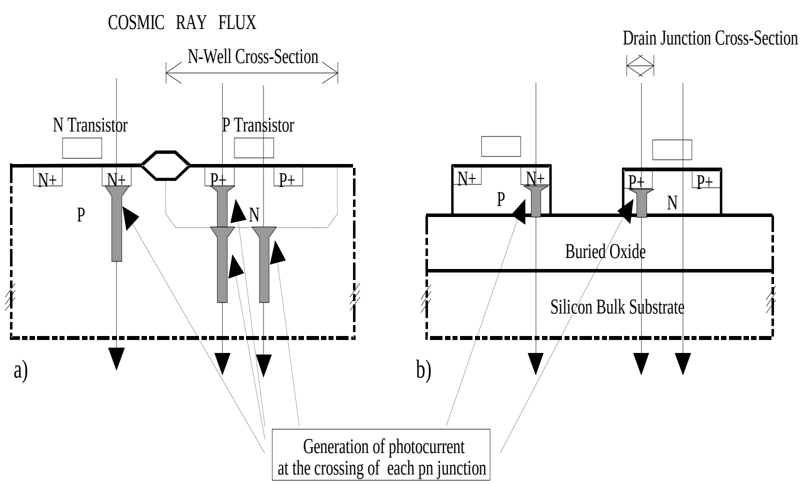


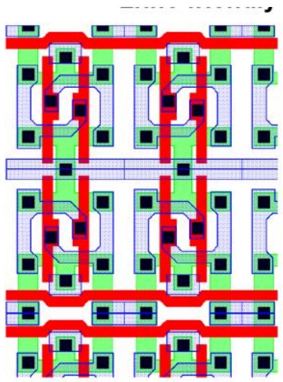


Short transient currents measured at the source and drain electrodes of a 0.25 µm NMOS transistor

35 MeV chlorine ion => Collected Charge 1 to 100 femtoCoulombs
=> 0,1 to 10 V in 10 femtofarads

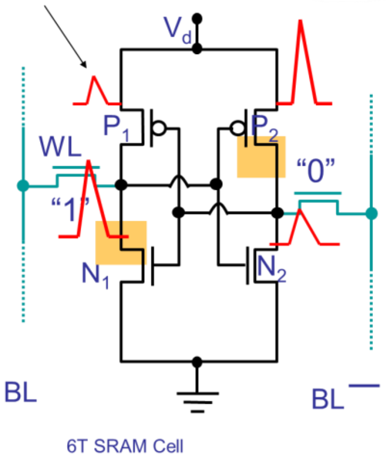
3. Many Transistor in a circuit
‘pixelization’ increases complexity
Response on vertical and surface layout



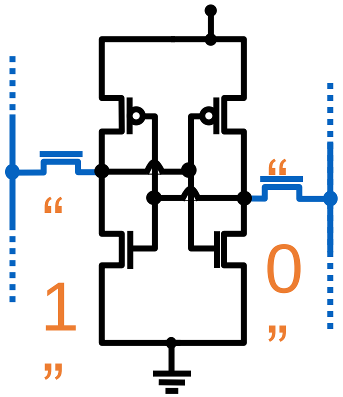


4. Circuit response (SRAM 6-T cell)

Amplitude according to the location of the ion strike



Circuit impulse rtesponse: willi flip? Will it remain stable?
Single Event Upset
Single Event rate



Metric is generally related to the beam flux and ionizing particle dE/dx (LET Linear Energy Threshold)

Graph is build up with a succession

of experiments or simulations

(single isotope beamand monoenergetic Energy)

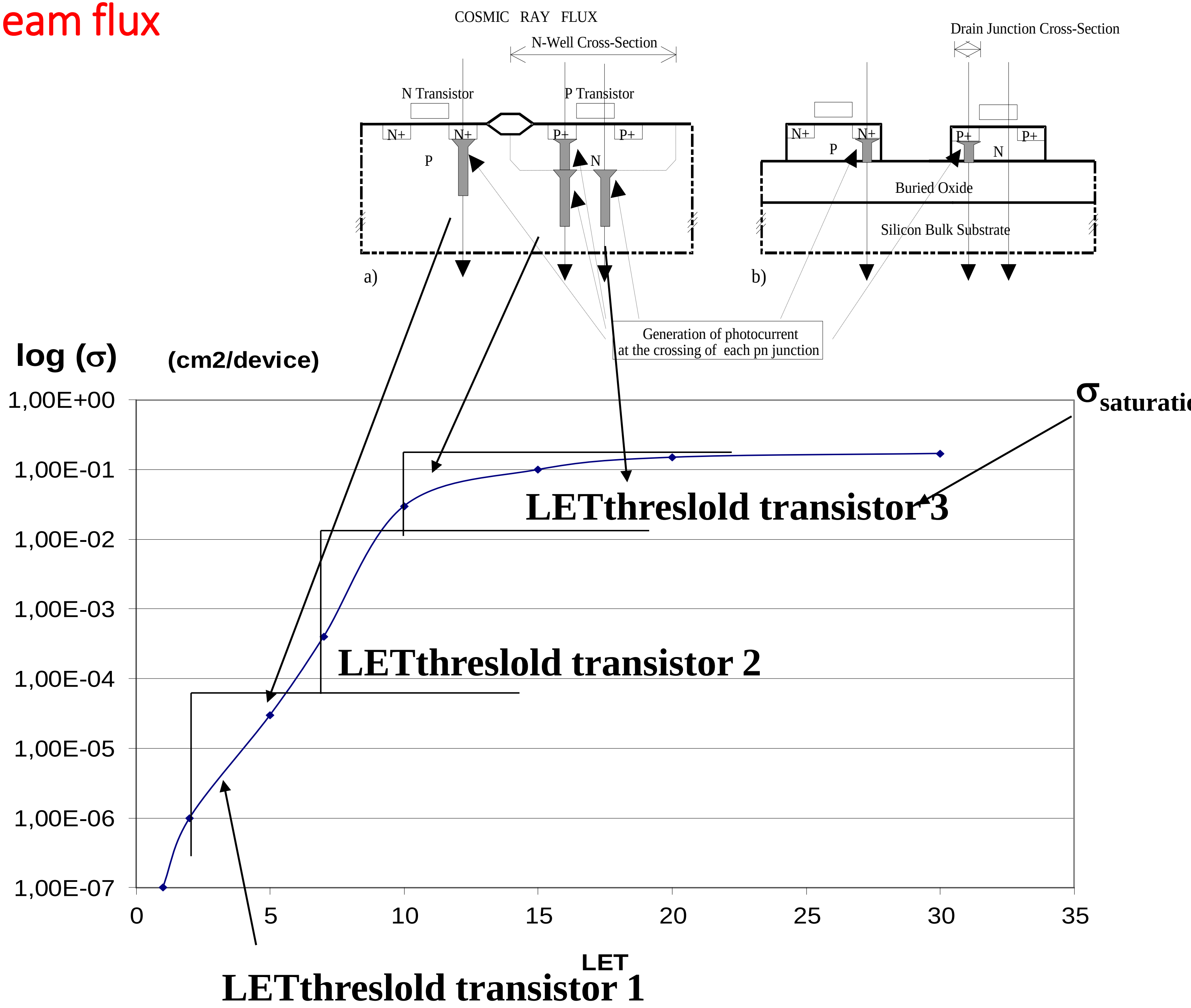
At each step

$$\sigma_{SEE}\ (LET) = N_{event} / \phi_{flux\ (energy\ E)}$$

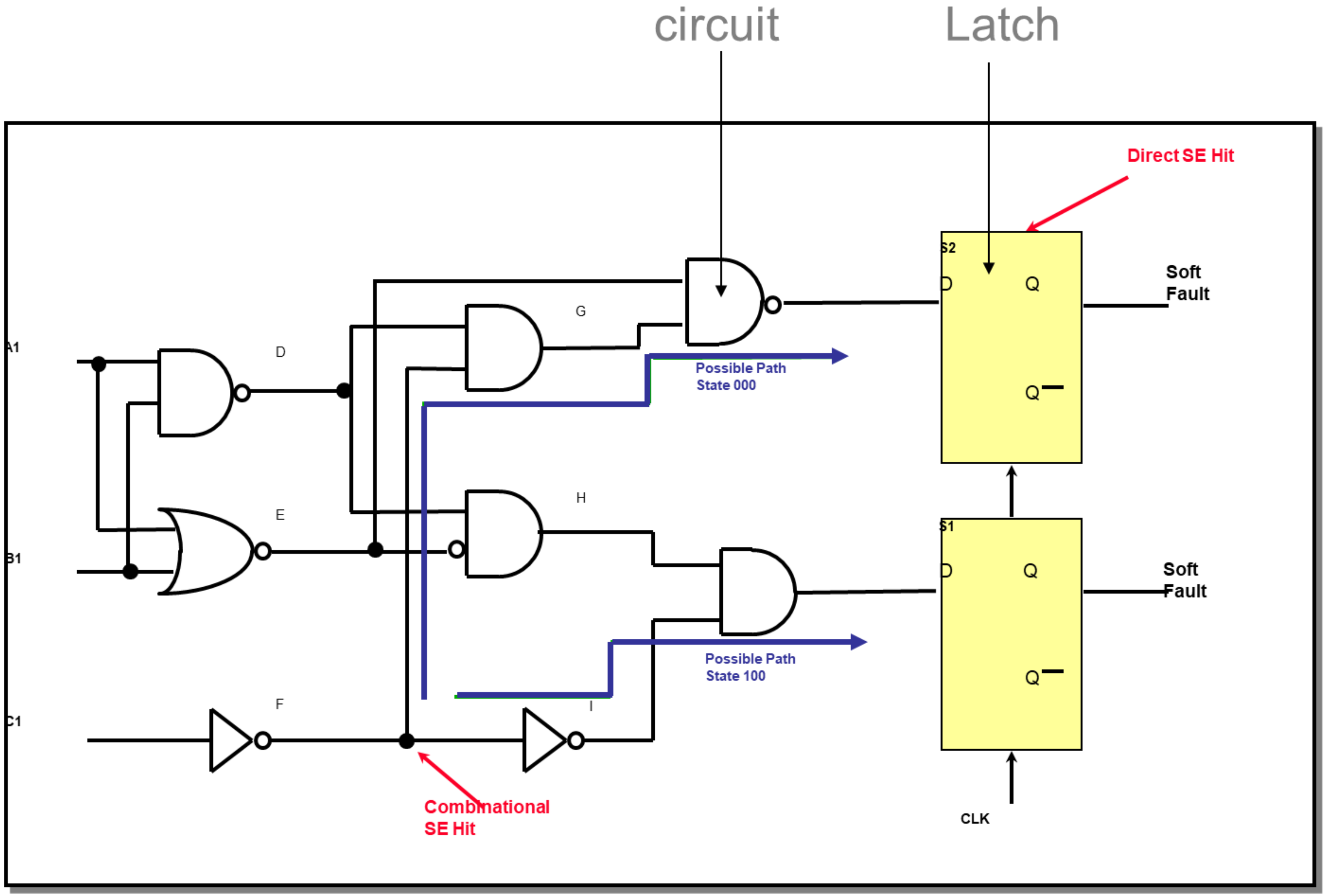
In case of a spectrum one expects

$$N_{event} = \int \sigma_{SEE}\ (LET)\ \phi_{differential\ flux}\ dLET$$

NOTE that σ_{SEE} is a complex mix of nuclear cross section σ_{nuc} and of circuit response with a threshold on the delivered ionization



Single Event Transient Propagation vs Masking

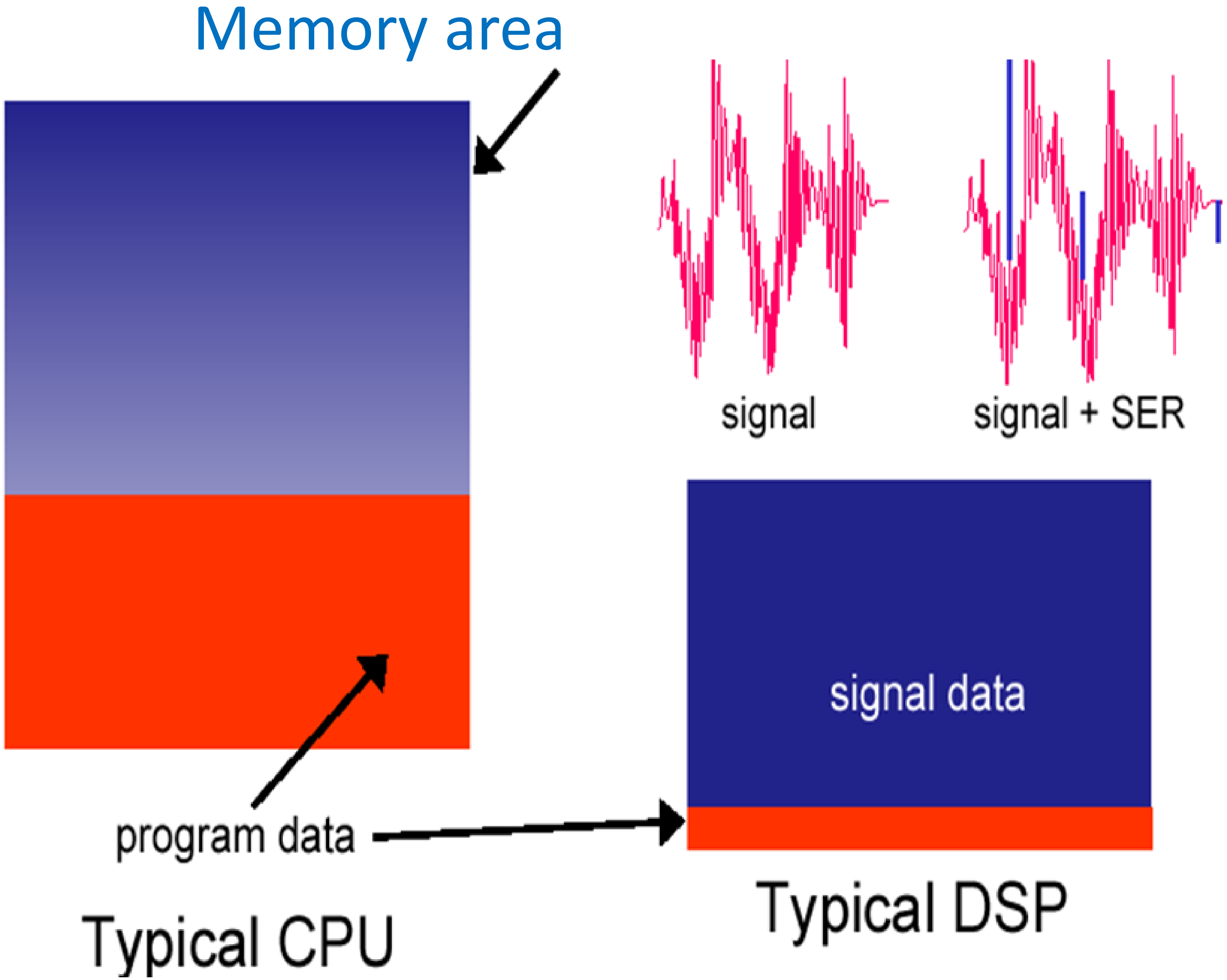


Single Event Rate.

CPU, DSP, ADC, etc… differ
An issue for radiation testing standardization.
A matter of reserch papers.

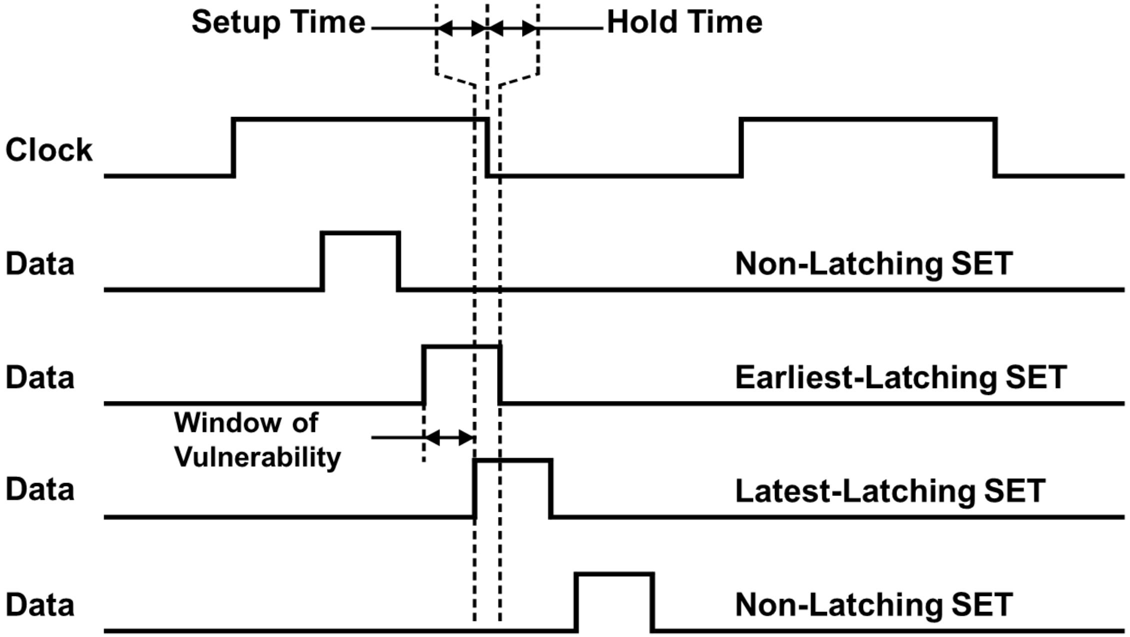
« test as you run it » ?

Test standards references
at the end of the talk



Window of vulnerability

a linear dependence is observed of the Single Event Rate with the clock frequency

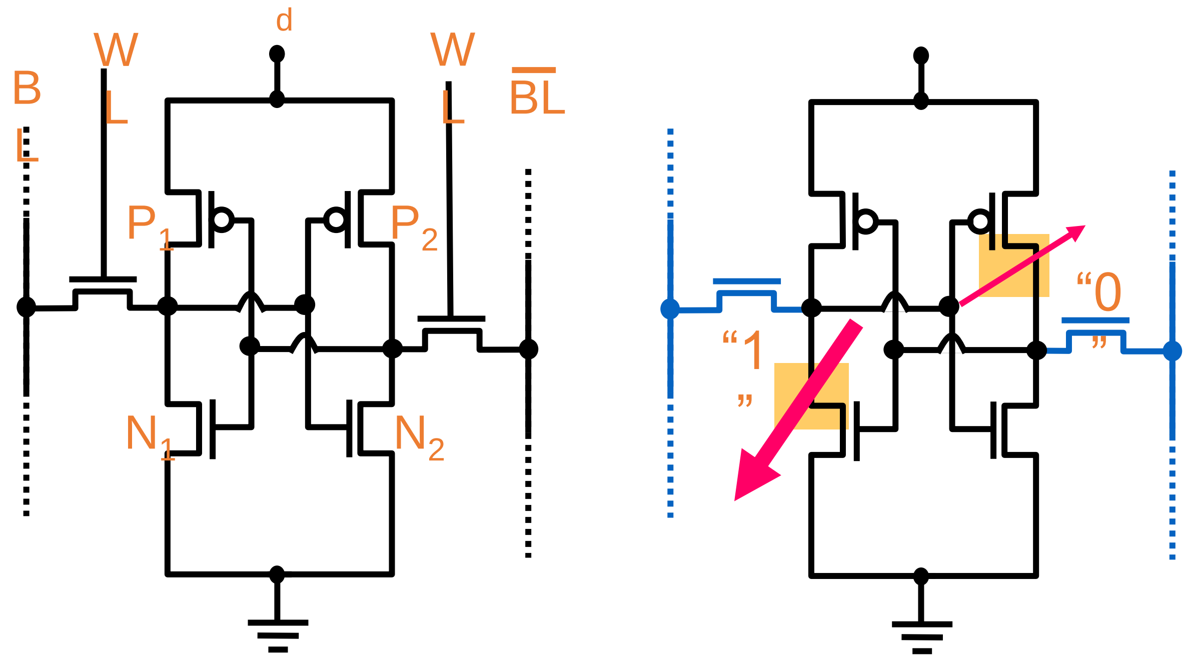


Clock rate increase makes the transient capture more probable during the setup and hold time

Lets go back to Electronics scaling in DIGITAL CIRCUITS

LET’s have a look at SRAMS, used in Cache and some FPGA, etc…

- In SRAM, bit-flip can occur if the transient meets the feed back condition.

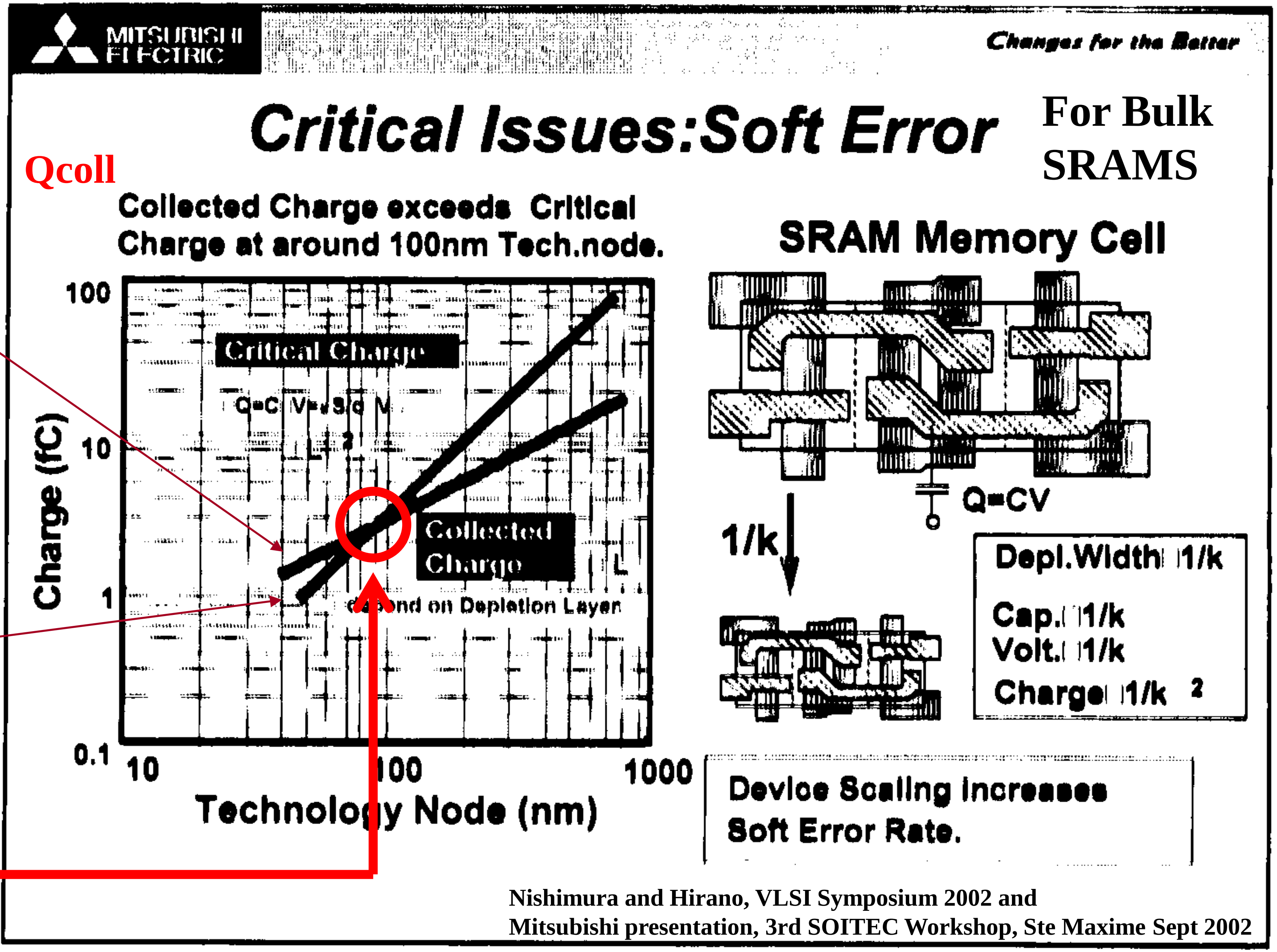


6T SRAM Cell

- Data is corrupted if Qinjected > Qstored

A clever remark (2002): A transition between 0.25µm and 0.1µm technology Nodes

Qcoll~L



Critical Issues:Soft Error

For Bulk SRAMS

Qcoll

Collected Charge exceeds Critical Charge at around 100nm Tech.node.

Technology Node (nm)

Device Scaling Increases Soft Error Rate.

Nishimura and Hirano, VLSI Symposium 2002 and
Mitsubishi presentation, 3rd SOITEC Workshop, Ste Maxime Sept 2002

Qcrit~L^2

Qcoll>Qcrit
below 0.1µm
(circa 2000)

We shall illustrate this using a simple “STATIC” model

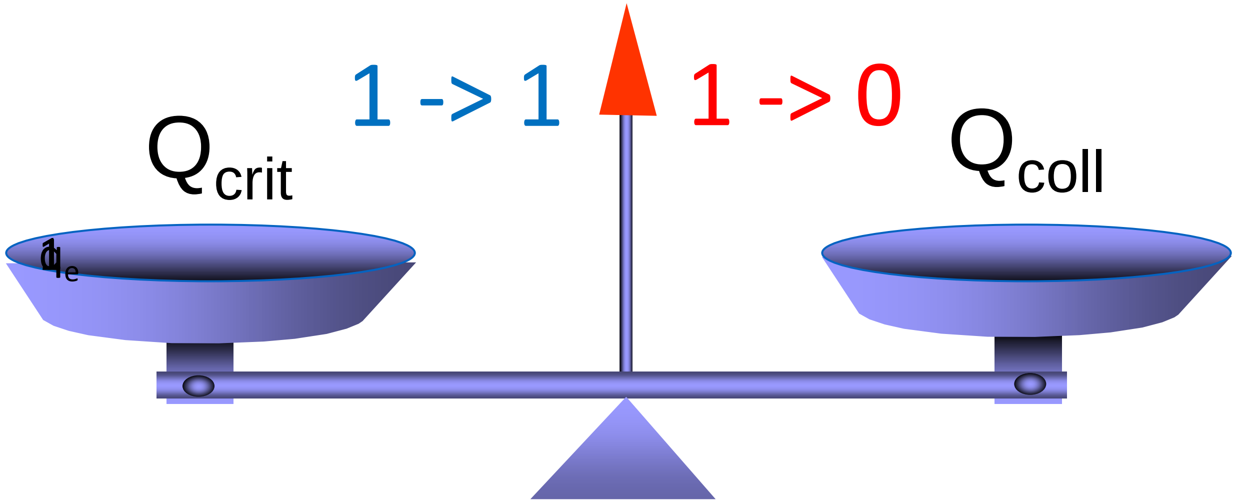
Single Event Upset at an electrical node in a SRAM or a DRAM

Qcrit = Stored Charge define the bit “1”

Qcrit>Qcoll => stable => no error

Qcoll = variable Collected Charge, particle dependant

Qcoll > Qcrit => Flip => Error



Drawing after Robert Baumann, RADECS 2001 Short Course and IRPS02

$Q_{crit} \sim C\,V \sim (\varepsilon)\,(W.L) / t \sim (\varepsilon)\,(L^2) / t$

= Stored charge on all the capacitances (

$Q_{coll} \sim (q_e / w)\,(dE/dx)\,(L^1)$

L = Collection Length by drift and diffusion

V = Supply voltage of the cell

t, equivalent thickness of materials

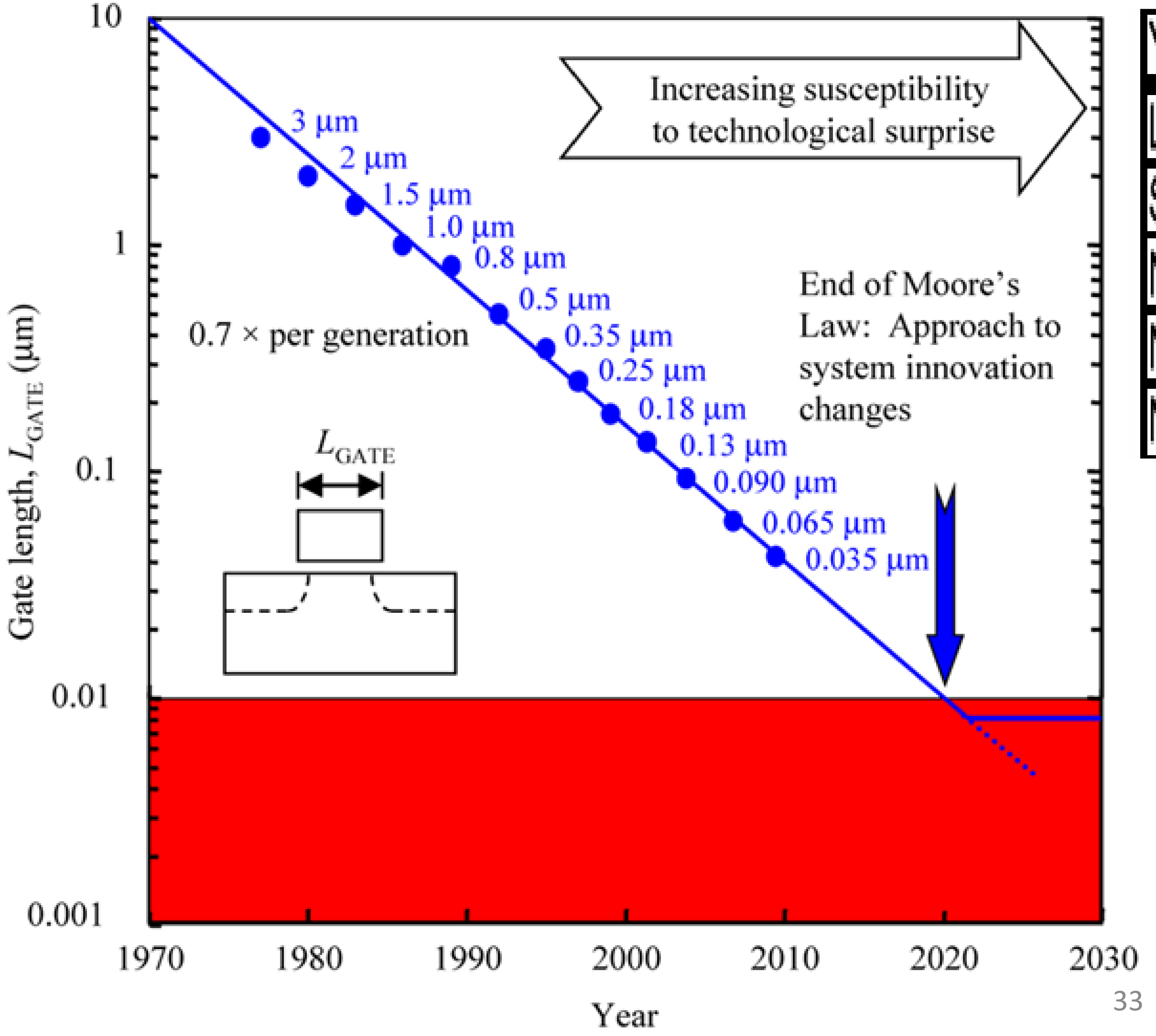
ε, weighted dielectric constant (Si, SiO2) in the cell

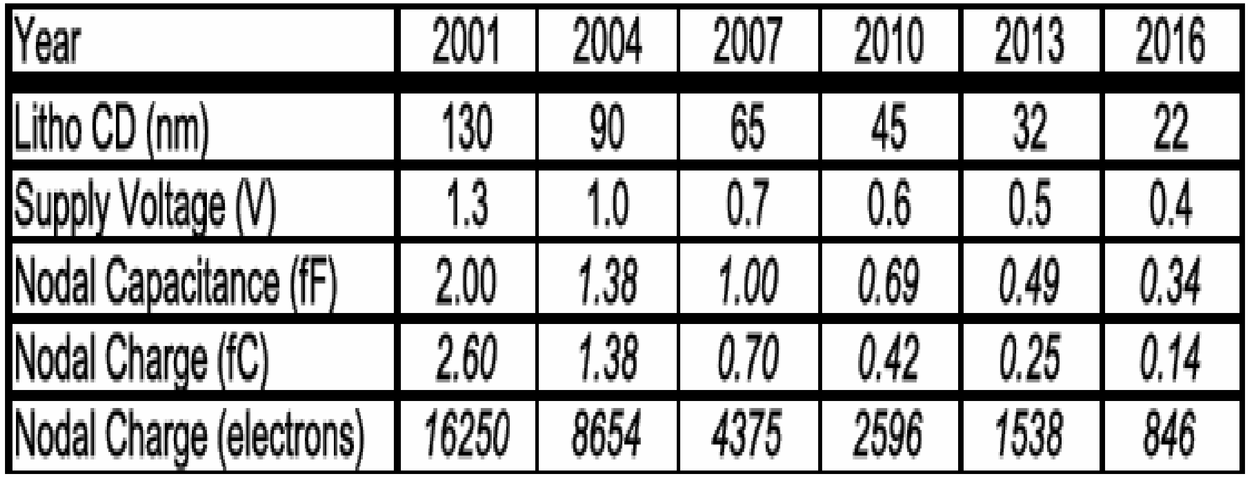
q_e = electron charge

w = ionization yield of the cell as a radiation detector

(PN junctions and transistors=

Consequence of scaling



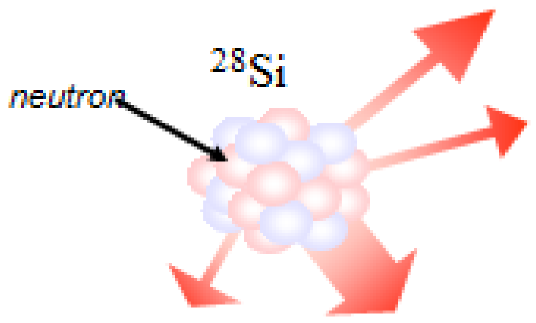


Year	2001	2004	2007	2010	2013	2016
Litho CD (nm)	130	90	65	45	32	22
Supply Voltage (V)	1.3	1.0	0.7	0.6	0.5	0.4
Nodal Capacitance (fF)	2.00	1.38	1.00	0.69	0.49	0.34
Nodal Charge (fC)	2.60	1.38	0.70	0.42	0.25	0.14
Nodal Charge (electrons)	16250	8654	4375	2596	1538	846

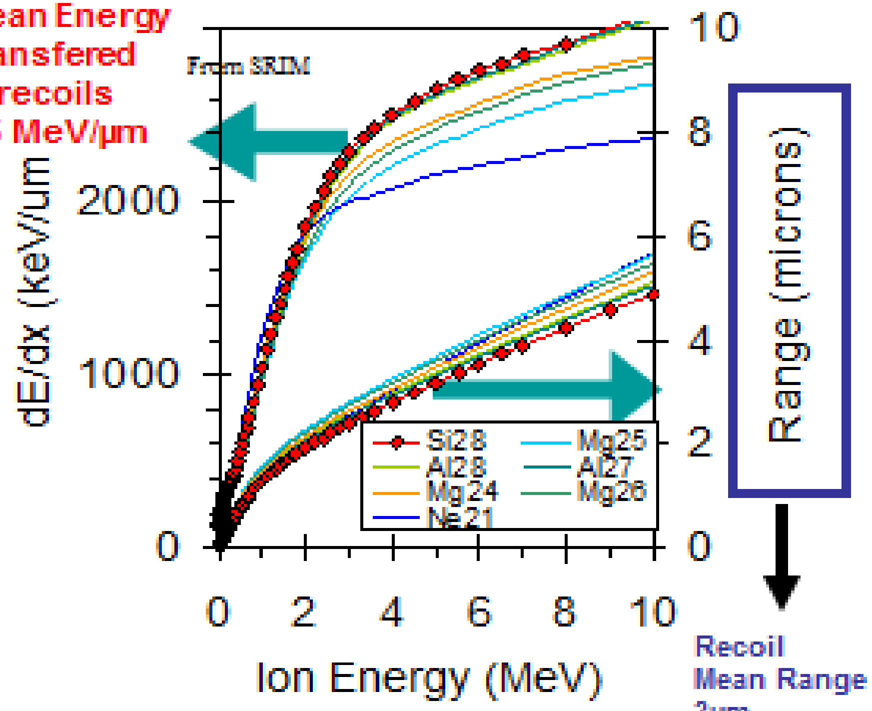
Any SRAM (cache), Registers sensitivity, DRAM (main memory, dramatically evoved with characteristic length of CMOS (Lgate, e.g.)

Basic of Neutron Effect => REMAIN THE SAME on Silicon for a neutron, dE/dx remains the same! REGARDLESS OF THE TECHNOLOGY NODE

Neutron => Silicon Recoil Range = 10µm



Mean Energy Transfered to recoils 2.5 MeV/µm



Recoil Mean Range 3µm

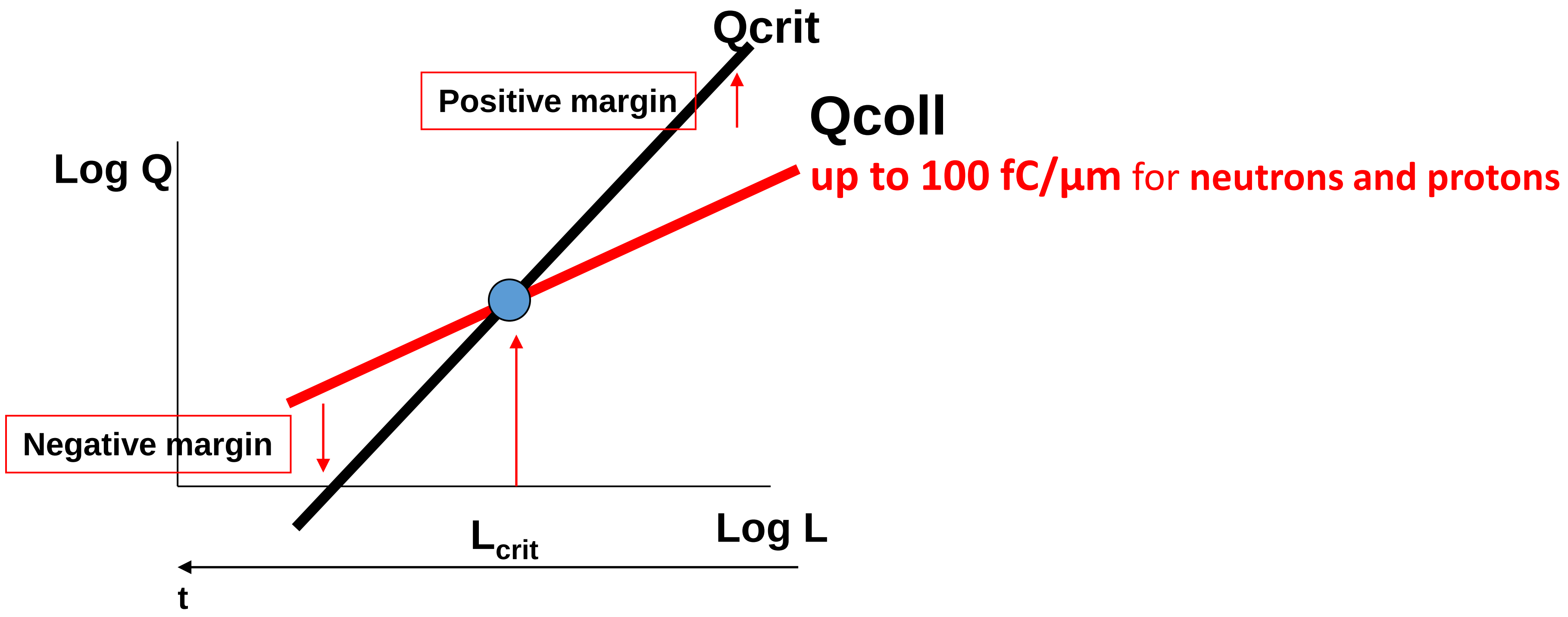
Products	Thresholds
^{25}Mg + α	2.75 MeV
^{28}Al + p	4.00 MeV
^{27}Al + d	9.70 MeV
^{24}Mg + n + α	10.34 MeV
^{27}Al + n + p	12.00 MeV
^{26}Mg + ^{3}He	12.58 MeV
^{21}Ne + 2α	12.99 MeV

Reaction table from F. Wrobel et al., IEEE Trans. Nucl. Phys., Vol. 47, No. 6, Dec. 2000

After Baumann, RADECS Short Course 2001

Application

- Qcrit~ CV ~ $\varepsilon_{ox} S/t_{ox}$ V ~ L^2
- Qcoll~ Diffusion length (or chord length) ~ L



True for a given type of technology (SOI, doping…) **and design** (transistor and circuitry surfaces)

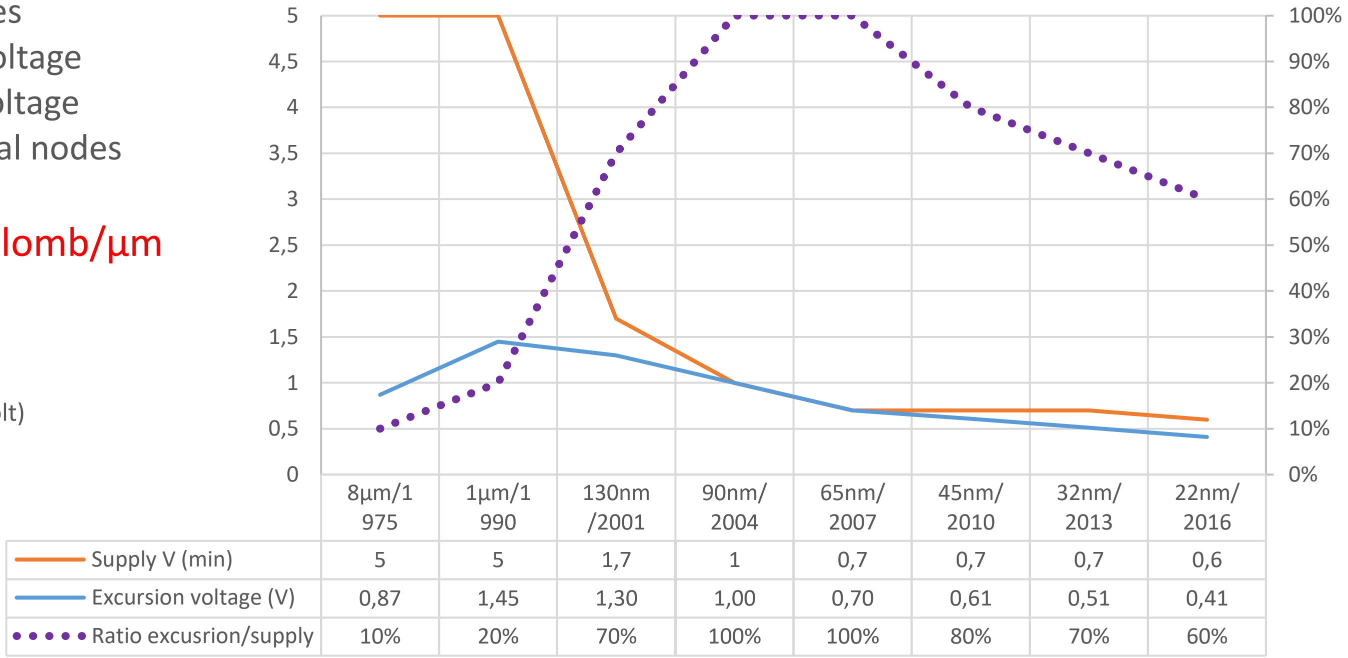
- => Differs from manufacturer to another

Since digital node ~1 micron and below (~1990)
All digital curcuits became prone to upset

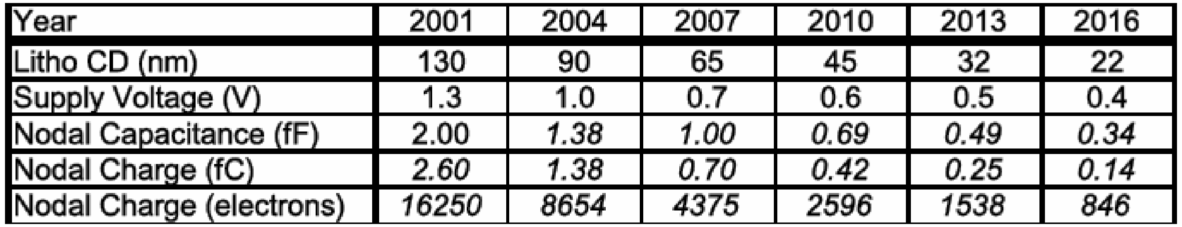
Examples
Excursion voltage
vs supply voltage
on CMOS digital nodes

at 10 femtocoulomb/µm

absolute values (volt)
and % (left axis)



	8µm/1975	1µm/1990	130nm/2001	90nm/2004	65nm/2007	45nm/2010	32nm/2013	22nm/2016
Supply V (min)	5	5	1,7	1	0,7	0,7	0,7	0,6
Excursion voltage (V)	0,87	1,45	1,30	1,00	0,70	0,61	0,51	0,41
Ratio excusrion/supply	10%	20%	70%	100%	100%	80%	70%	60%



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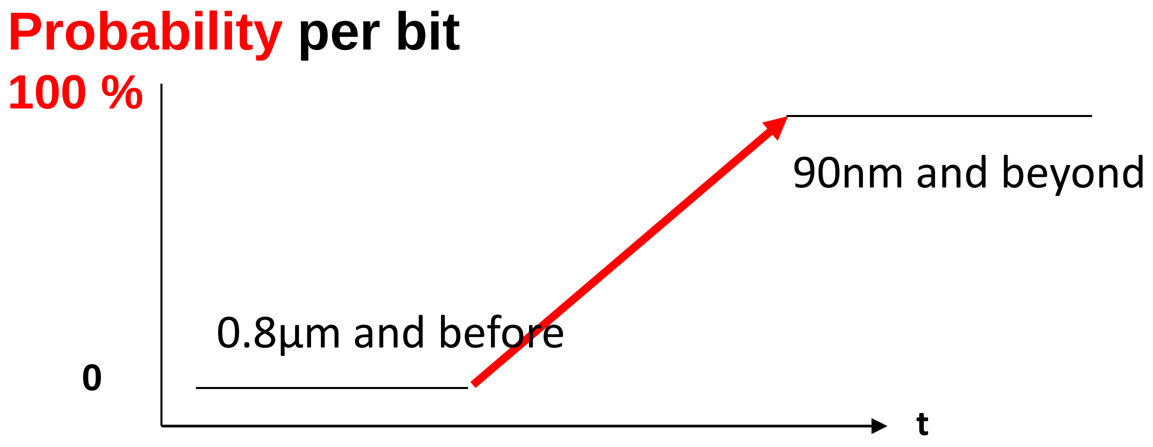
Nodal Charge (electrons)	*16250*	*8654*	*4375*	*2596*	*1538*	*846*

Conclusion 1
After 0.5µm and downward
any technology became vulnerable



As remarked by many workers, SRAM Sensitivity per bit stabilizes

But Megabit, Giga, Terabit size increases

Mitigations Issues and methods

NUCLEAR PHYSICS
Probability of a nuclear reaction in the vicinity of a transistor

→

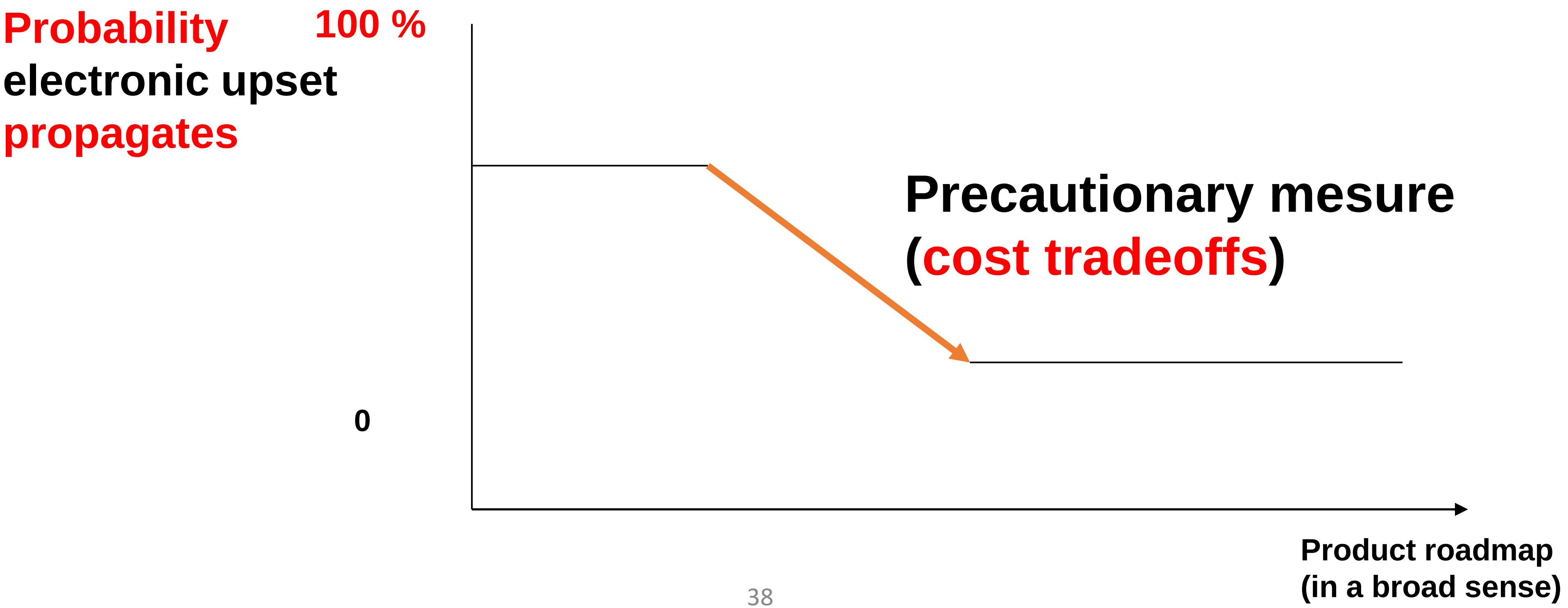
TECHNOLOGY
Probability that recoils cause a given electric pulse in a transistor

SOI
Triple Well

→

DESIGN
Probability that the perturbation propagates and cause failure

EDAC
Error Detection and Correction



Conclusion 2. Mitigation Chain: A Multi-Scale Effort

NUCLEAR PHYSICS
Nuclear reaction
in the vicinity of a transistor

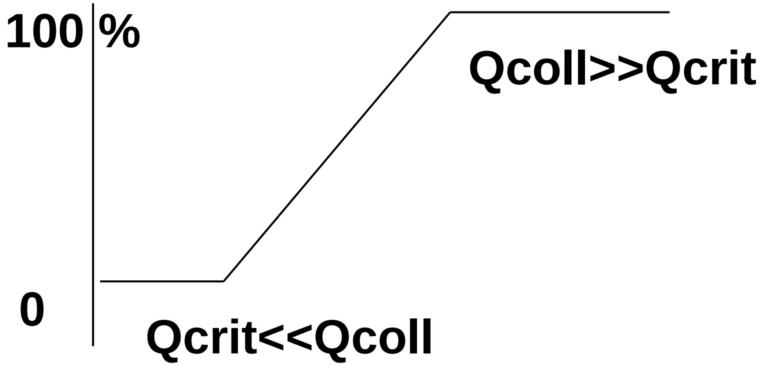
→

ELECTRONIC TECHNOLOGY
Recoils cause
a given electric pulse in a transistor

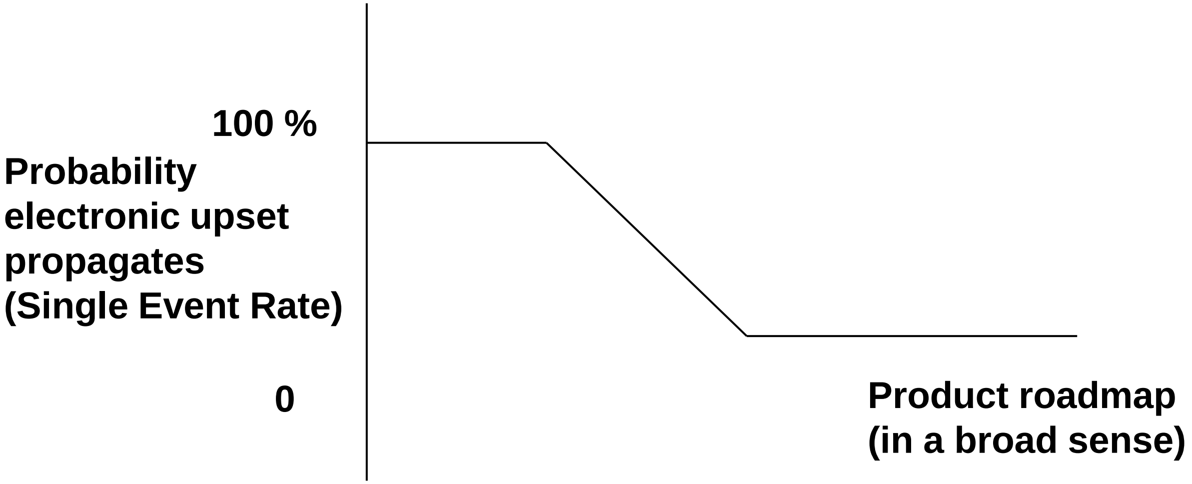
→

DESIGN AND CLOCK RATE
Perturbation
propagates and cause failure

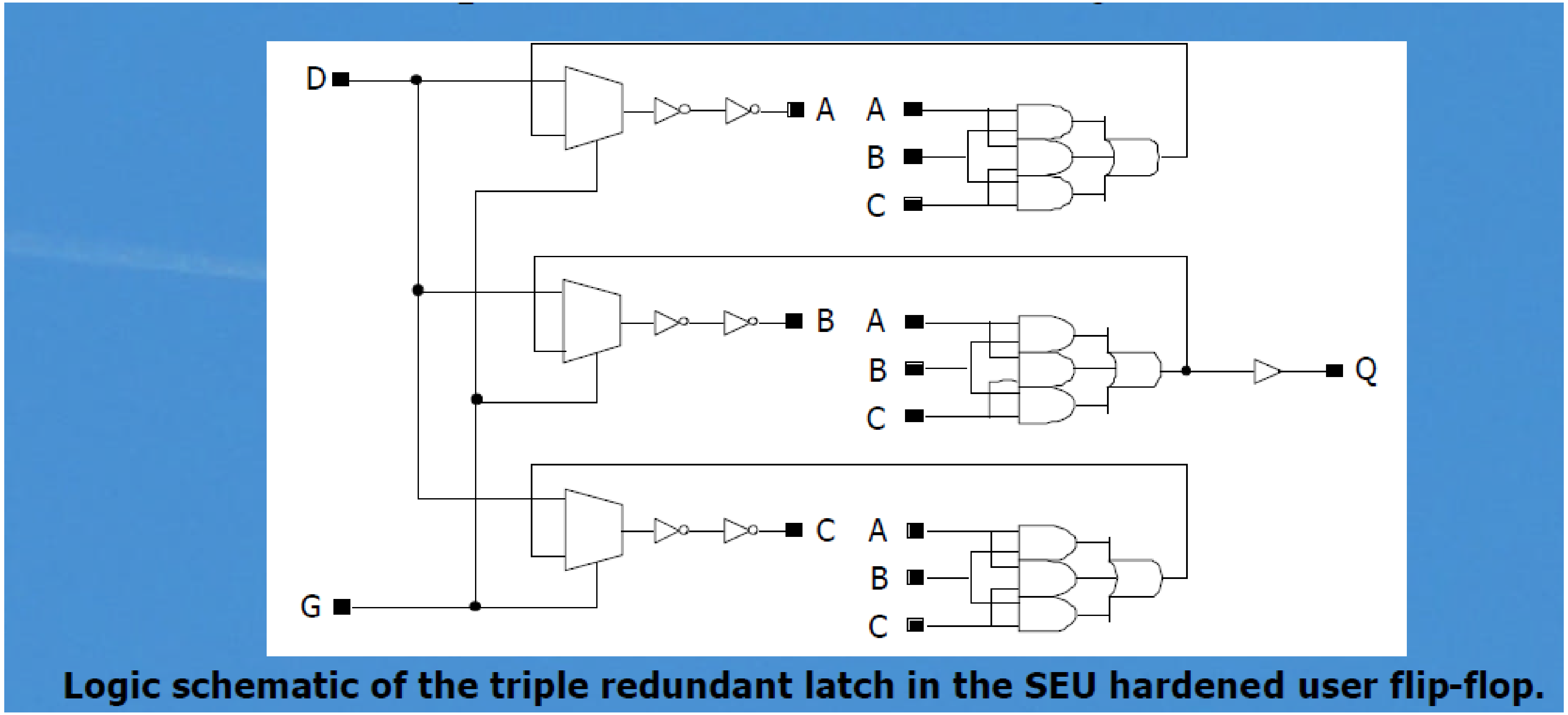
Modulation by probability and collection efficiency



Precautionary mesure
(cost tradeoffs)



Many scheme of EDAC. Eg, for a flip-flop



Logic schematic of the triple redundant latch in the SEU hardened user flip-flop.

The same data is written in three memories (latch)

Three comparators feed the majority vote back into each flip-flop

At the price of area and power added.

Atmospheric neutrons effects
Wrap-Up and Documentation .

- **Upset Rate increases for three causes:**
  - **Information and data more sensitive:**
  - **Critical Charge downscaling according to Moore's Trend and I.T. progresses**
  - **Frequency increase**
  - **System complexity upscaling**
  - **Protective circuit at low design level only and cumbersome**
- **To know more**
  - **Flash-based FPGAs in space, design guidelines and trade-off for critical Applications**
  - **"Soft Errors From Particles to Circuits, Jean-Luc Autran and Daniella Monteanu", CRC Press, 2015**
  - **Robert Baumann, Consultant, Radiosity Inc https://radiositysolutions.com/, in several IEEE Nuclear and Space Radiation Effects Conference Short Courses, eg** "Landmarks in Terrestrial Single-Event Effects", Invited Talk, Invited Short-Course, NSREC 2013

- **Some Standardization and Methods**
  - **Gound level, Manufacturers:**

    JEDEC Test Specification JESD-89 issued 2001, updated 2006, 2021 **"Measurement and Reporting Of Alpha Particle and Terrestrial Cosmic Ray Induced Soft Errors in Semiconductor Devices"**

    JESD89-1B "TEST METHOD FOR REAL-TIME SOFT ERROR RATE"
  - **Atmospheric, avionics:**

    IEC TC107 – 62396 TS – 2004 "**STANDARD FOR THE ACCOMODATION OF ATMOSPHERIC RADIATION EFFECTS VIA SINGLE EVENT EFFECTS WITHIN AVIONICS EQUIPMENTS"**
  - **Space Electronics:**

    ESA "SCC basic specification no 22900", issue 4, April 1995 and seq.

Conclusions and some thoughts (Single Event Effects)

1. Radiation Single Event Transient is a sort of ‘back-door’ command with risk of malfunction or hard failure.

2. The chip or circuit behavior is a category of a Real Time issue in an asynchronous mode:
   - Single Event Transient randomly occurs out of order at any time and node in the ‘space of configuration’ of the ‘machine’.
   - And only the design team or house knows the precise chip layout and has a model of ‘machine.
   - It is hard to find a worst case and test strategy is cornerstone.

3. At several circuit and system levels, the best is to include a ‘design for testability’, and a ‘hardening by design’.

4. Radiation effects on circuit and system are rather a mystery, but the firm grounds are in physics.

   Knowledge can be shared by convergence of interest in physics, technology and real-time
   - **Reliability and safety in Space Electronics and Transportation industries**
   - **Dependability and performance in Research Physics Instrumentation (Experimental Astrophysics and and High Energy Colliders)**
   - **Emerging large facilities for Fusion Research Reactors (a lot of electronics involved in the plasma diagnistics and command control).**

- Limited design approaches Test standards exist in some of these areas: Avionics, Space Electronics