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VMM Based Readout Prototype for the SoLID Detector at Jefferson Lab

We have designed a prototype board for the readout of GEM detectors in the future SoLID experiment at JLab. The readout board is based on the VMM front-end ASIC developed for the upgrade of the ATLAS muon detectors at the CERN Large Hadron Collider. For use in triggering applications the VMM can continuously and simultaneously produce 6-bit ADC values for hits in each of the 64 channels. If the pulse processing circuitry of the VMM is reset after the fast 6-bit conversion and data output, the effective dead time per hit can be reduced to a level acceptable for SoLID. We focus on using this data path for the readout of the detector.
Our prototype board supports 2 VMM ASICs (128 channels). A Xilinx Kintex UltraScale FPGA collects the 128 streams of 6-bit serial data clocked at up to 320 MHz. Upon receipt of a trigger the FPGA captures a programmable time window of hit data and packages it for readout. Dual readout paths have been implemented. The radiation hard fiber optic readout path employs the CERN GBTx and VTRx data transport components. For test setups and low radiation environments there is an SFP+ fiber transceiver capable of 1Gb or 10Gb Ethernet.

We have assembled a system consisting of 512 channels and connected it to a GEM detector. Measurements on the high-rate performance of the system will be shown.

Minioral

Yes

IEEE Member

No

Are you a student?

No

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