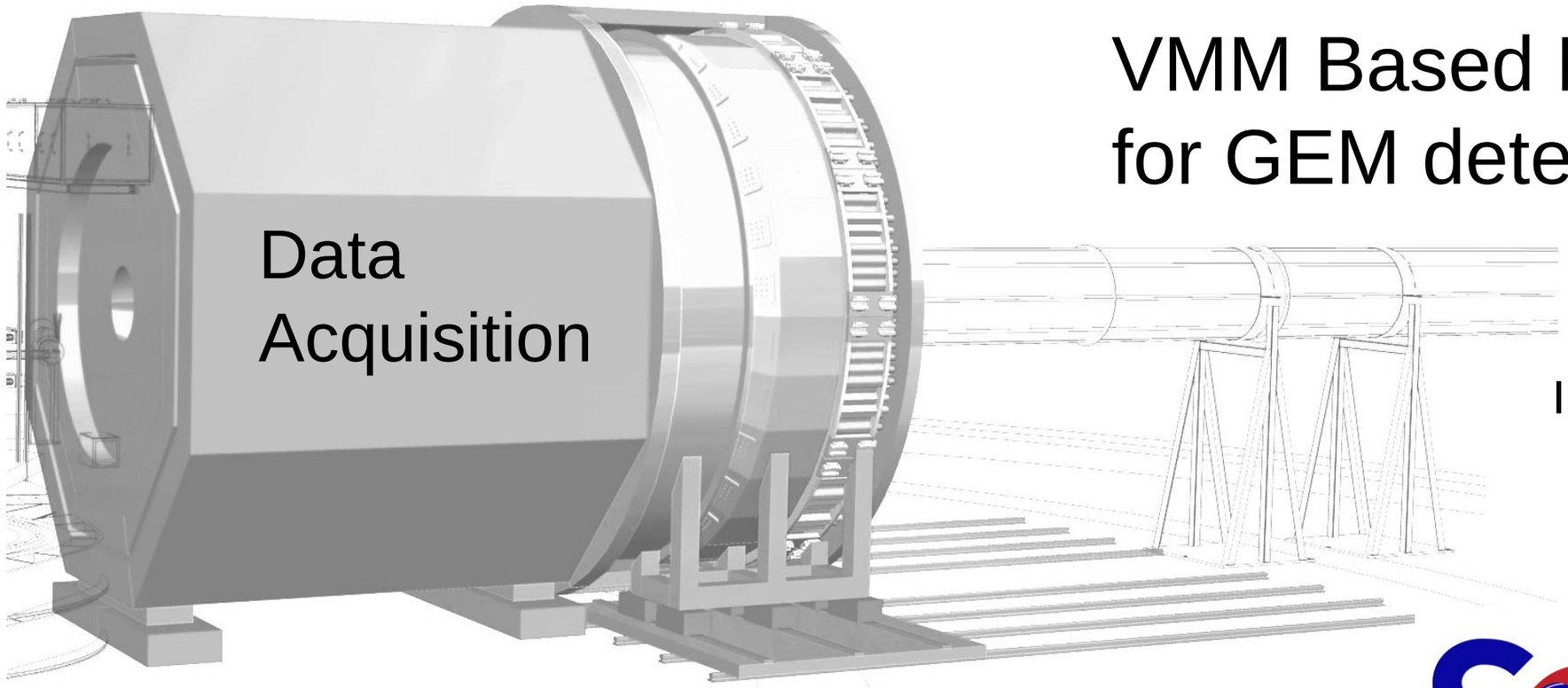


VMM Based Readout Prototype for GEM detectors

Data Acquisition

IEEE Real Time Conference
August 2022

SOLENOIDAL LARGE INTENSITY DEVICE

Ed Jastrzembski

Jefferson Lab Fast Electronics – DAQ Group

JSA | U.S. DEPARTMENT OF ENERGY | Office of Science | SoLID | Jefferson Lab

Ed Jastrzembski, Jeff Wilson, Ben Raydo, Bryan Moffit, Chris Cuevas, William Gu, David Abbott, Fernando Barbosa, Cody Dickover, Hai Dong, Shifaben Vahora
Jefferson Lab Fast Electronics – Data Acquisition Group

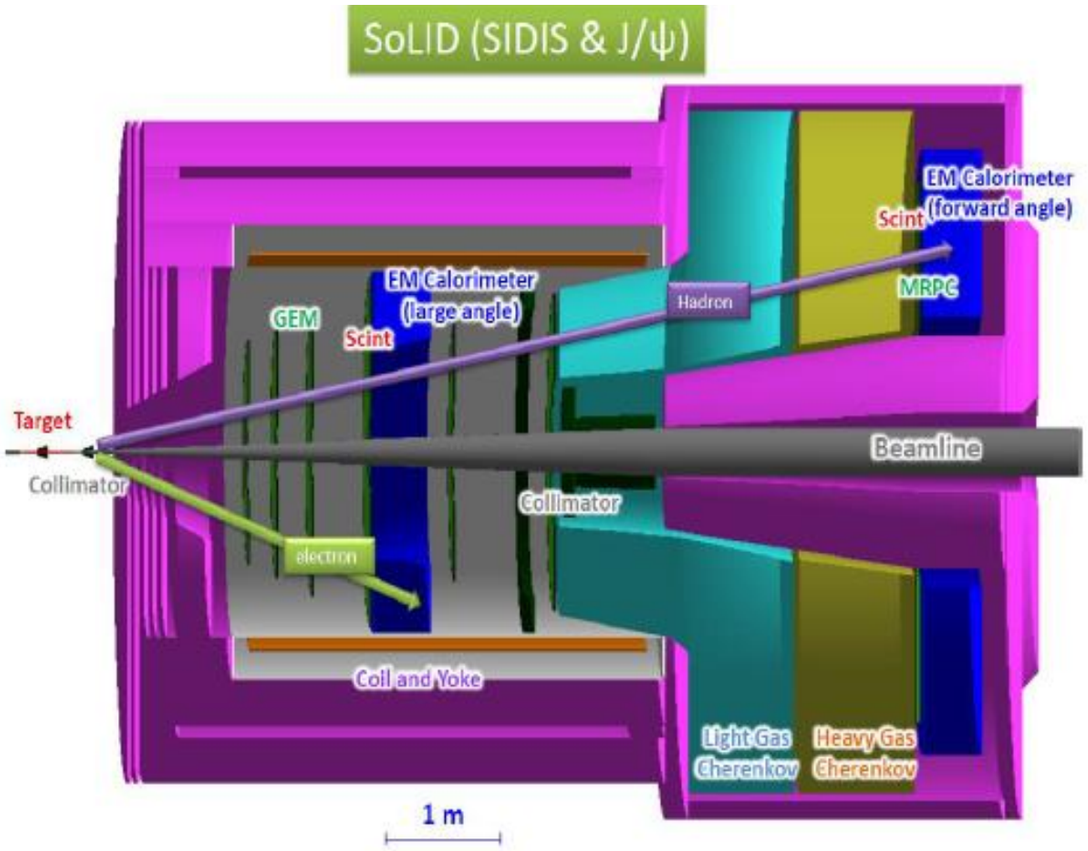
Alexandre Camsonne
Jefferson Lab Hall A / SoLID Experiment

Xinzhan Bai
University of Virginia / SoLID Experiment

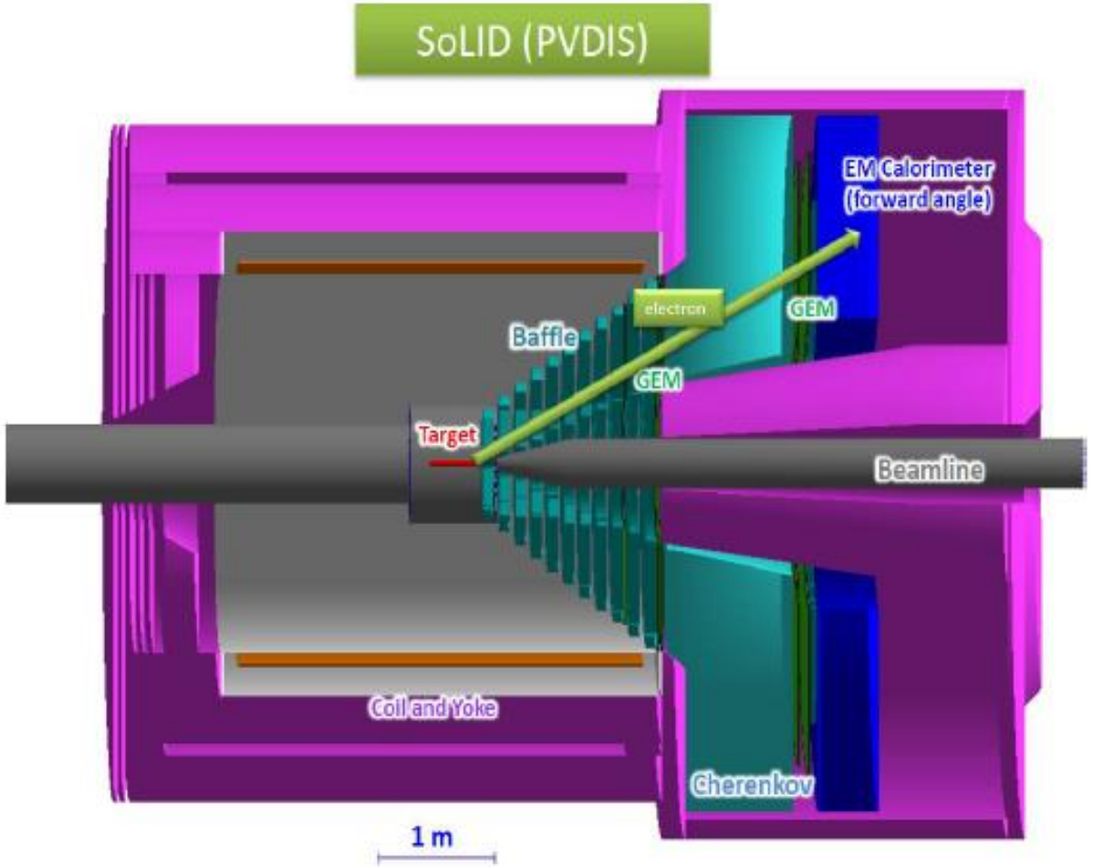
Solinoidal **L**arge **I**ntensity **D**evice

Nucleon Structure Study

Semi-Inclusive Deep Inelastic Scattering



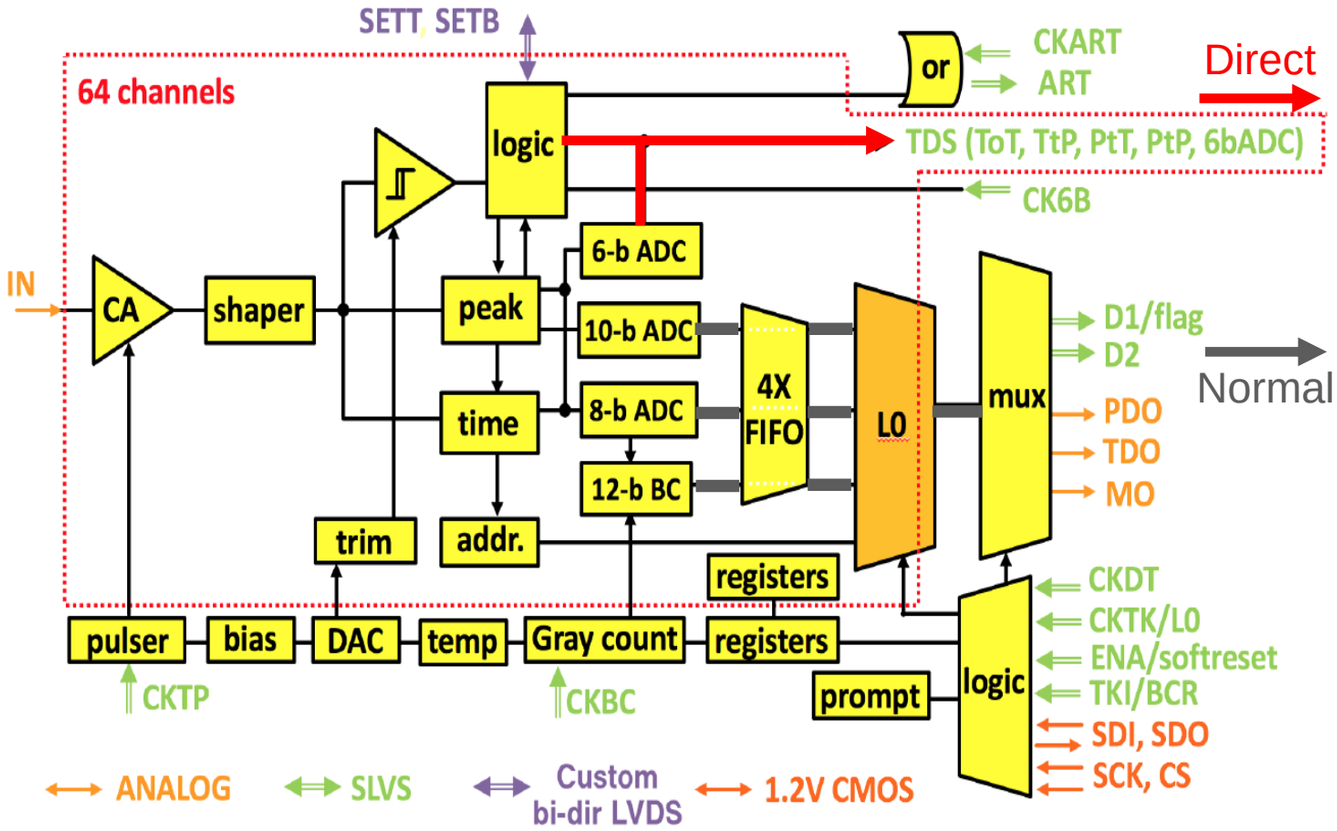
Parity-Violating Deep Inelastic Scattering



(ref 1)

VMM chip

VMM3 block diagram



(ref 2)

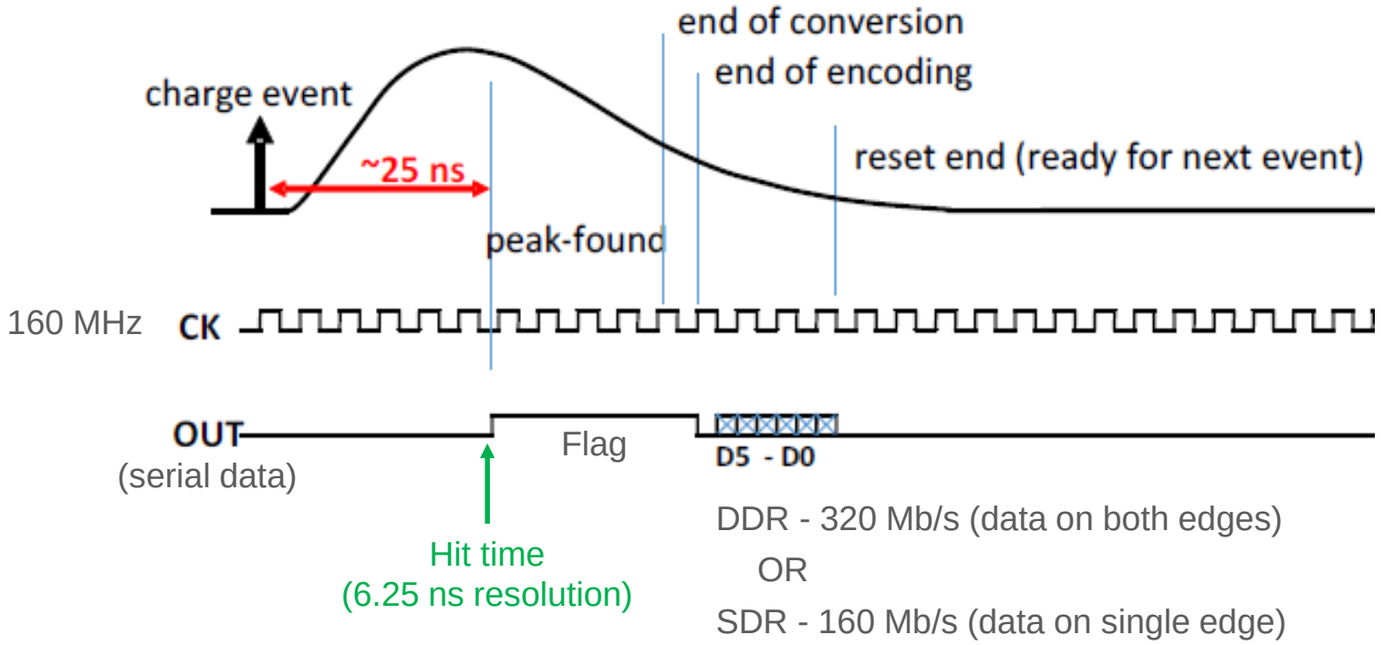
- ASIC for ATLAS New Small Wheel
- Radiation hard similar to APV25 : > 100 Mrad
- 64 channels
- Low noise over wide range of input capacitance (<1 pF to ~1 nF)
- Shaping times : **25 ns**, 50 ns, 100 ns, 200 ns
- Pulse amplitude proportional to charge at input
- Gains : 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
- **6 bit ADC (25 ns conversion)** and **10 bit ADC (220 ns conversion)**, 8 bits TDC (1 ns resolution), 12 bits Beam Crossing time stamp
- 4 MHz of rate per channel thanks to multilevel FIFO
- Continuous or triggered readout on normal data path
- Latency up to 16 μs in triggered mode
- **Fast direct outputs (64 channels) for ATLAS trigger (6b ADC, ToT)**
- Normal data link up to 320 Mb/s

SoLID prototype goals for VMM

- Flux of 1 MHz/cm^2 results in rates of several MHz for some GEM strips
- Need to minimize front-end dead time and be able to read out high data volume resulting from trigger rates beyond 100 KHz
- The VMM3 chip offers a fast 6-bit A/D conversion of the peak amplitude, resulting in a dead time of ~65 ns. We will try to use this as the readout mode for the GEMs.
- Need to implement VMM3 prototype to test if this *fast direct readout* mode produces data with quality sufficient for tracking in high backgrounds
- If it does, identify possible final readout board architecture for VMM3

VMM 6-bit Direct Output data format

Peak amplitude converted to 6-bit value

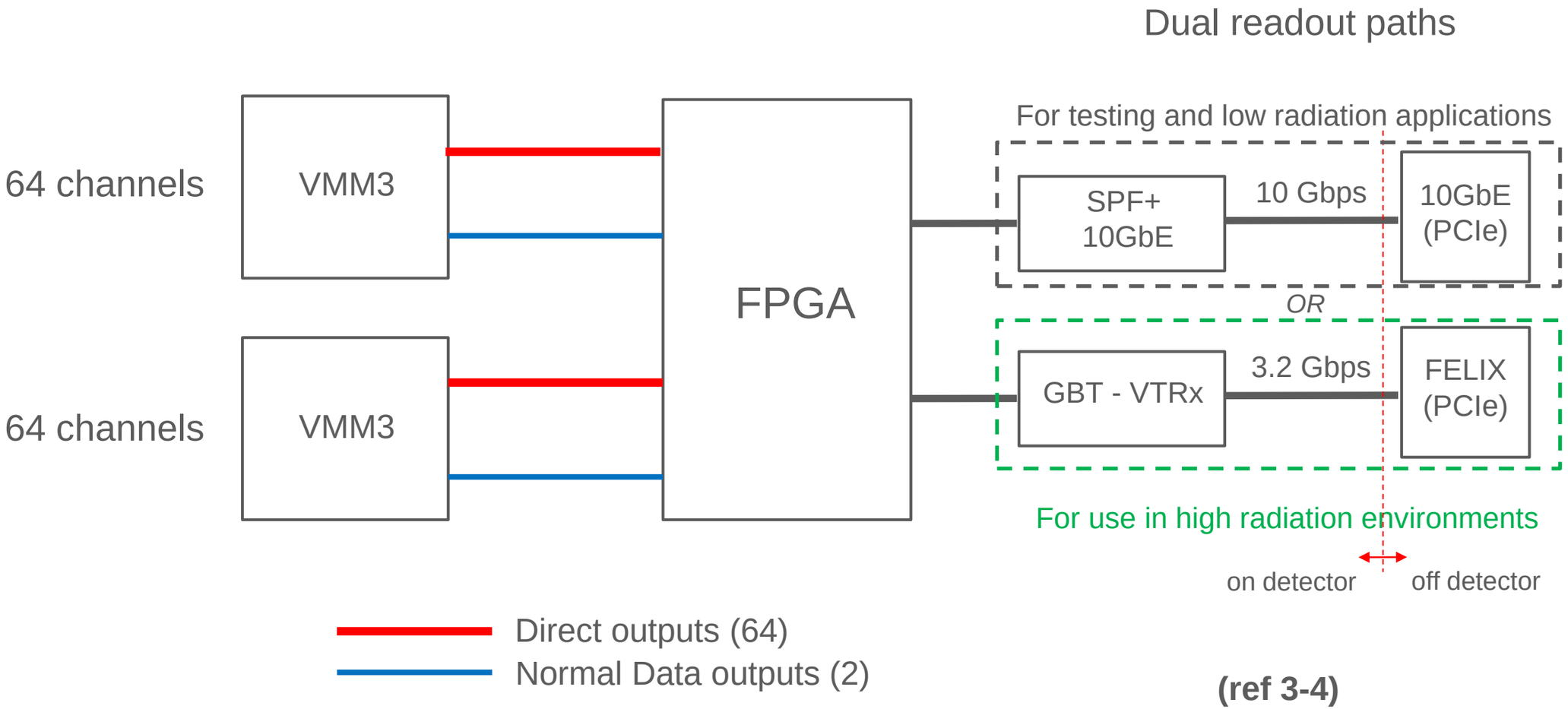


DDR - 320 Mb/s (data on both edges)

OR

SDR - 160 Mb/s (data on single edge)

Concept for VMM prototype readout



(ref 3-4)

VMM3 Prototype Board

- **Xilinx Kintex UltraScale FPGA (KCKU040)**
  - Compatible with receiving low level **SLVS** signals from VMM3
  - Good immunity against radiation induced ‘latch-up’
  - Detect and correct radiation induced SEUs (Single Event Upsets) in configuration memory with Xilinx IP
  - Use redundant design techniques (TMR –Triple Modular Redundancy) to mitigate against SEUs in user logic
  - 10 Gb Ethernet readout for testing and low radiation applications
  - CERN GBT – VTRx – FELIX readout for high radiation environments (ref 3-4)
- **Support components also sensitive to the effects of radiation**
  - Power components (linear regulators, DC-DC converters)
  - Commercial grade (COTS) power components can fail – no mitigation techniques available
  - Can use rad hard CERN bPOL DC-DC converters for point of load power
  - Many voltages required: VMM: 1.2V analog, 1.2V digital

    FPGA: 0.95V, 1.2V, 1.8V, 2.5V; FPGA serial transceivers: 1.0V, 1.2V, 1.8V

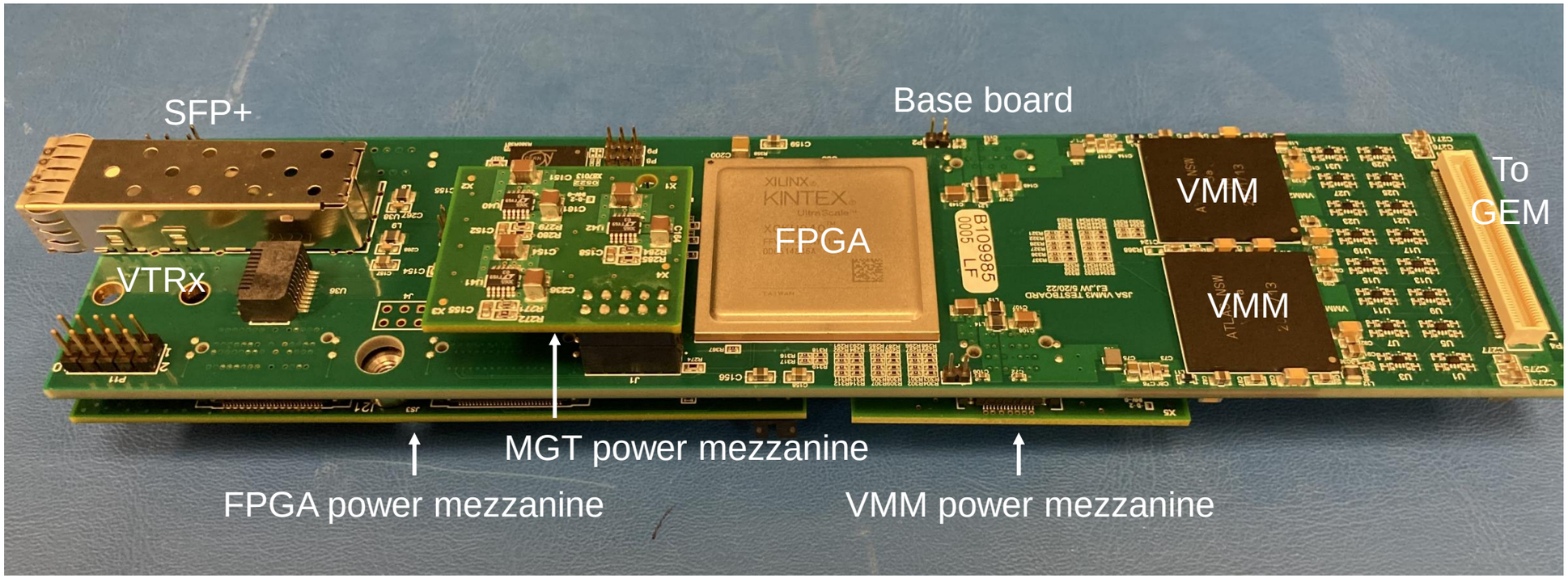
    GBT, GBT-SCA: 1.5V; VTRx: 2.5V; SPF+ (10 Gb Ethernet): 3.3V

Implementation strategy

- Board width (128 channels) constrained to **50mm** due to pitch of GEM detector strips
- Place all power components and signal interface ICs on mezzanine boards
- Gives additional board surface area required for these components
- Initial power using COTS components – can be final configuration for low radiation applications
- Construct mezzanine boards with CERN bPOL power components for radiation tolerant solution
- Alternative solution - mezzanine boards can accept cables from remotely located power supplies

Prototype assembly

128 channels



50 mm x 215 mm

Status and plans

- 6 complete readout board assemblies constructed (with COTS power)
- 1Gb Ethernet readout firmware implemented and tested (hardware is 10Gb capable)
- Data processing and formatting firmware implemented and tested
- Pulsed built in test capacitors of VMM inputs – resulting 6-bit ADC data read out

Next

- Get VMM normal data path (10-bit ADC) working
- Connect to GEM – evaluate data from cosmic rays and radioactive source
- Low intensity beam tests with existing hardware and firmware
- High intensity beam tests - depending on radiation levels *may* require rad hard power, GBT-FELIX readout, Triple Modular Redundancy (TMR) firmware

References

[1] *JLab SoLID Program*, https://indico.cern.ch/event/799284/contributions/3478747/attachments/1894383/3124966/Chen-HiX2019-SoLID.pdf

[2] *The VMM ASIC*, https://indico.fnal.gov/event/46746/contributions/210446/attachments/141147/177643/2021_03_18_Iakovidis_VMM_CPAD.pdf

[3] *GBT Project Status*, https://indico.gsi.de/event/3446/contributions/15320/attachments/11088/13570/2015.04.09_GMazza-GBT_GSI_9Apr2015.pdf

[4] *FELIX: The new detector readout system for the ATLAS experiment,* http://iopscience.iop.org/article/10.1088/1742-6596/898/3/032057/pdf

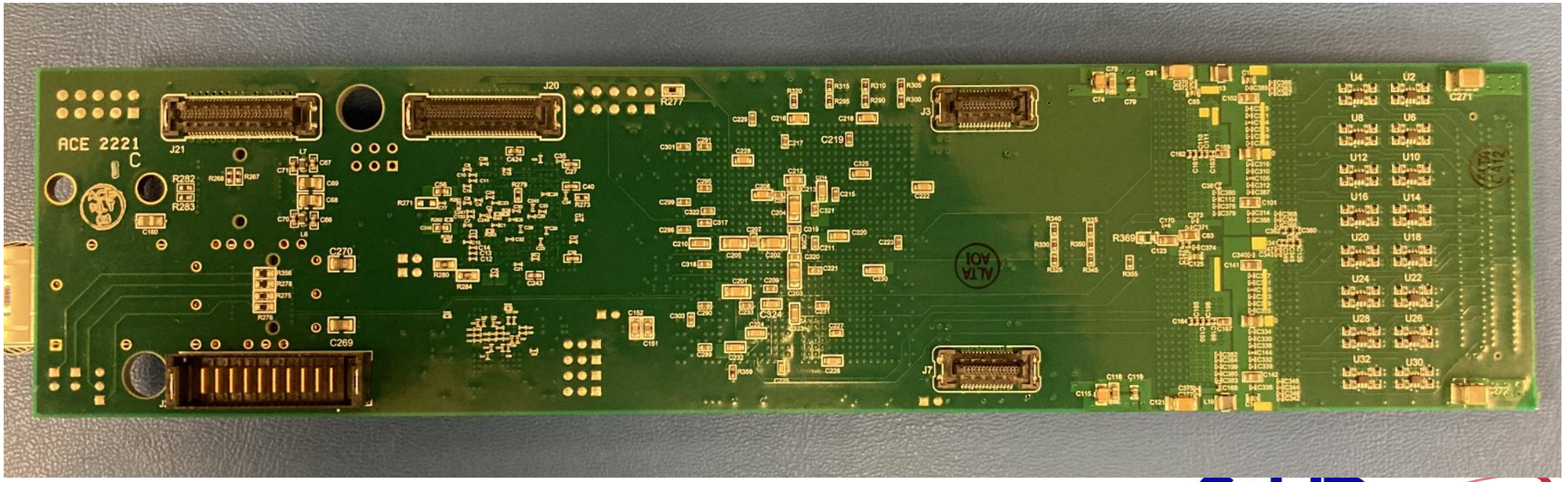
Supplemental SLIDES

Prototype base board

- Only FPGA + radiation hard components (VMM, GBT, GBT-SCA, VTRx).
- Even though focus is on low resolution (6-bit) ADC readout, design for low noise so that 10-bit ADC readout will perform well.
- Extensive VMM power filtering circuits allows switch mode power supplies (CERN bPOL) to be used. (Circuits copied from ATLAS *mmfe8* design.)
- 20-layer PCB – many ground layers. Stripline controlled impedance design for 100 ohm differential signals. No digital signals cross any cut lines of power distribution planes.
- Isolate analog and digital grounds of VMM with cut lines – joined at power entry points (modelled after *mmfe8* design).

Base board

Top

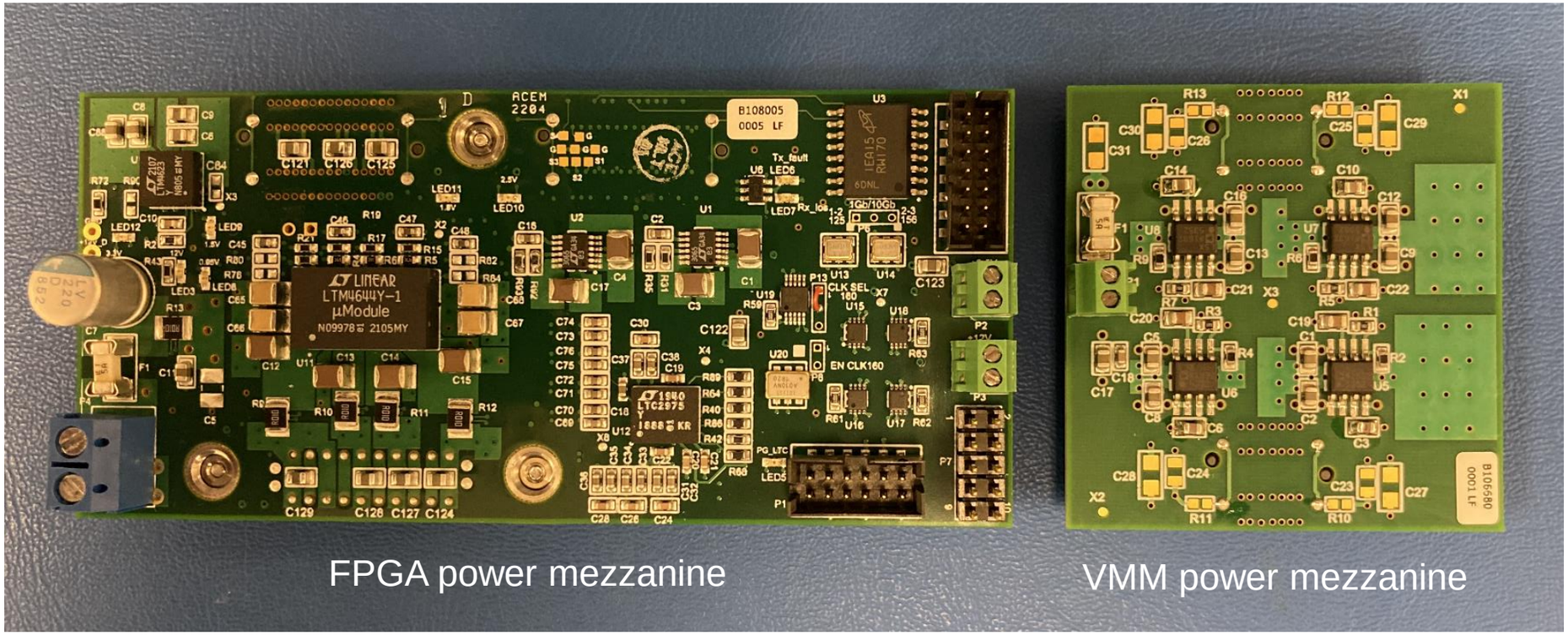


Bottom

Power mezzanine boards

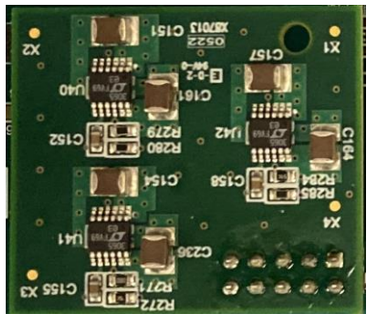
- Initial versions use commercial grade components. Can be replaced with rad hard versions using CERN bPOL components. (No changes to base board.)
- Samtec *floating* connectors (FT5 series) join base board with mezzanine boards that have multiple connectors. (Relaxes positioning tolerance of connectors.)
- FPGA power mezzanine
  - 12V input; 2.5V and 12V outputs to VMM power mezzanine board
  - Voltages for FPGA core and I/O, Ethernet transceiver, GBT, GBT-SCA, VTRx
  - LTC2975 PMBus controller monitors input voltage/current, FPGA voltages/currents. Supports supply sequencing, fault handling.
  - Connections for global control signals (clock, trigger, sync, busy) when Ethernet readout used
  - EEPROM and JTAG interface for FPGA
- VMM power mezzanine
  - Separate analog and digital power for each VMM (4 low-noise linear regulators)
- MGT power mezzanine
  - Voltages for Multi-Gigibit Transceivers of FPGA (3 low noise linear regulators). For 1/10 Gb Ethernet.

Mezzanine boards

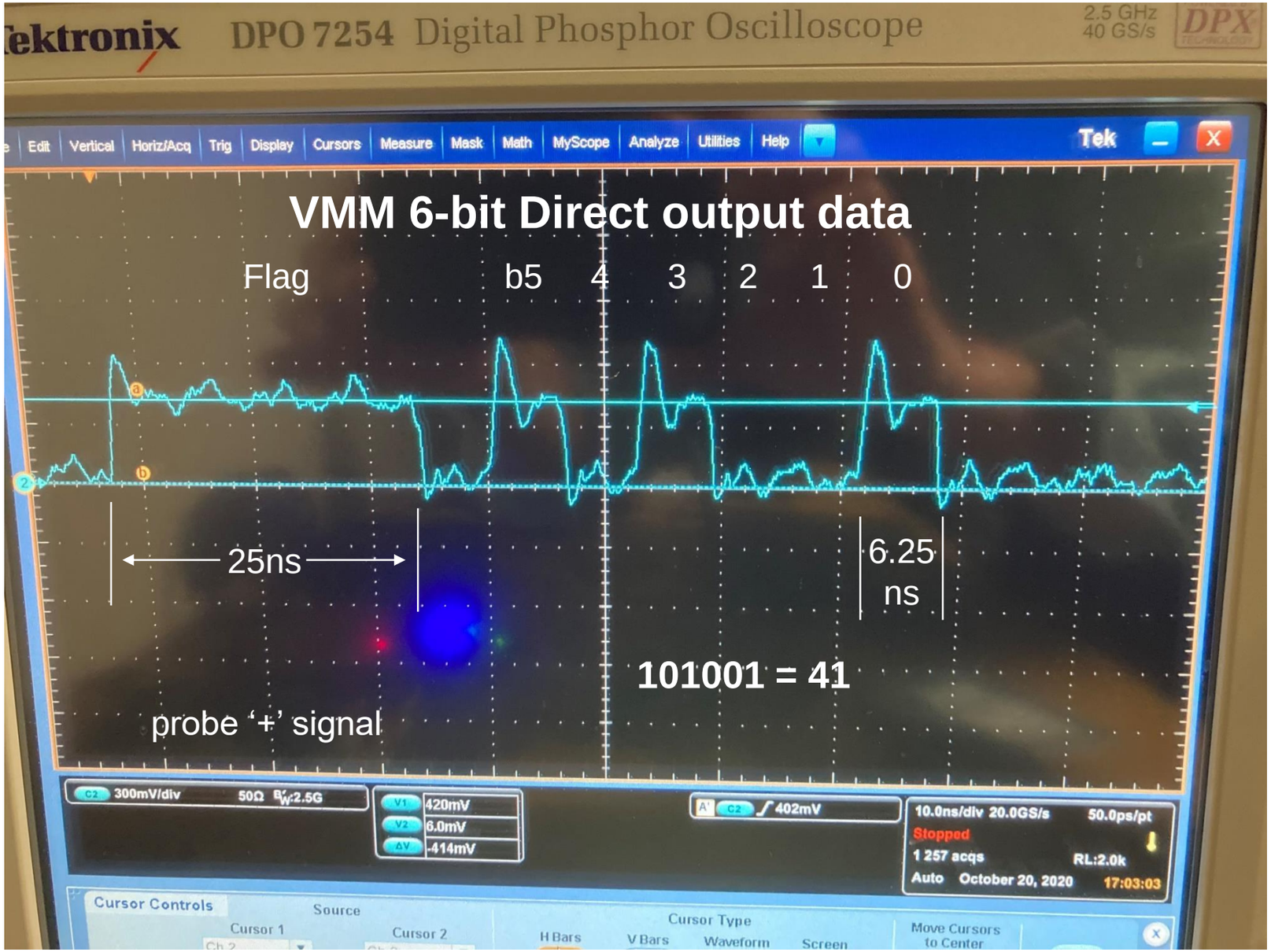


FPGA power mezzanine

VMM power mezzanine



MGT power mezzanine



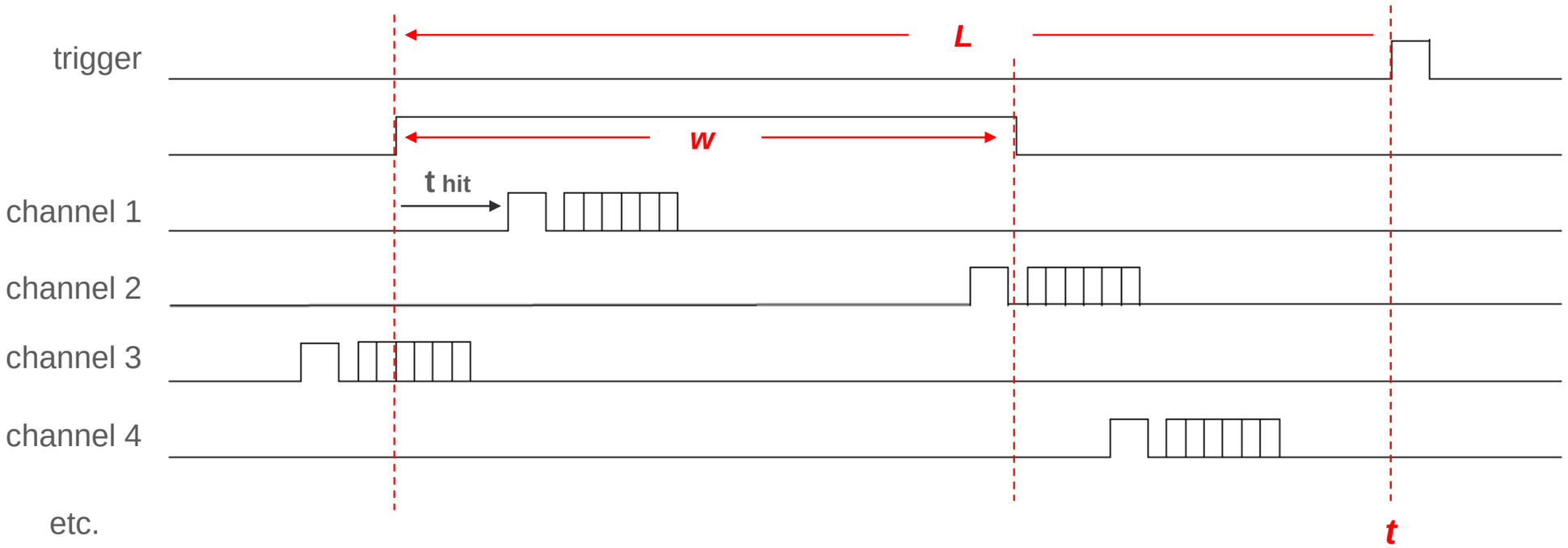
SDR - 160 Mb/s

41 x 16 = 656
consistent with
10 bit data avg

FPGA function

- Direct output data from the VMM3 chips is continuously written into a circular buffer in the FPGA.
- Let ***L*** be the trigger latency (L < 6.4 μs) and ***w*** be the data capture window size (w < 1.6 μs)
- Upon receipt of a trigger at time ***t***, data corresponding to the time period [***t*** – ***L***, ***t*** – ***L*** + ***w***] is captured and formatted for transmission off the chip

Conceptually

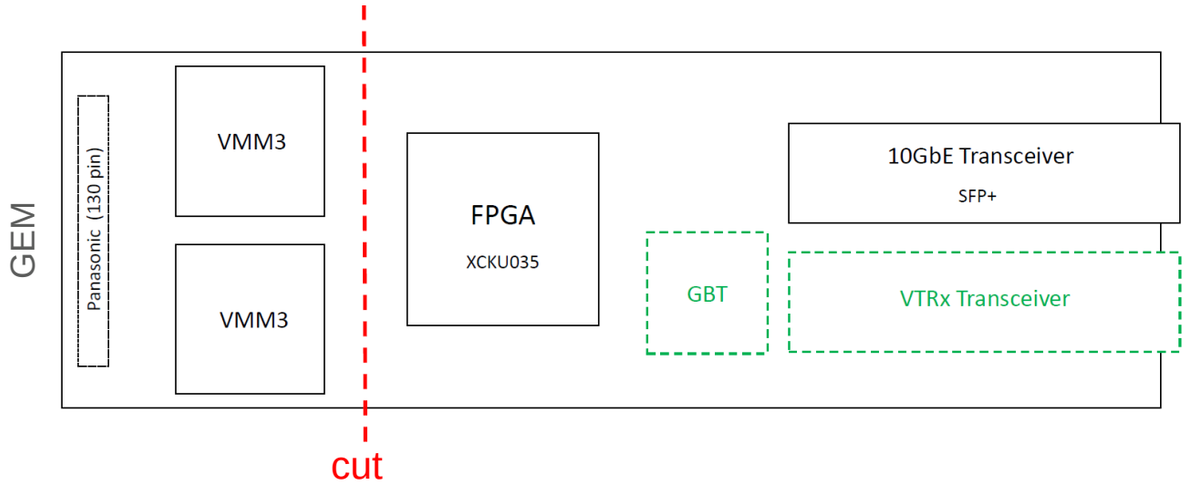


VMM readout card options for high radiation

(1) Connect GEM to readout card with cable. Locate readout card in lower radiation zone.

(2) Split readout card into 2 pieces

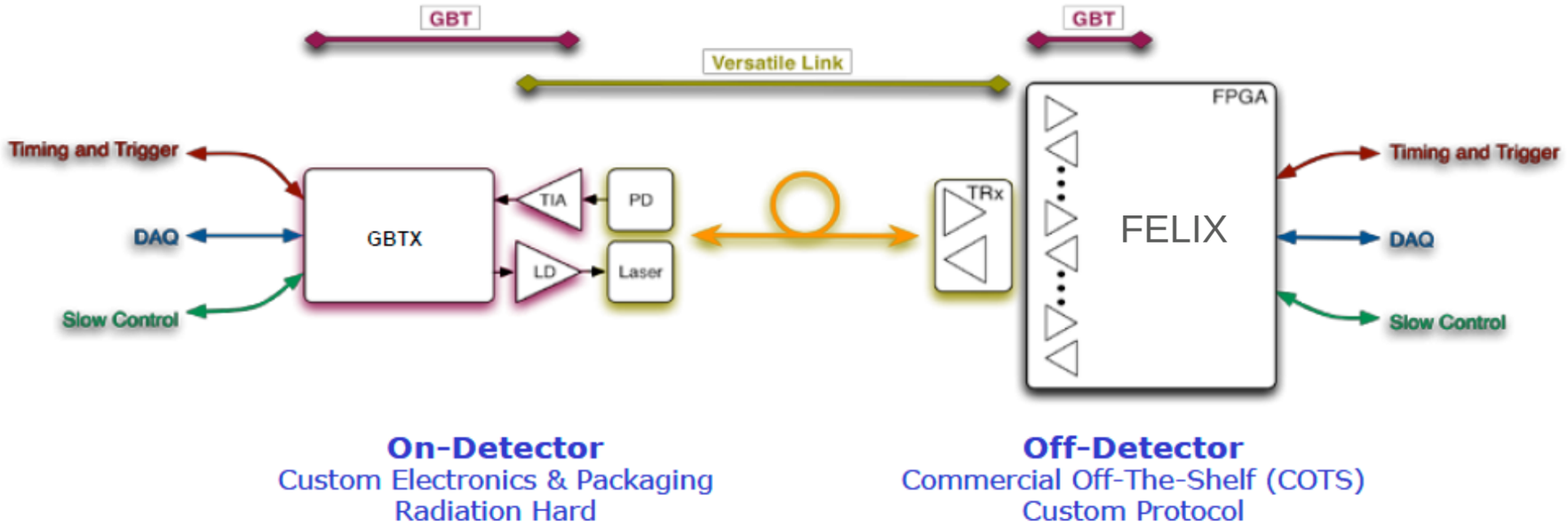
- carry digital signals across with cable or flex circuit
- locate section with FPGA in lower radiation zone



(3) Convert FPGA design into rad hard ASIC

- initiated contact with designers of the ATLAS VMM, ROC, and TDS ASICs to find out about the process and cost

GBT - VTRx link

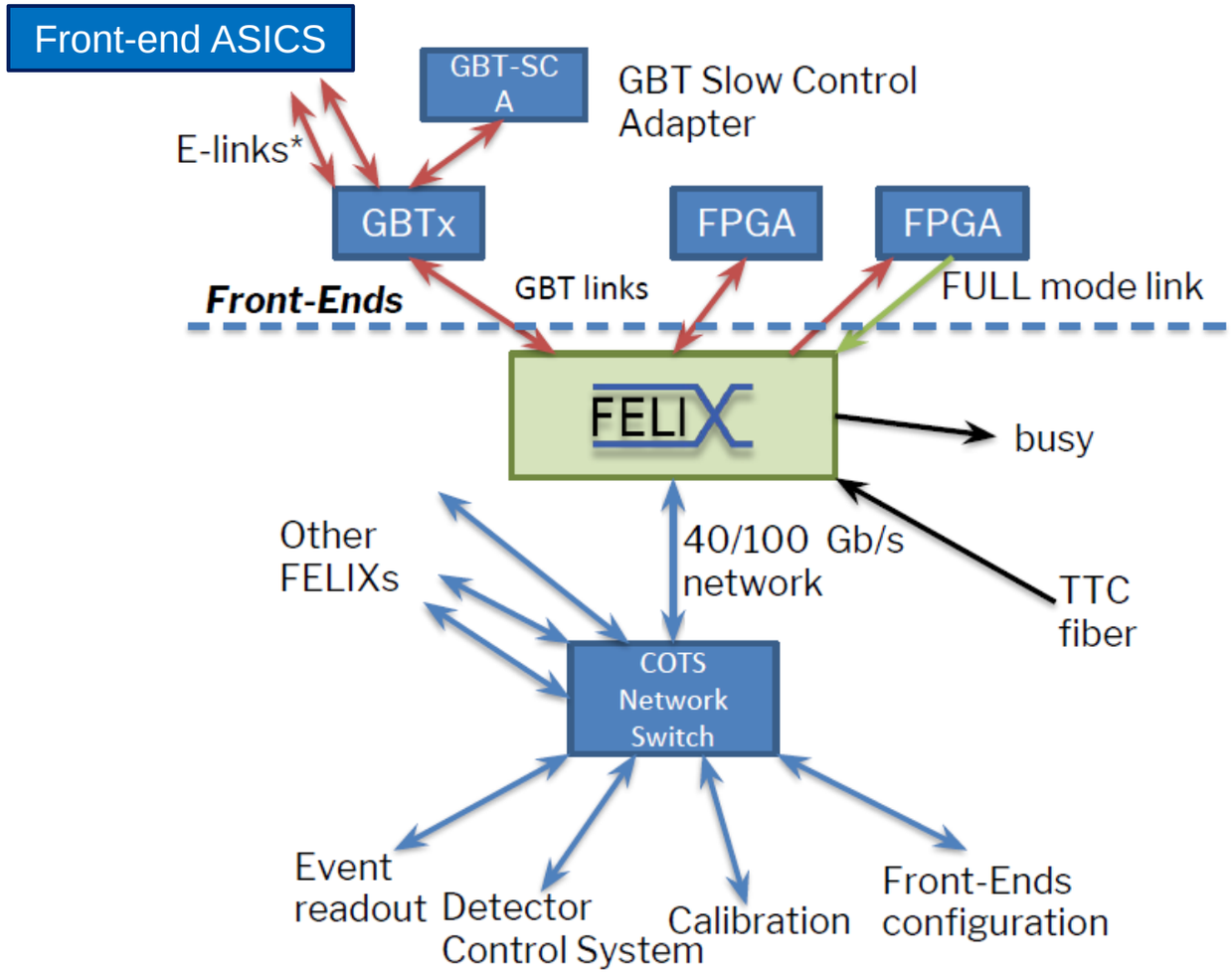


Single bidirectional rad hard optical link simultaneously provides data paths for:

- Timing and Trigger Control (TTC)
- Data Acquisition (DAQ)
- Slow Controls (SC) – configuration and monitoring

Fixed Latency

FELIX



- FELIX is a router between front-end serial links and a commodity network, which separates data transport from data processing.
- Routing of detector control, configuration, calibration, monitoring and detector event data
- TTC (Timing, Trigger and Control) distribution integrated
- Configurable E-links in GBT Mode
- Detector independent

FELIX hardware implemented in PCIe Gen3