# A 10-bit Resistor-Floating-Resistor-String DAC for Multi-Voltage Threshold Digitizer in PET

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***Abstract*— This work presents a low-area and high-precision 8-channel 10-bit resistor-floating-resistor-string (RFR) digital to analog converter for multi-voltage threshold digitizer in PET medical imaging equipment. Two-stage segment structure is adopted to reduce the chip area, which the first-stage coarse quantization circuit can be shared among each channel. And the RFR-DAC combines a 6-bit RDAC and a 4-bit floating resistor string DAC to offer unique two-voltage-selection scheme without the need of unity-gain buffers to isolate parallel-connected resistor strings. At the same time, the optimal segmentation strategy is realized by mathematical modeling of the multi-channel RFR DAC segmentation strategy and the chip area. According to the demand characteristics for the multi-voltage threshold digitizer, the output voltage range of each channel is optimized to reduce the chip area. The 8-channel 10-bit RFR-DAC experimental prototype chip designed and implemented based on the 180-nm standard CMOS process has an core area of 670μm×880μm. The experimental results show that DNL of the prototype chip is ±0.07LSB, INL is ±0.55LSB, the output error voltage (DVO) is 0.8LSB, and the overall power consumption is 0.22mW.**

***Index Terms*— DAC, RFR-DAC, low-area, high-precision, PET, MVT, digitizer.**

## I. Introduction

The multi-voltage threshold (MVT) is an amplitude-based sampling method, which is used to sample the PET event waveform at the earliest possible stage of the signal detection chain. This approach can greatly reduce the complexity of PET front-end electronics and has the potential to overcome technical issues that may arise when fast ADCs are needed. The reduced electronic complexity can also lead to reduction in production cost and power consumption[1].

The accurate reconstruction of MVT front-end readout system depends on the accurate setting of threshold voltage. Therefore, multi-channel high-precision DAC is very important for the overall performance of front-end readout system. In this work, we present a low-area and high-precision 8-channel 10-bit digital to analog converter (DAC), with the main purpose to support higher time resolution of the whole PET system.

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## II. ASIC Description

The block diagram of the RFR-DAC is illustrated in Fig. 2. The proposed DAC is composed of a data latch circuit, a global circuit and 8-channel circuits. The data latch circuit is composed of seven 9-bit latches and one 8-bit latch in parallel. The input data of eight channels can be configured asynchronously and independently, mainly to complete the latch buffer of the input codeword. The global stage is composed of global resistor string, bandgap reference circuit, global bias circuit, global shared current source and current slot module. It provides shared coarse quantization voltage and shared global compensation current source and current slot for

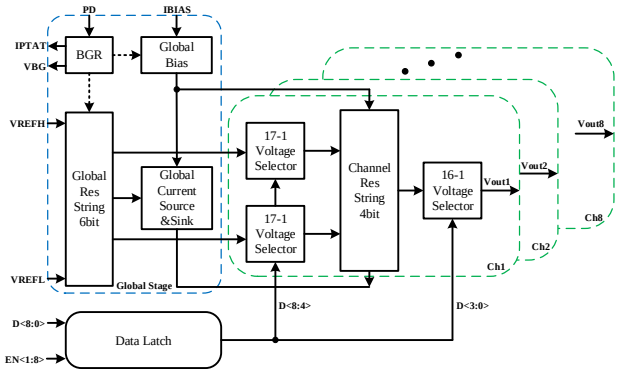


Fig.1. The diagram of the proposed DAC

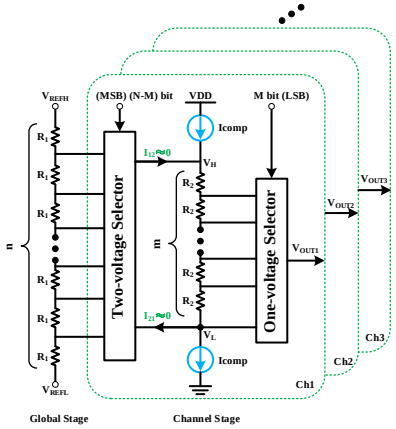


Fig.2. Architecture of RFR-DAC with two-voltage-selection scheme.

8-channel stages. Except for different output ranges, the 8-channel circuits are composed of two 17-1 voltage selectors, channel resistance string and 16-1 voltage selector, which are responsible for completing the second stage fine quantization and outputting the final result.

### A. *Segmentation strategy optimization*

The first stage global resistance string and the second stage channel resistance string are respectively composed of two kinds of resistors with resistance values of R1 and R2 in series, the area occupied by the resistance array formed by the two is actually proportional to the number of the two kinds of resistors. Therefore, as long as the sum of the number of two resistors in the whole chip is minimized, the overall area optimization can be achieved. In order to reduce the chip area, the number of resistors is modeled mathematically.

According to the Fig. 2, the total number of resistors required for 8-channel 10-bit RFR-DAC is:

$$Z_{total} = 2^{N-M} + 8 \times 2^{M}$$

then,

$$\frac{\partial Z_{total}}{\partial M} = (2^{M+3} - 2^{N-M}) \times ln\, 2$$

and ,

$$(2^{M+3} - 2^{N-M}) \times ln\, 2 = 0 \Rightarrow M = \frac{N-3}{2}$$

Where N = 10 is the resolution of RFR-DAC, and the optimal value M=3.5. Consider the regulation range of voltage in the 8-channel, we chose M=4.

### B. *Channel output range optimization*

The output voltage VTH1~VTH8 of 8-channels has an obvious size relationship (VTH1<VTH2<VTH3<VTH4< VTH5<VTH6< VTH7<VTH8), the DAC designed in this work should be strictly monotonic. According to this information, the chip area consumption caused by the overlap of output ranges between channels can be reduced, so as to reduce the chip area. In this work, the output range between adjacent channels of RFR-DAC is designed to have a certain overlap margin to meet the expansion requirements of DAC output range.

| Ch | Output LSB ($V_{LSB1}$) | Full range ($V_{LSB1}$) | Output voltage（mV） @ $V_{REF}$ =1.25V |
|---|---|---|---|
| 1 | 1 ~ 18 | 18 | 19.53125 ~ 350.34180 |
| 2 | 8 ~ 25 | 18 | 156.25000 ~ 487.06055 |
| 3 | 15 ~ 32 | 18 | 292.96875 ~ 623.77930 |
| 4 | 22 ~ 39 | 18 | 429.68750 ~ 760.49805 |
| 5 | 29 ~ 46 | 18 | 566.40625 ~ 897.21680 |
| 6 | 36 ~ 53 | 18 | 703.12500 ~ 1033.93555 |
| 7 | 43 ~ 60 | 18 | 839.84375 ~ 1170.65430 |
| 8 | 50 ~ 63 | 14 | 976.56250 ~ 1229.24805 |

## III. Experimental Results

The prototype chip was manufacturing. The post-simulation results of DNL, INL and DVO is illustrated in Fig. 4~6. DNL is ±0.07LSB, INL is ±0.55LSB, DVO is 0~0.8LSB,

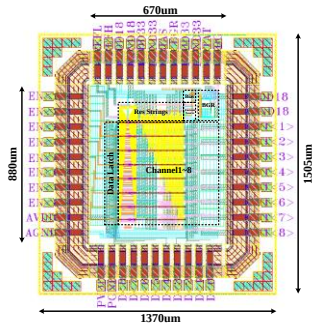


Fig.3. Layout of the prototype chip.

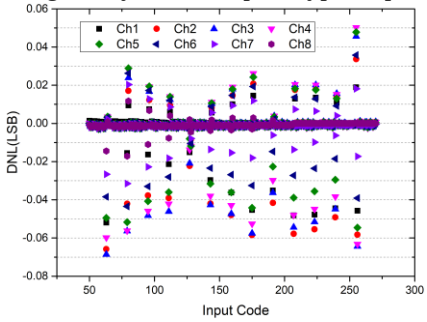


Fig.4. Measured DNL versus input code.

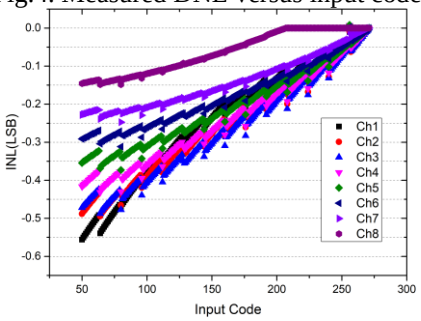


Fig.5. Measured INL versus input code.

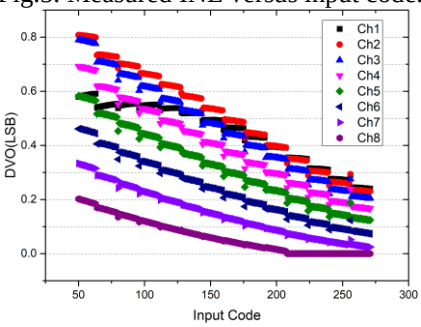


Fig.6. Measured DVO versus input code.

## IV. Conclusion

A low-area and high-precision 8-channel 10-bit RFR-DAC was presented in this work. The proposed architecture of the DAC is proved to have great potential for multi-voltage threshold digitizer in PET.

## References


[1] Q. Xie, C. M. Kao, Z. Hsiau, and C. T. Chen, "A New Approach for Pulse Processing in Positron Emission Tomography," *IEEE Transactions on Nuclear Science*, vol. 52, no. 4, pp. 988-995, 2005.