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A 10-bit Resistor-Floating-Resistor-String DAC for Multi-Voltage Threshold Digitizer in PET

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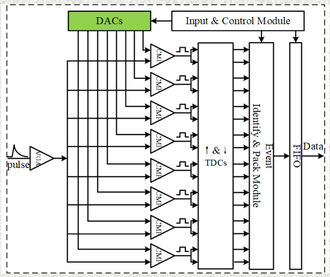
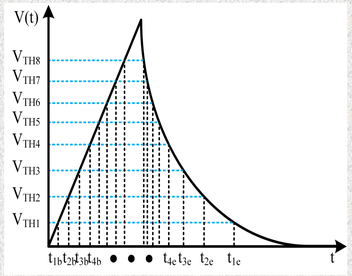
Abstract

This work presents a low-area and high-precision 8-channel 10-bit resistor-floating-resistor-string (RFR) digital to analog converter for multi-voltage threshold digitizer in PET medical imaging equipment. Two-stage segment structure is adopted to reduce the chip area, which the first-stage coarse quantization circuit can be shared among each channel. And the RFR-DAC combines a 6-bit RDAC and a 4-bit floating resistor string DAC to offer unique two-voltage-selection scheme without the need of unity-gain buffers to isolate parallel-connected resistor strings. At the same time, the optimal segmentation strategy is realized by mathematical modeling of the multi-channel RFR DAC segmentation strategy and the chip area. According to the demand characteristics for the multi-voltage threshold digitizer, the output voltage range of each channel is optimized to reduce the chip area. The 8-channel 10-bit RFR-DAC experimental prototype chip designed and implemented based on the 180-nm standard CMOS process has an core area of 670μm×880μm. The experimental results show that DNL of the prototype chip is ±0.07LSB, INL is ±0.55LSB, the output error voltage (DVO) is 0.8LSB, and the overall power consumption is 0.22mW.

Introduction



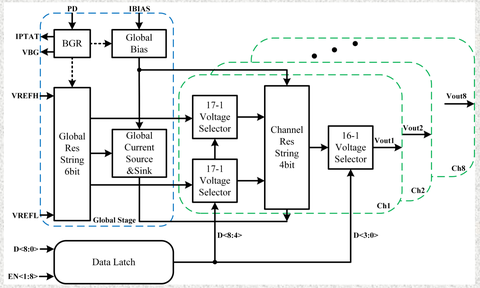
The block diagram of the 8-level MVT digitizing channel



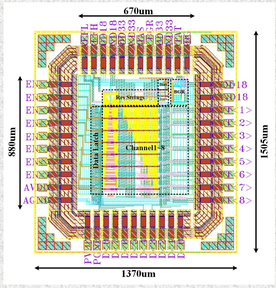
MVT sampling method for photodetector pulse signal.

The multi-voltage threshold (MVT) is an amplitude-based sampling method, which is used to sample the PET event waveform at the earliest possible stage of the signal detection chain. This approach can greatly reduce the complexity of PET front-end electronics. The accurate reconstruction of MVT front-end readout system mostly depends on the accurate setting of threshold voltage. A high resolution DAC with small size is required for the PET.

ASIC description



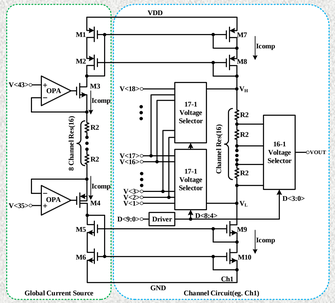
The diagram of the proposed ASIC

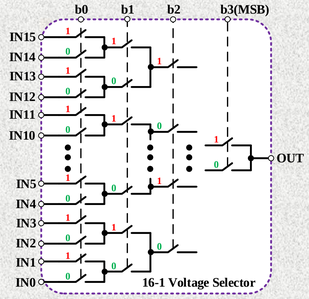


Layout of the prototype chip

The proposed ASIC is composed of a data latch circuit, a global circuit and 8-channel circuits. The global stage is composed of global resistor string, bandgap reference circuit, global bias circuit, global shared current source and current slot module. Except for different output ranges, the 8-channel circuits are composed of two 17-1 voltage selectors, channel resistance string and 16-1 voltage selector, which are responsible for completing the second stage fine quantization and outputting the final result.

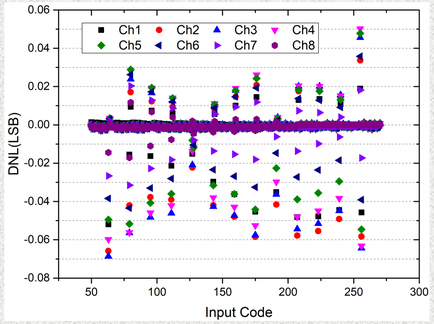
Circuit design



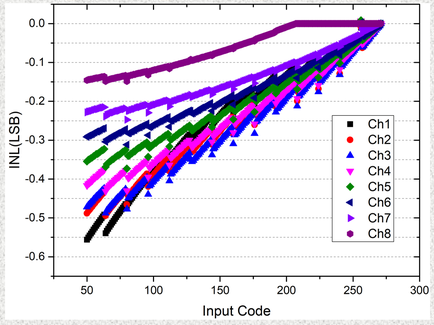


- Resistor-floating-resistor-string DAC(RFR-DAC)
- Optimal segmentation strategy: Global-6bit；Fine-4bit.
- Optimal output voltage range of each channel.
- Voltage selector with tree structure
- Complementary CMOS transistor switch

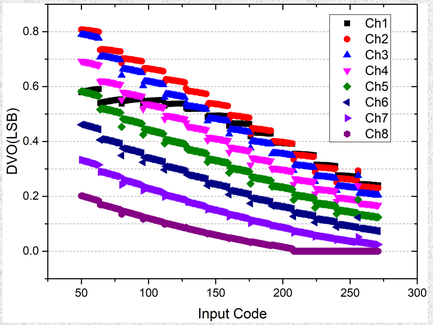
Experimental results



Measured DNL versus input code.



Measured INL versus input code.



Measured DVO versus input code.

Summary

- A low-area and high-precision 8-channel 10-bit RFR-DAC was presented in this work. The proposed architecture of the DAC is proved to have great potential for multi-voltage threshold digitizer in PET.
- The 8-channel 10-bit RFR-DAC experimental prototype chip designed and implemented based on the 180-nm standard CMOS process has an core area of 670μm×880μm.
- The experimental results show that DNL of the prototype chip is ±0.07LSB, INL is ±0.55LSB, the output error voltage (DVO) is 0.8LSB, and the overall power consumption is 0.22mW.