CDEX


# Preliminary Design of CDEX-100 DAQ Achitecture

**Jingjun Wen, Tao Xue, Lin Jiang, Jianmin Li, Yinong Liu**

**Tsinghua University**
**On behalf of the CDEX Collaboration**

**August 1st 2022**

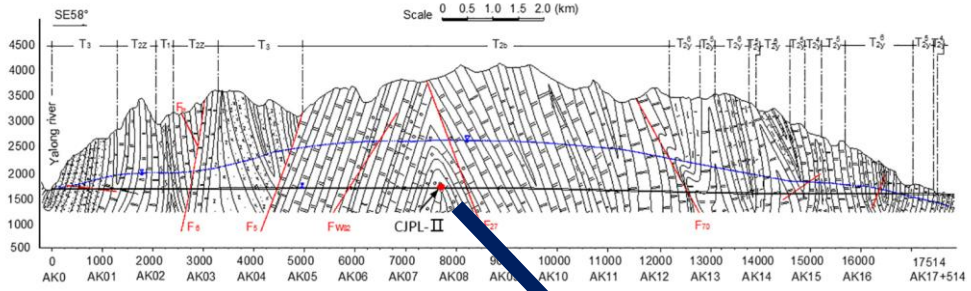
**23rd Virtual IEEE Real Time Conference**

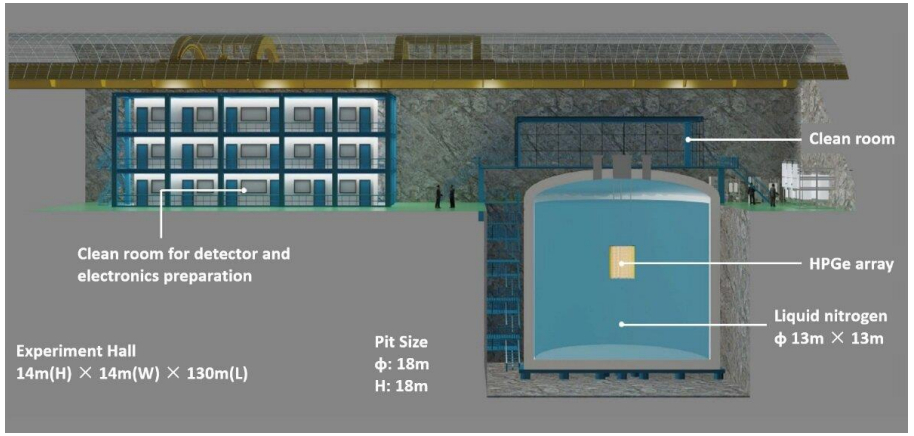
# OUTLINE

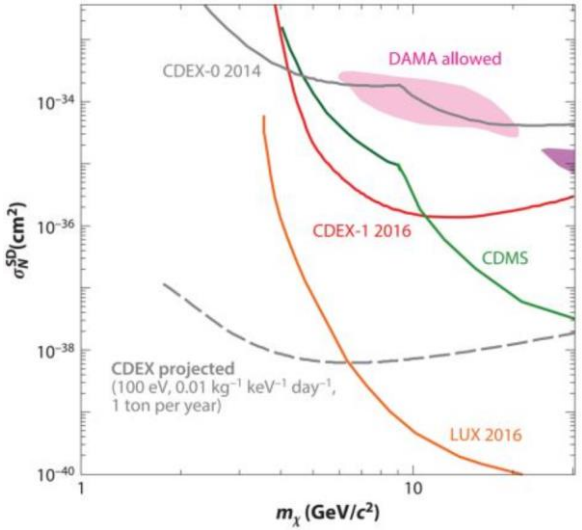
- Introduction
  - CDEX-100 Experiment
- Current Structure of DAQ System
  - Hardware and PCB layout
  - Readout and Clock Architecture
  - Signal Integrity and Clock Distribution Test
- Status and Plans

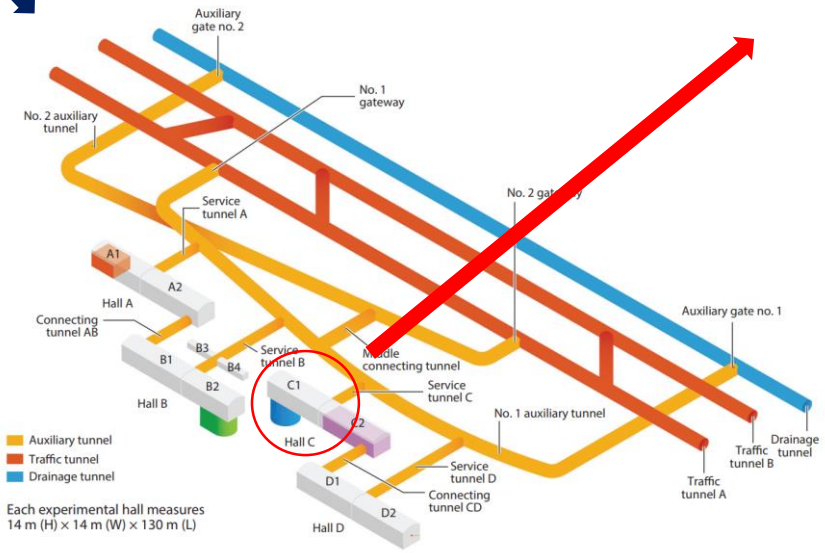
# CDEX-100 -- China Dark matter EXperiment

- **Direct detection of cold dark matter with 100-kg PCGe**
  - 100 PCGe (1 kg / detector)
  - Located in CJPL-II (2400 m underground)



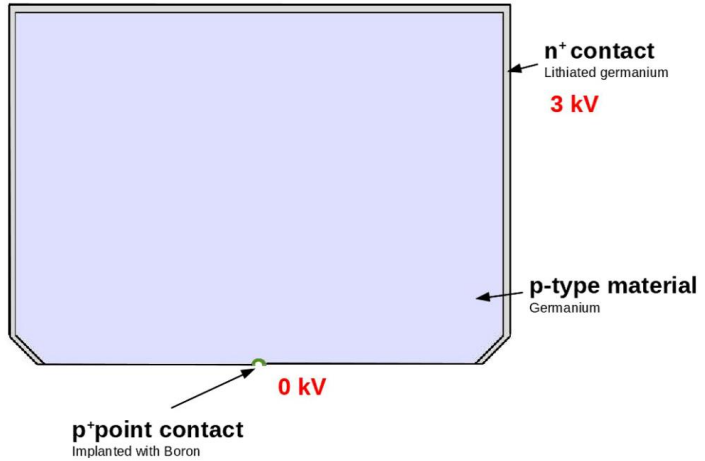



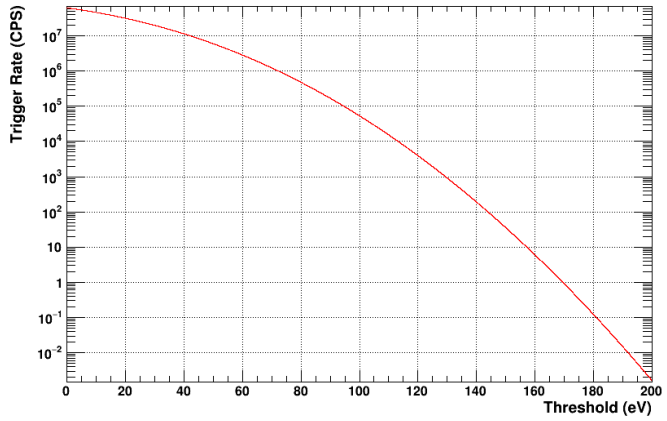

# CDEX-100 -- China Dark matter EXperiment

- **Readout Requirement for DAQ System**
  - **300 Sampling channels**
    - 100 PCGe (3 channels/detector)
  - **High sampling resolution**
    - Better energy resolution & PSD efficiency
    - Sample Rate 125 MSPS and 16 bits resolution
  - Support **ultra-low trigger threshold** (~120 eV)
    - ~3kHz @(120 eV threshold)
    - Long record time (~120 us each trigger)

    } ***High Bandwidth***

    - **Low-threshold rare case search still requires high transmission bandwidth**
  - Synchronization system



# OUTLINE

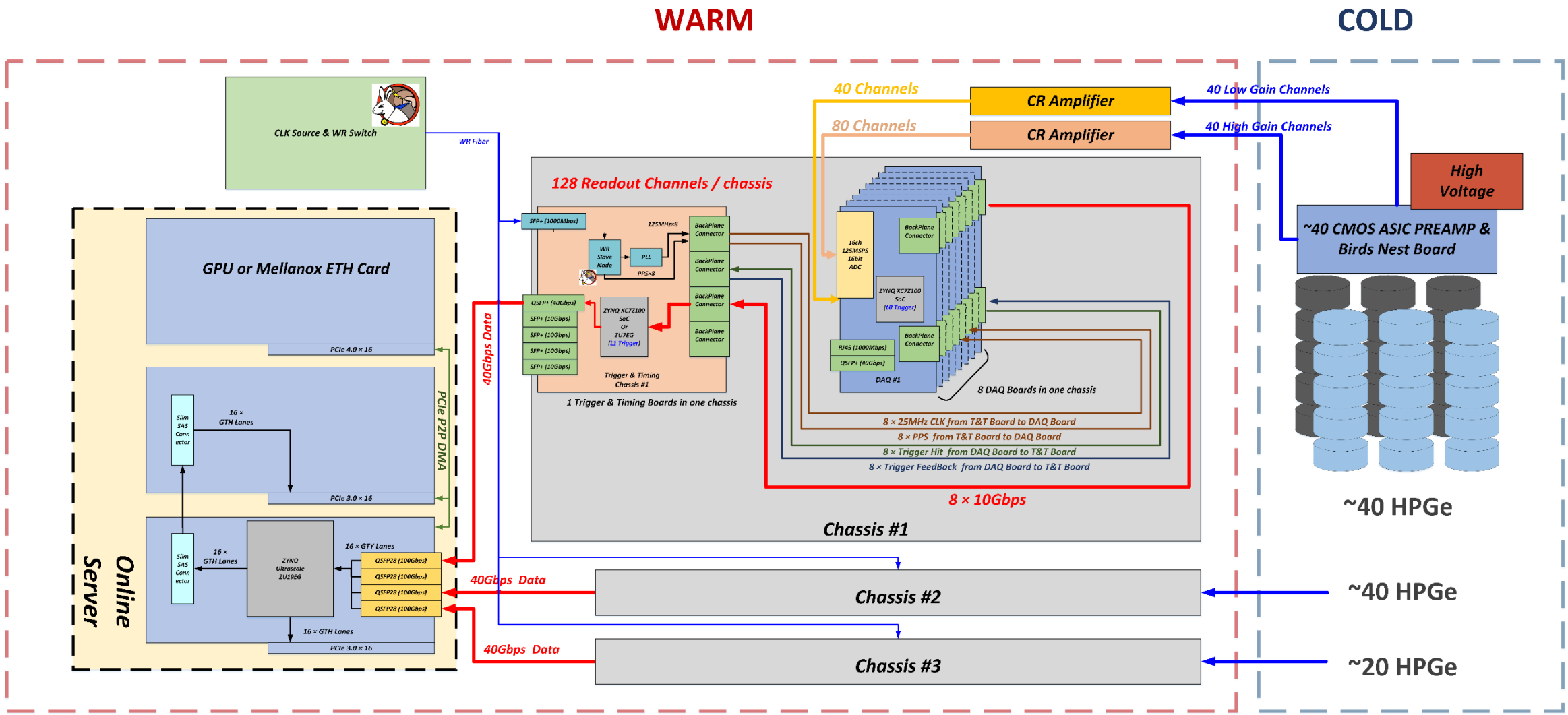
- Introduction
  - CDEX-100 Experiment

- **Current Structure of DAQ System**
  - **Hardware**
  - **Readout and Clock Architecture**
  - **Signal Integrity and Clock Distribution Test**

- Status and Plans

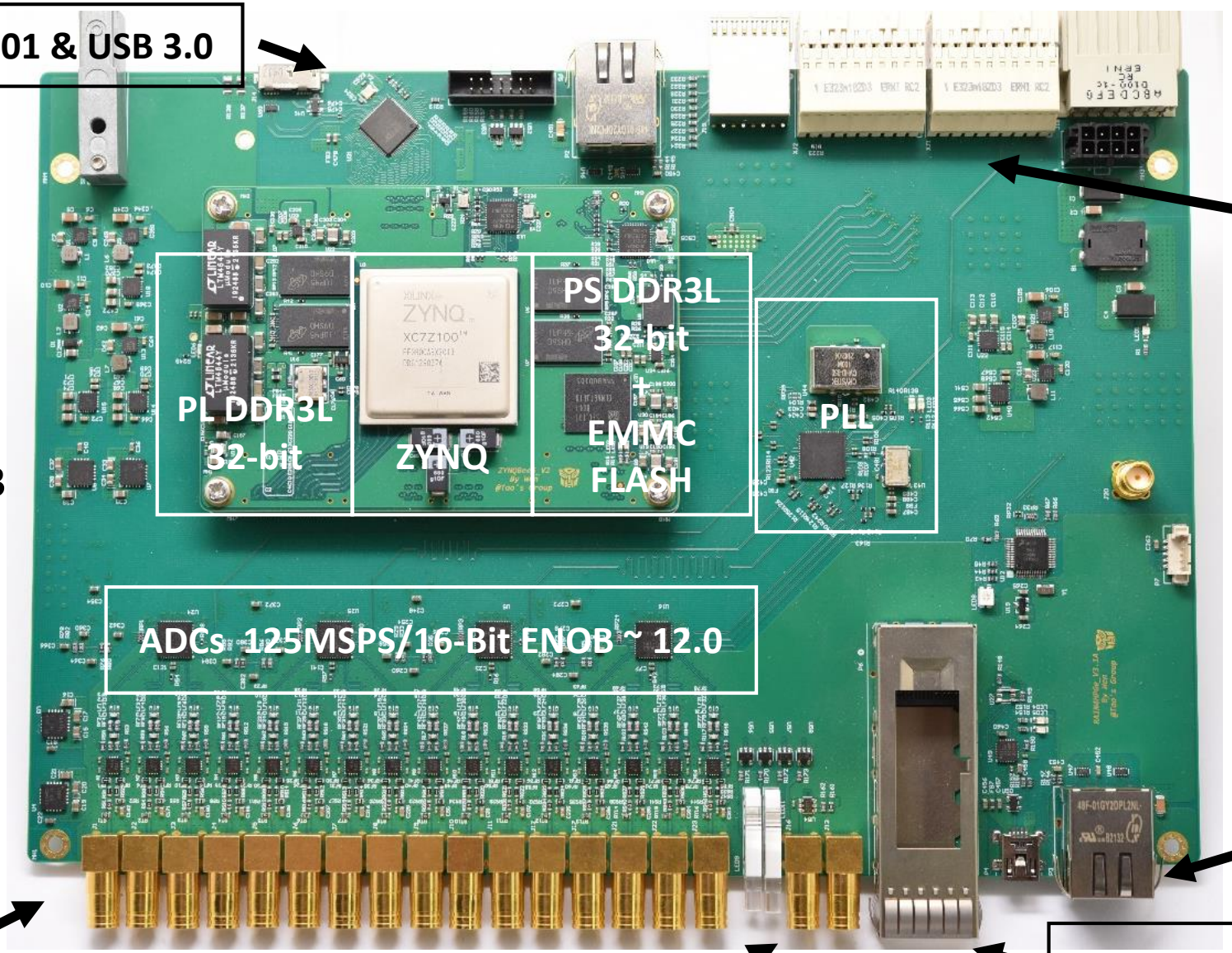
# Current DAQ System Block Schematic

- Data Transfer: Backplane + Fiber + PCIe
- Clock Sync: White Rabbit

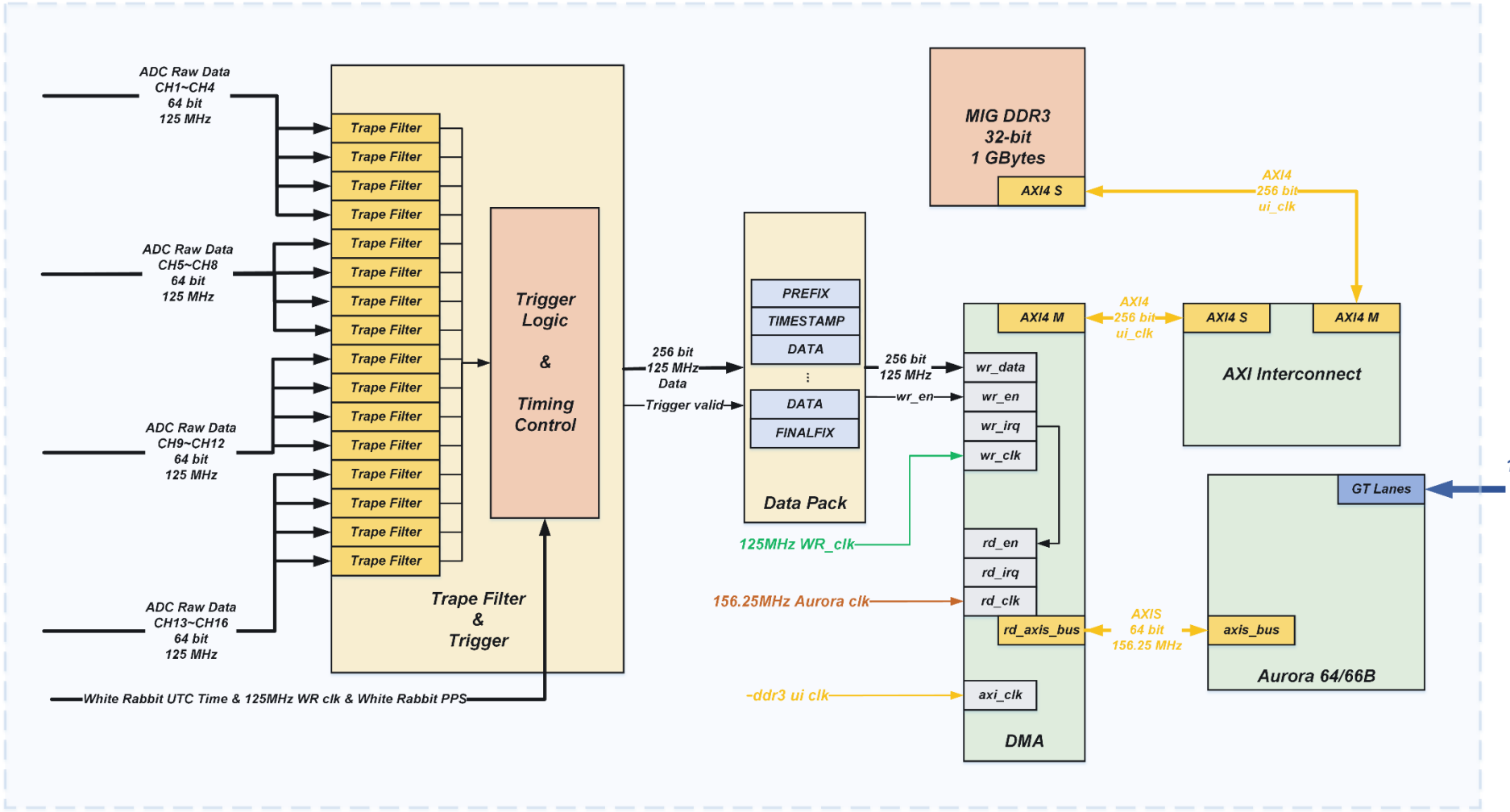


# Readout Unit : RAIN4HPGe Hardware

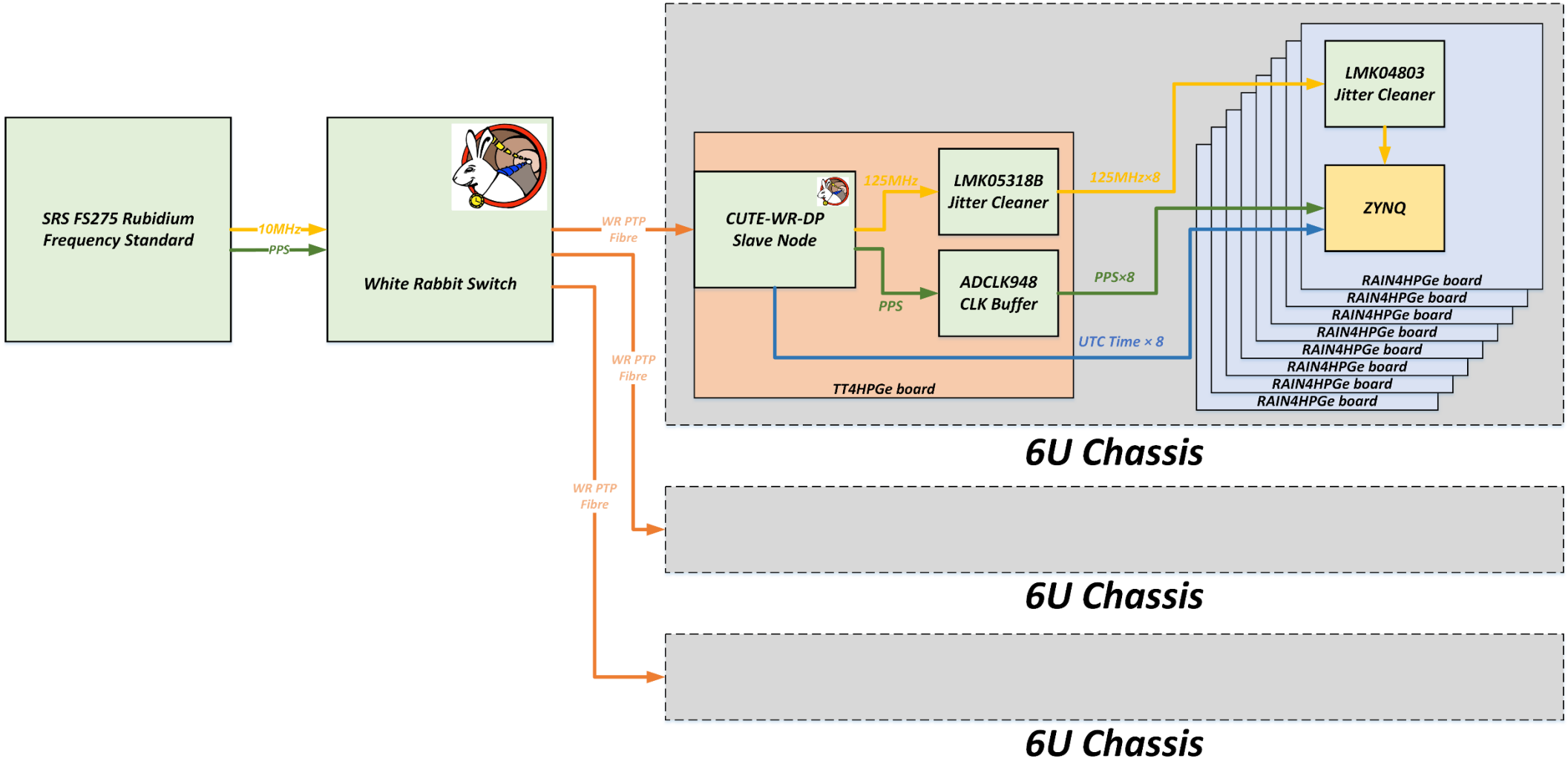
- Provide 16 sample channels 125M/16bit ENOB > 12.0 bits
- ZYNQ XC7Z100 SoC as readout unit
- 32-bit, 1GBytes DDR3 as deep buffer pool
- Backplane – 10Gbps
  - Using DS125BR 250 Redriver to guarantee SI
- QSFP – 40 Gbps



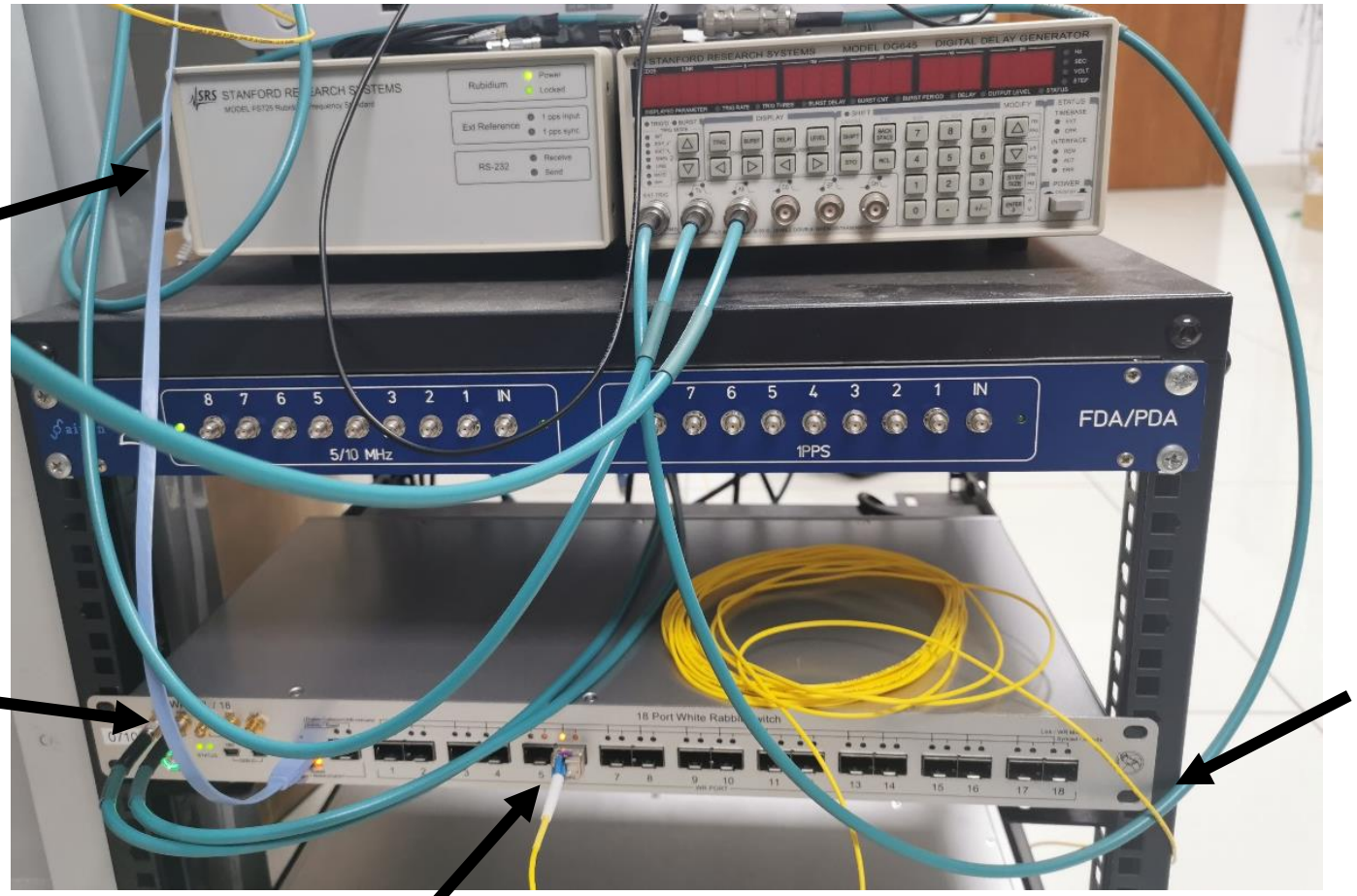
# Readout Unit : RAIN4HPGe block & Firmware



# Clock Distribution Tree



# WR Switch and Clock Source




**SRS FS725 Rubidium Frequency Standard**

**10MHz & PPS From Rubidium**

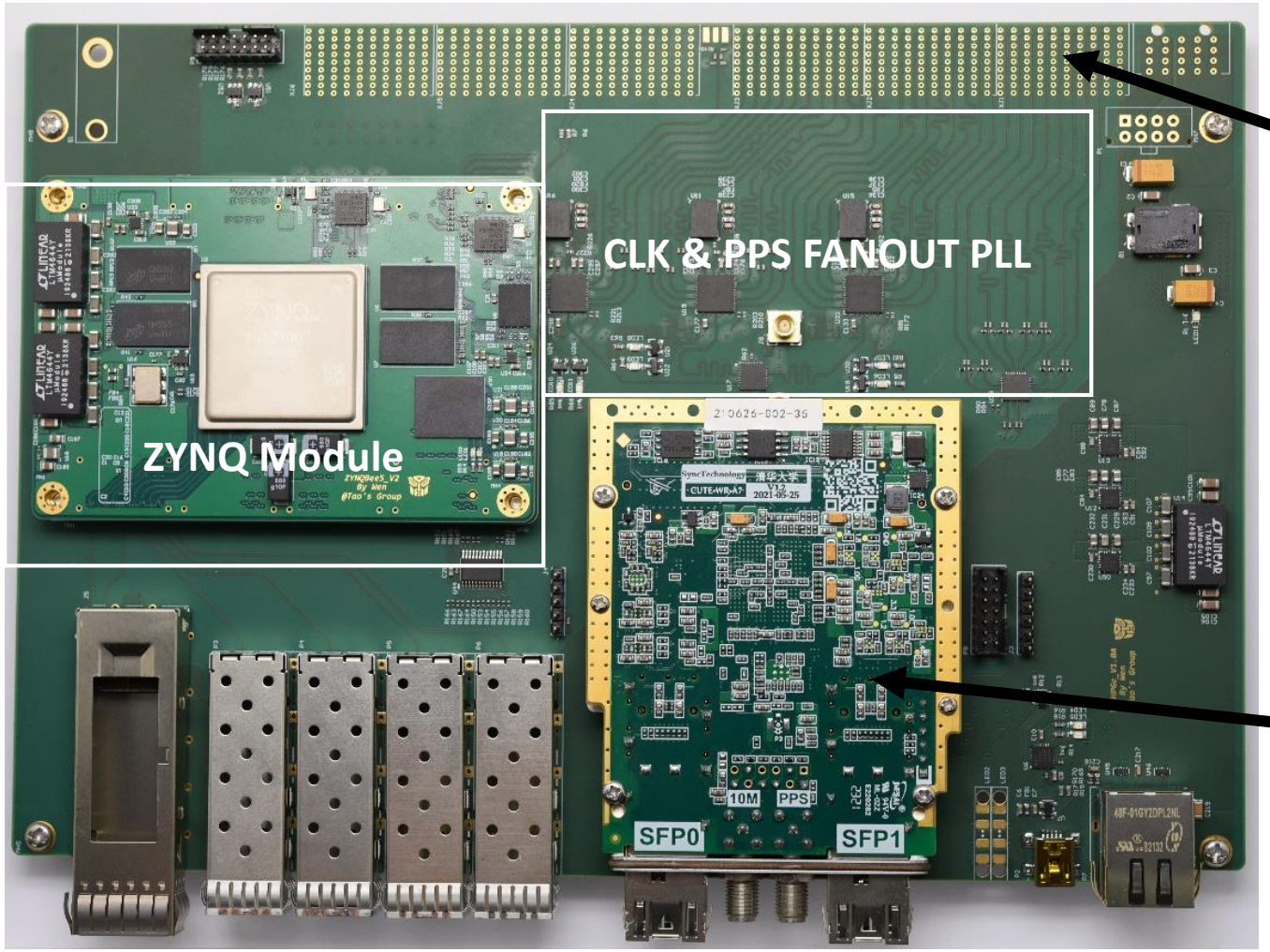
**WRS-18 White Rabbit Switch**

**Fiber to CUTE-WR-DP**

# Trigger & Timing Unit : TT4HPGe Hardware

*OR*

- Cute-WR-DP provide sync clock/PPS/UTC
- On board PLL & Jitter Cleaner fanout clock/ PPS to Readout Unit
- Receive the data from 8 Readout Unit
- L1 Trigger & Upload via QSFP+ & SFP+
- 32-bit, 1GBytes DDR3 /64-bit, 4Gbytes DDR4 as deep buffer pool




**CPCI Backplane**
- 8×10Gbps lanes from Readout Unit
- 8×125MHz White Rabbit clock
- 8×White Rabbit UTC time
- 8×White Rabbit PPS time
- PS UART/I2C

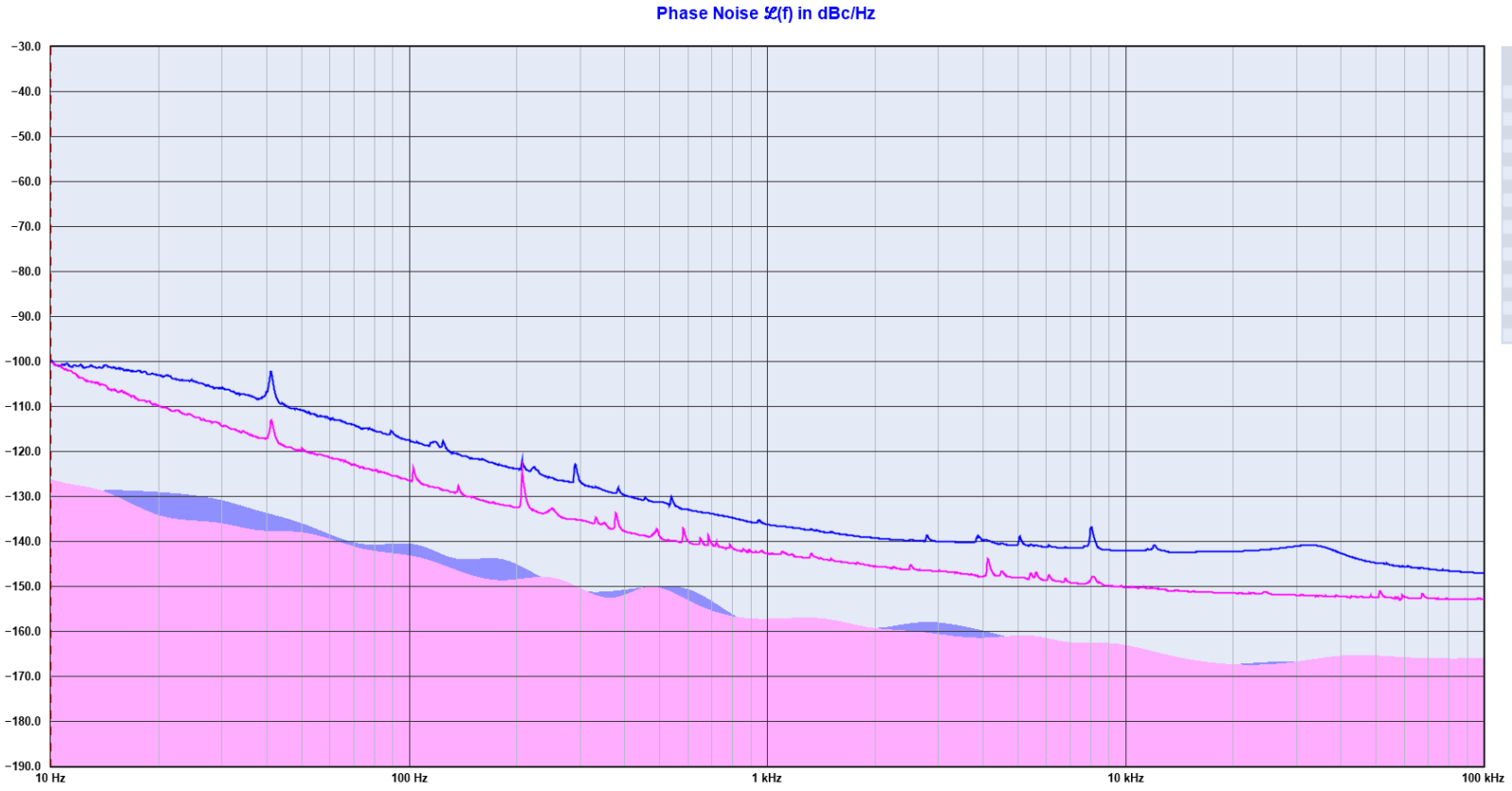
**Cute-WR-DP**
- White Rabbit Slave Node
- Provide 125MHz CLK/PPS/UTC

1× QSFP+ & 4×SFP+

Optical Fiber from WR switch

# Clock Distribution Test

- **Phase Noise**
  - **Blue Line : 10 MHz from CUTE-WR-DP**
  - **Red Line : 10 MHz fanout by LMK05318B PLL (clk source – CUTE-WR-DP)**

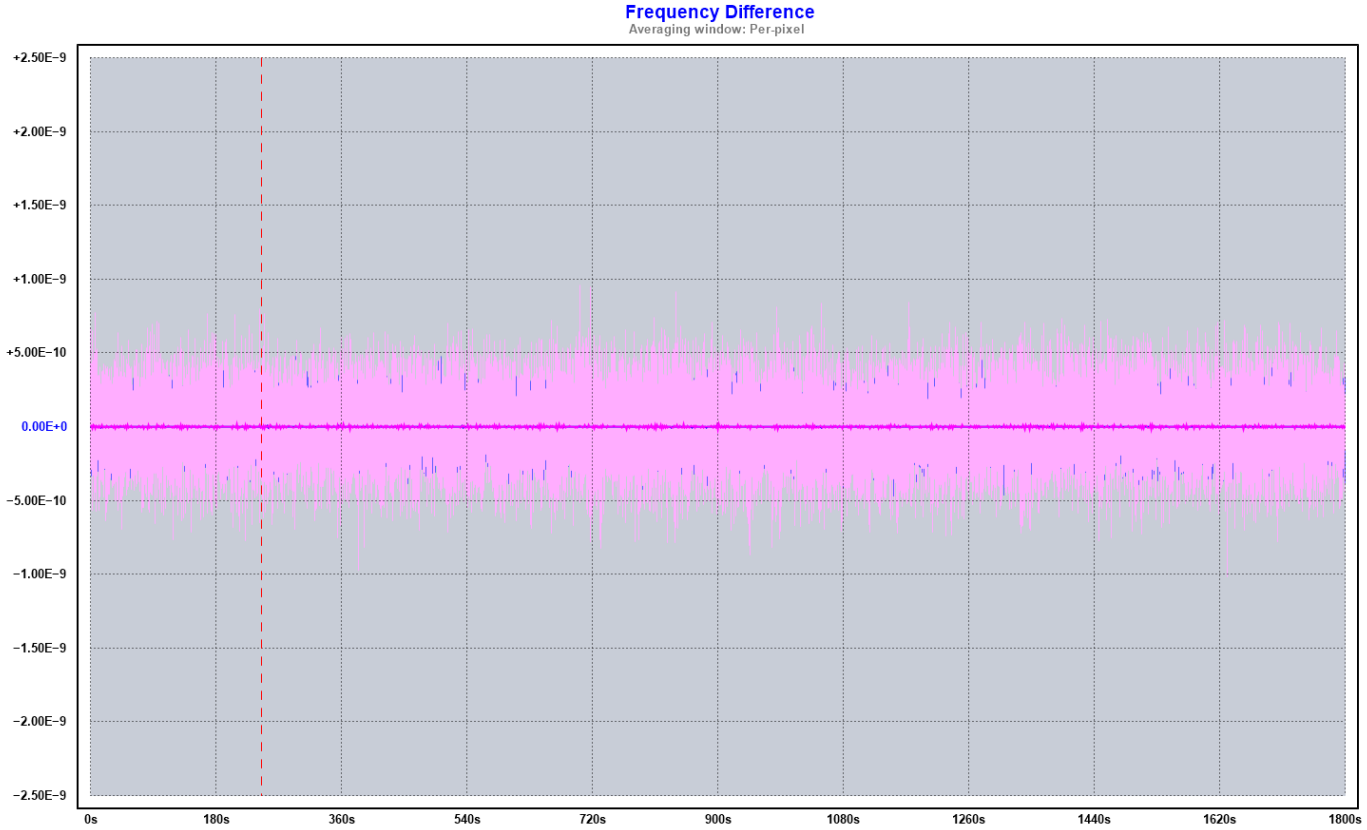



| PM Spur Offset (Hz) | dBc |
|---|---|
| 68.0 | -120.2 |
| 120.0 | -127.5 |
| 160.0 | -120.0 |
| 200.0 | -129.2 |
| 240.0 | -130.3 |
| 250.0 | -124.2 |
| 270.0 | -127.4 |
| 290.0 | -125.3 |
| 340.0 | -130.3 |
| 410.0 | -117.7 |
| 440.0 | -126.1 |
| 480.0 | -109.7 |
| 510.0 | -123.9 |
| 550.0 | -124.5 |
| 610.0 | -126.3 |
| 750.0 | -131.6 |
| 820.0 | -134.5 |
| 2780.0 | -134.1 |
| 5040.0 | -128.3 |

| Trace | Notes | Input Freq | Sample Interval | ENBW | dBc/Hz at 10 Hz | Duration | Acquired | Instrument |
|---|---|---|---|---|---|---|---|---|
| WR_SlaveNode_10MHz | | 10.000 MHz | 0.010 s | 50 Hz | -100.1 | 30m 0s | 180000 pts | Microsemi 3120A |
| LMK05318B_10MHz (Unsaved) | | 10.000 MHz | 0.010 s | 50 Hz | -100.1 | 30m 0s | 180000 pts | Microsemi 3120A |

# Clock Distribution Test

- **Frequency Difference**
  - **Blue Line : 10 MHz from CUTE-WR-DP**
  - **Red Line : 10 MHz fanout by LMK05318B PLL (clk source – CUTE-WR-DP)**

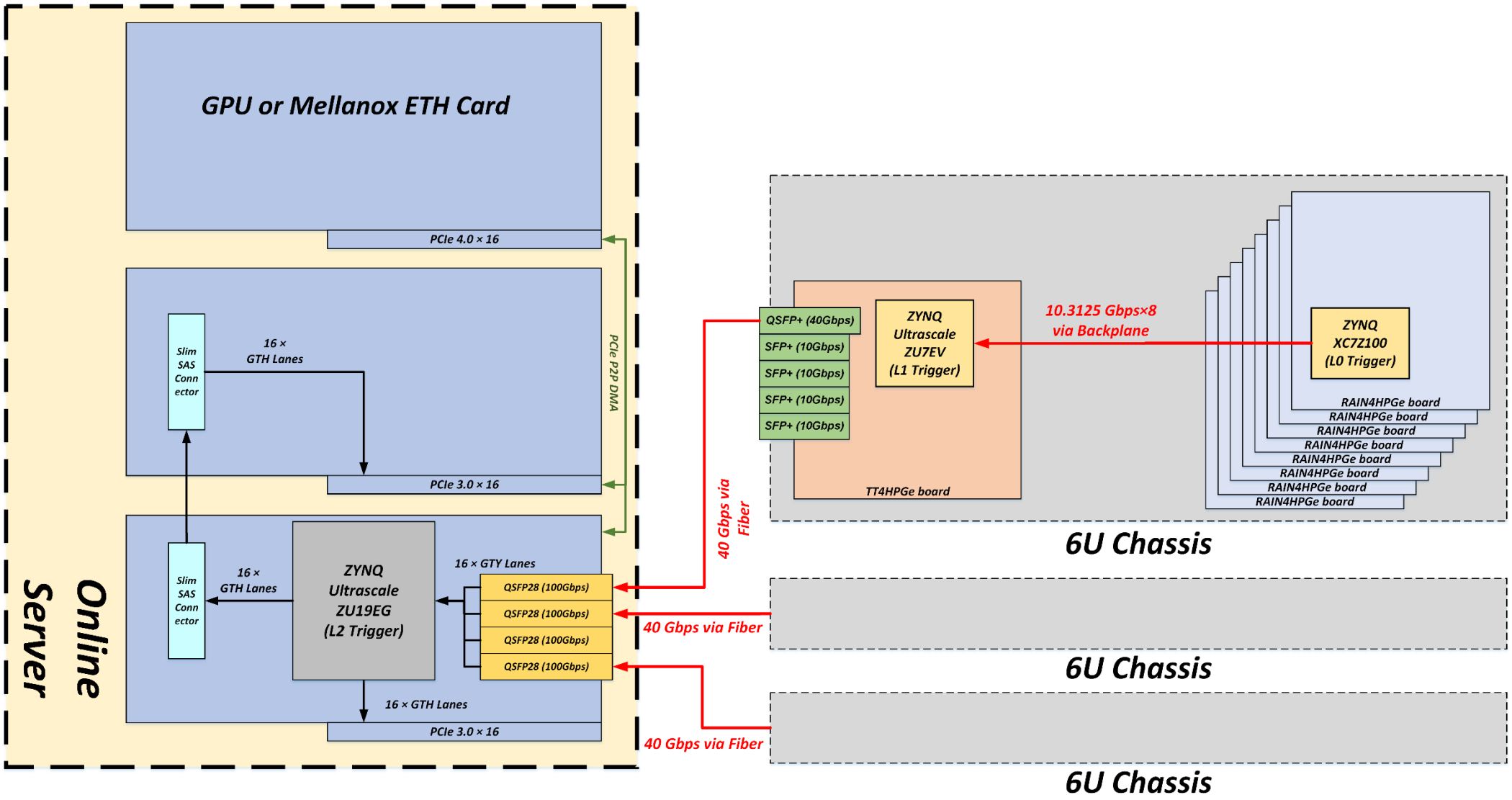



| Origin | Drift (Hz/sec) | Drift (Hz/min) |
|---|---|---|
| −5.08E−14 | +2.73E−10 | +1.64E−8 |
| −7.11E−14 | +4.92E−10 | +2.95E−8 |

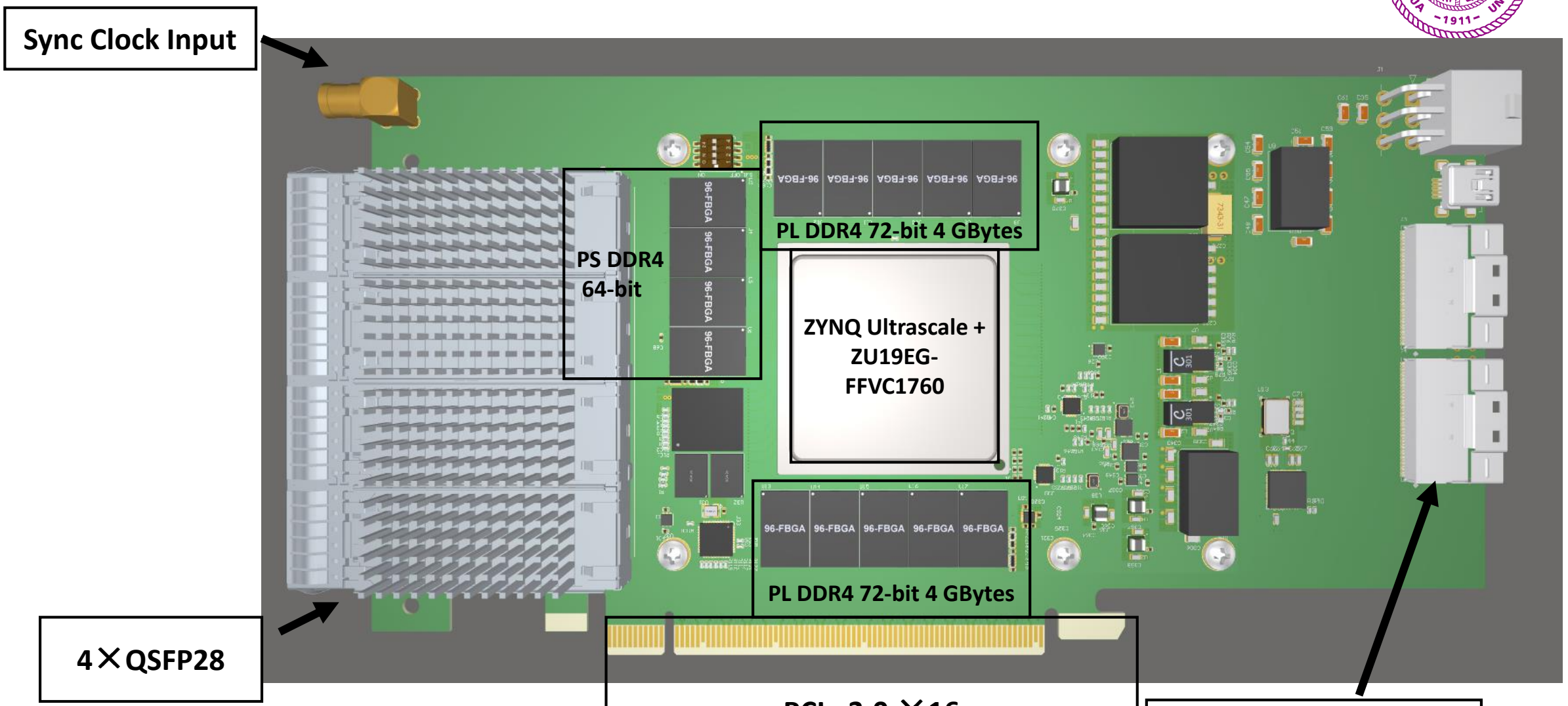
| Trace | Notes | Input Freq | Sample Interval | ENBW | Freq at 245s | Duration | Acquired | Instrument |
|---|---|---|---|---|---|---|---|---|
| WR_SlaveNode_10MHz (Unsaved) | | 10.000 MHz | 0.010 s | 50 Hz | 9 999 999.998 Hz | 30m 0s | 180000 pts | Microsemi 3120A |
| LMK05318B_10MHz (Unsaved) | | 10.000 MHz | 0.010 s | 50 Hz | 10 000 000 Hz | 30m 0s | 180000 pts | Microsemi 3120A |

- **Phase Difference between chassis is under test**

# Readout Data Collection Tree



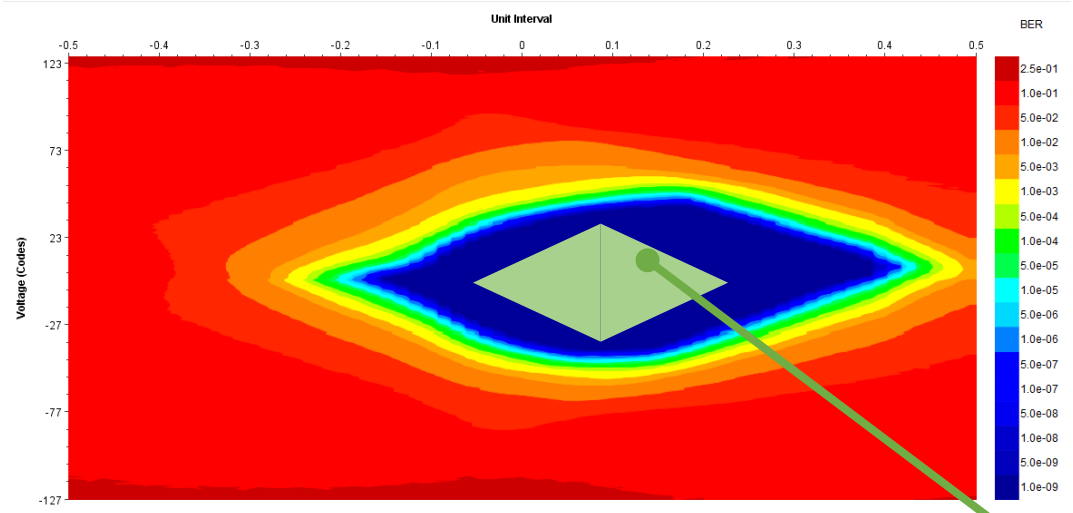
# PCIe Network Unit :



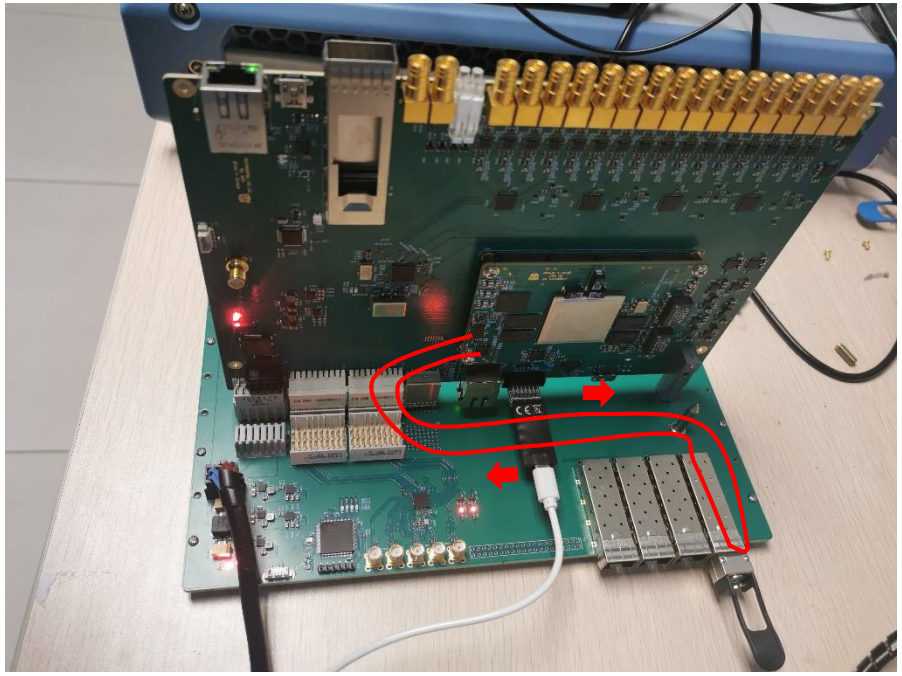

- **Still Under Design**

# Signal Integrity Test

- **SI Test was carried on a Test Backplane**
  - **Long trace loop (~17 inch), through Readout Unit/B2B Connector/Backplane Connector/Backplane**
  - **Lane Speed : 10.3125 Gbps**
  - **Coding Style : PRIBS-31**




| Name | TX | RX | Status | Bits | BER | Errors |
|---|---|---|---|---|---|---|
| Ungrouped Links (0) | | | | | | |
| Found Links (1) | | | | | | |
| Found 0 | MGT_X0Y10/TX | MGT_X0Y10/RX | 10.312 Gbps | 2.865E13 | 3.491E-14 | 0E0 |



*BER < 1E-13*

*SFF-8418 Minimum eye diagram at the receiver*


16

# OUTLINE

- Introduction
  - CDEX-100 Experiment

- Current Structure of DAQ System
  - Hardware and PCB layout
  - Readout and Clock Architecture
  - Signal Integrity and Clock Distribution Test

- **Status and Plans**

# Status and Plans

- **Hardware**
  - Readout Unit & Trigger/Timing Unit & Backplane is verified
  - PCIe Network Unit is in design
- **Firmware**
  - Firmware of the Readout Unit/Trigger/Timing Unit has alpha version released and is under testing
  - Firmware of the PCIe Network Unit is still under developing
- **Joint Test of the Readout Unit and Trigger/Timing Unit is running**
- **Lossless data compression algorithm is also under study**

# CDEX

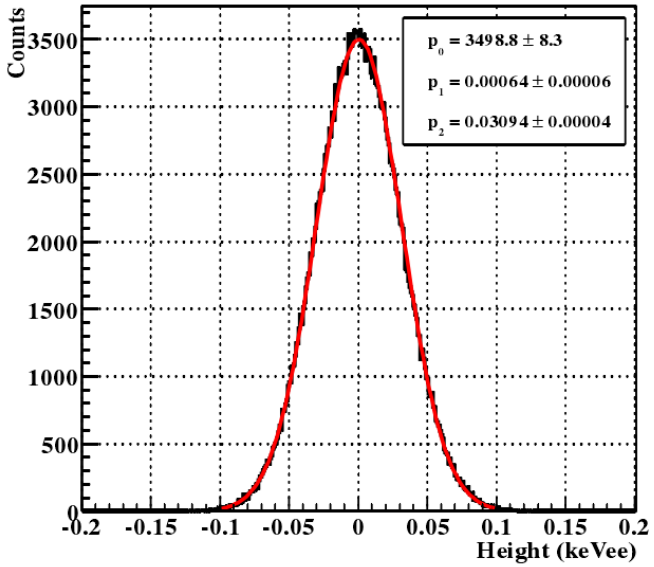

## Thank you for your attention!

# BACKUP

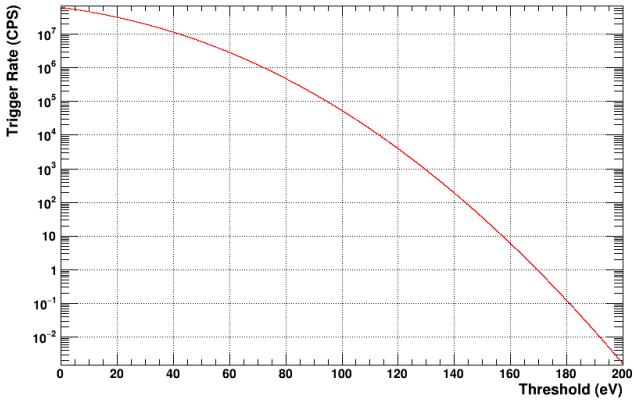
- **Trigger threshold v.s. Data transfer rate**
  - **CDEX-1B system noise**
    - μ = 0 eV, σ = 30 eV
  - **The number of points whose value exceeds $x_m$**

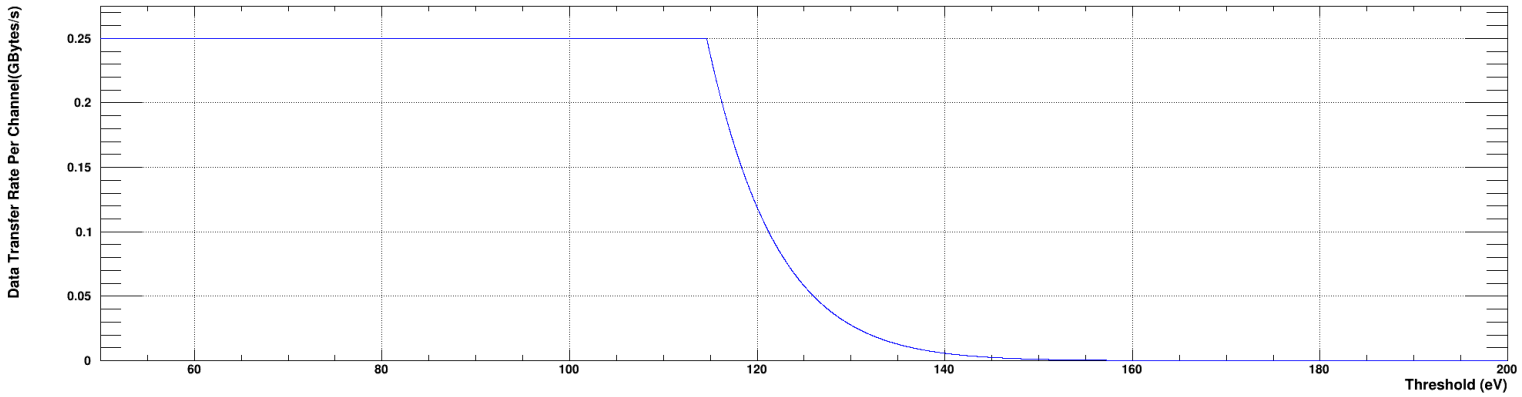
$$Counts = f_s \times \int_{x_m}^{+\infty} P(x)dx \quad \text{where} \quad P(x) = \frac{1}{\sqrt{2\pi}\sigma} \cdot e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2}$$

  - **Record 120 us (Once trigger)**



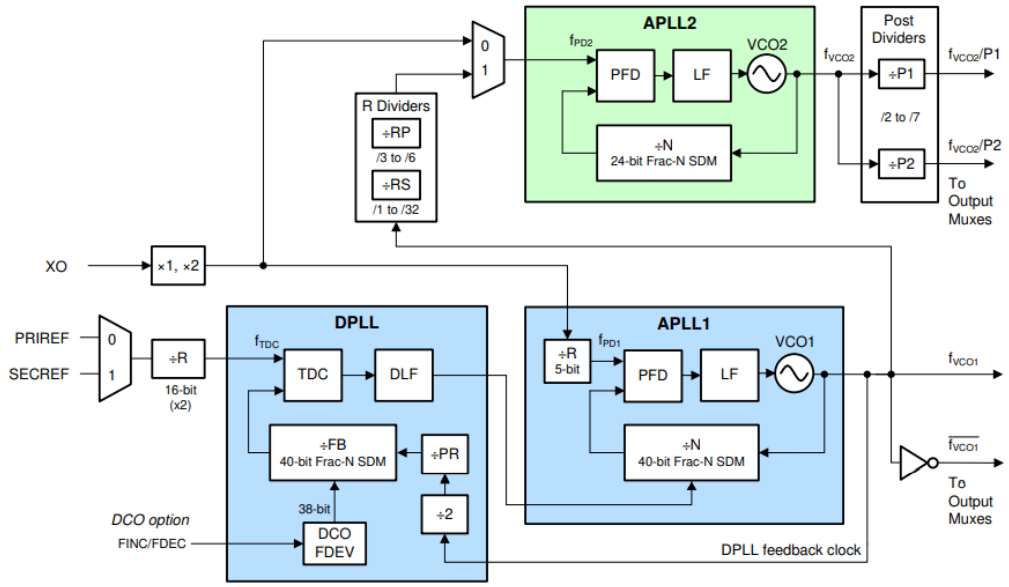

CDEX-1B System Noise
σ = 30eV

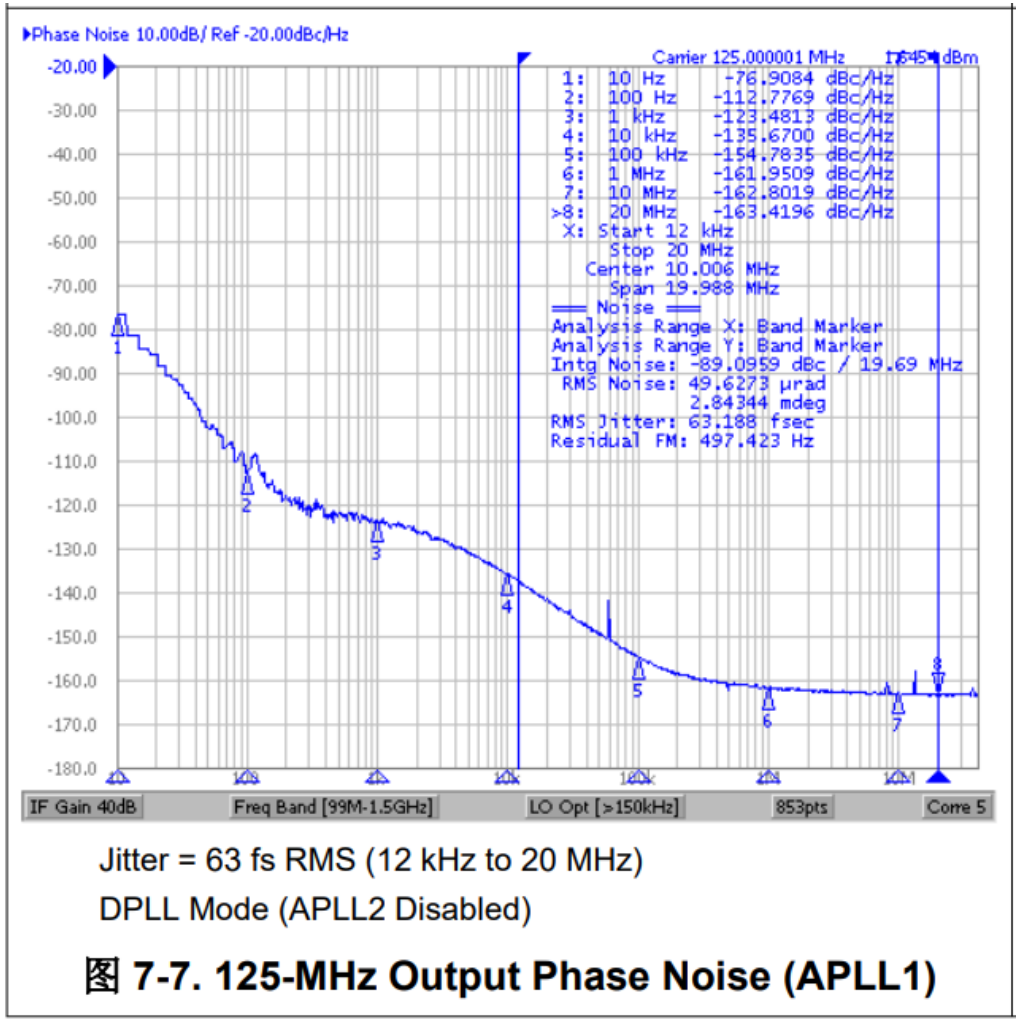


# BACKUP

- Clock phase noise v.s. Jitter cleaner
  - LMK05318B
    - Use DPLL to clean jitter
    - APLL use BAW VCO to achieve phase noise




Jitter = 63 fs RMS (12 kHz to 20 MHz)

DPLL Mode (APLL2 Disabled)

**图 7-7. 125-MHz Output Phase Noise (APLL1)**