Development of the Test-bench "Wukong" for Readout Electronics and Pulse Digitizer

23rd Virtual IEEE Real Time Conference Abstract ID #101

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Hardware Design of "Wukong" system

In this paper, two ADC mezzanine cards are developed based on 4 channels of 125MSPS, 16-bit AD9653 and 1 channel of 1GSPS 13-bit ADC13B1G, which are used for the acquisition of slow signal and fast signal respectively to extract the energy information and time information of incident particles. Table I shows the dynamic performance of ADC mezzanine cards and Fig. 1 shows the Wukong system with 4 ADC mezzanine cards and 1 DAC mezzanine card.

Table Ⅰ. ADC Dynamic Performance.

ADC name	Channel	Analog Input (Full-Scale)	ADC ENOB Measurement (@10MHz)
ADC13B1G	1	1.4 Vpp	10.45
AD9653	4	2 Vpp	12.25

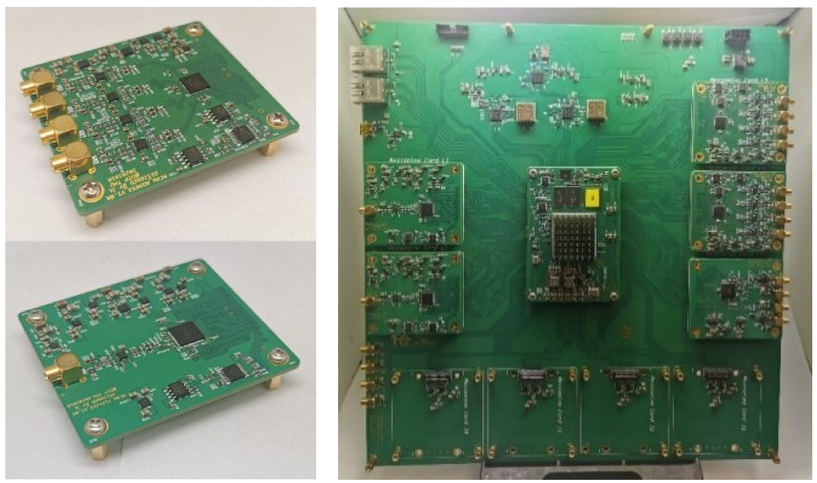


Fig. 1. Hardware design of Wukong system. The first photo is the ADC mezzanine cards, the second photo is the overall system.

Method

The total noise of ADCs could be expressed as the RMS (root mean square) of the quantization noise and equivalent input noise of ADCs, which can be expressed in Equation (1).

$$V_{n\_ADC} = \sqrt{V_{ir}^2 + V_q^2} \quad (1) \qquad V_q = \frac{Fullscale}{2^N}/\sqrt{12} \quad (2)$$

$$ENOB \approx \log 2\left(\frac{Fullscale}{V_{n\_ADC}\cdot\sqrt{12}}\right) \quad (3)$$

Without loss of generality, we could consider these noises uncorrelated and roughly estimate the ENOB of the system by Equation (3). It's necessary to note that this estimation method does not consider the effect of sampling clock jitter. In this paper, we calculated and simulated the total noise of the ADC driver based on the noise specification given in the datasheet and the actual bandwidth. The total ADC input noise theoretically calculated is $113.89\mu V$ RMS, and the total ADC input noise actual measured is $129.39\mu V$ RMS, which means that the maximum ENOB of the ADC is 12.13.

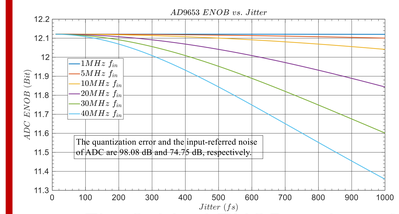
Table Ⅱ. Noise Contribution from Different Components in the ADC Signal Chain.

Section	Noise Contribution
AD5686R	53.32μV RMS (52.1μV RMS from internal reference)
AD8676+ADA4927	55.874μV RMS
AD9653	82.4μV RMS
Total	113.89μV RMS
AD9653 Channel A measured	129.39μV RMS

Experiment and Result

The total SNR of the ADC could be calculated by the following Equation, Section B states that the SNR_q is 98.08 dB while the SNR_t is 74.75 dB (ENOB = 12.13). Based on the above SNR_q and SNR_t, the effect of clock jitter on system ENOB could be calculated at different input sine wave frequencies, as shown in Fig. 2.

$$SNR_{ADC} = -10\lg(10^{-SNR_q/10} + 10^{-SNR_j/10} + 10^{-SNR_t/10})$$



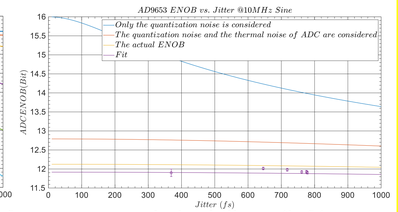
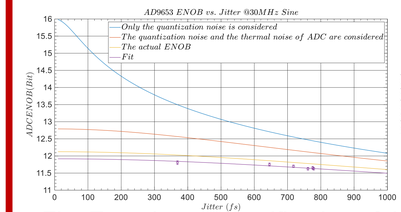


Fig. 2. Ideal ENOB vs. input frequency and clock jitter (left).
Fig. 3. Experimental verification of the relationship between clock jitter and ENOB at an input sine wave frequency of 10MHz (right).



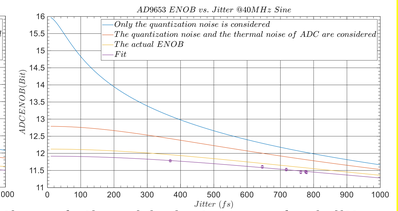


Fig. Experimental verification of the relationship between clock jitter and ENOB at an input sine wave frequency of 30MHz (left) and 40MHz (right).

The three figures above show the comparison between the theoretically calculated and actually measured ENOB under the input sine wave.

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