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Development of the Test-bench "Wukong" for Readout Electronics and Pulse Digitizer

On behalf of

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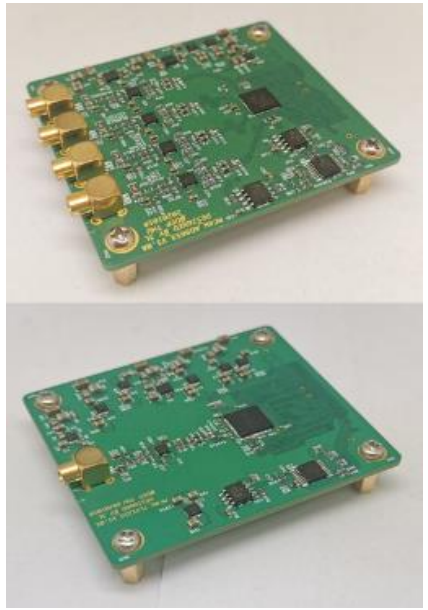
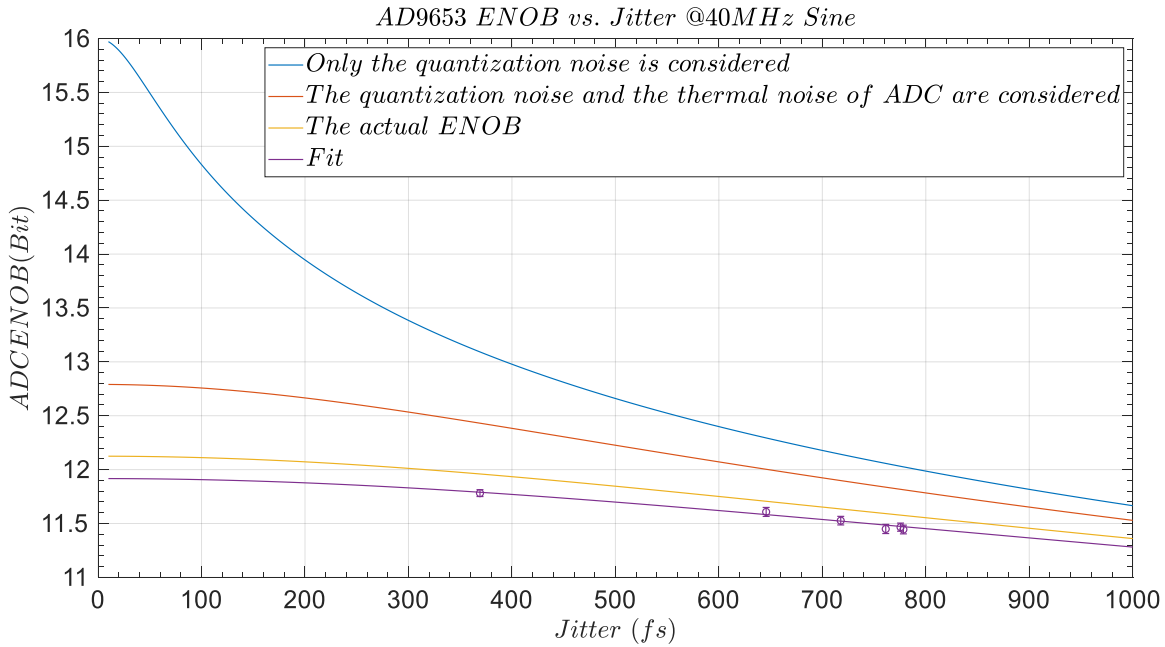




Analysis of the Reasons for the Deterioration of ADC ENOB

The SNR of ADC is mainly caused by 3 parts, ADC the quantization noise of ADC, the thermal noise of ADC and sampling clock jitter. The total SNR of ADC is,

$$SNR_{ADC} = -10\lg\left(10^{-SNR_{Quantization-Noise}/10} + 10^{-SNR_{jitter-Noise}/10} + 10^{-SNR_{Thermal-Noise}/10}\right)$$

The thermal noise contribution of the ADC and peripheral circuits is shown in the table below,

Section	Noise Contribution
AD5686R	**53.32μV RMS (52.1μV RMS from internal reference)**
AD8676+ADA4927	**55.874μV RMS**
AD9653	**82.4μV RMS**
Total	**113.89μV RMS**
AD9653 Channel A measured	**129.39μV RMS**

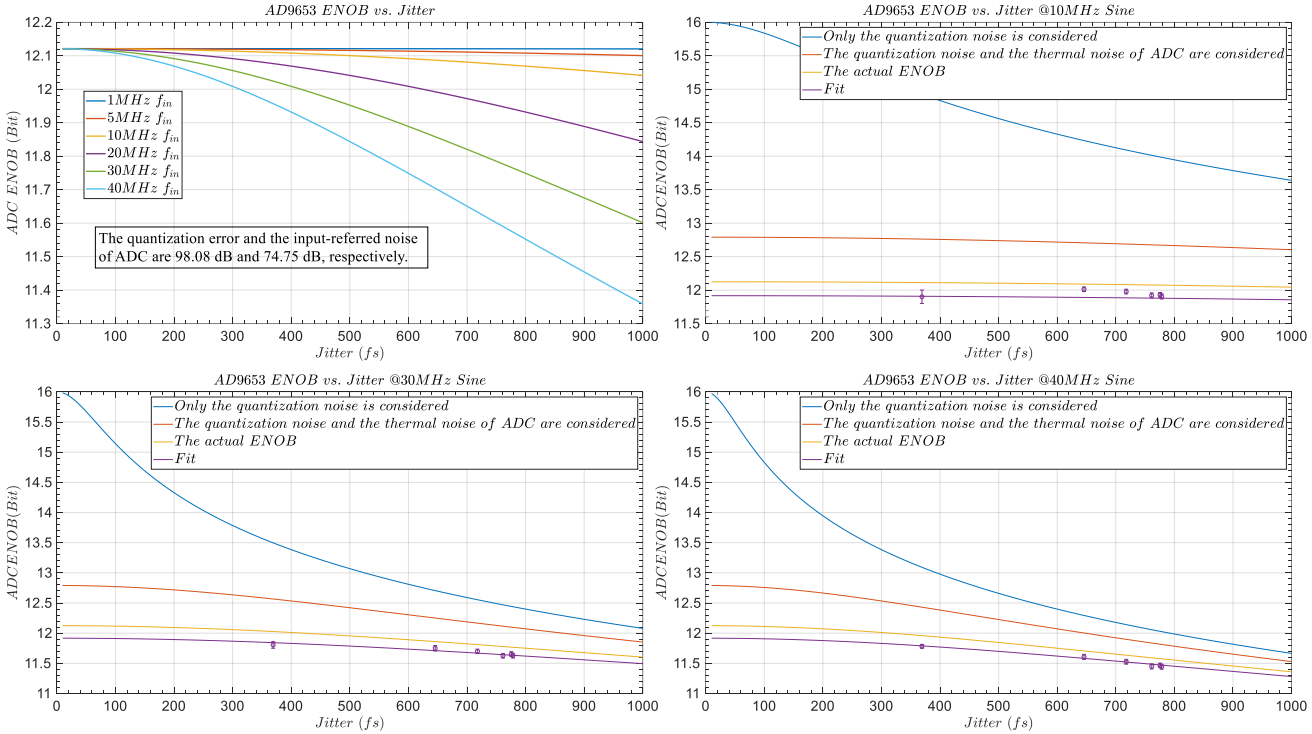
Without considering the clock jitter, the ENOB of the ADC can be estimated by the following 3 equations,

$$V_{n\_ADC} = \sqrt{V_{ir}^2 + V_q^2} \qquad V_q = \frac{Fullscale}{2^N}/\sqrt{12}$$

$$ENOB \approx \log 2\left(\frac{Fullscale}{V_{n\_ADC}\cdot\sqrt{12}}\right)$$

Consequently, the maximum ENOB of the AD9653 is 12.13

The SNR_q is 98.08 dB while the SNR_t is 74.75 dB (ENOB = 12.13). Based on the above SNR_q and SNR_t, the effect of clock jitter on system ENOB could be calculated at different input sine wave frequencies



The three figures above show the ENOB for theoretical calculations and measurements at a frequency of input sine wave 10MHz, 30MHz, and 40MHz, respectively. The measured results agree well with theoretical predictions.