Design of high-speed data transmission control system based on USB 3.0

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Abstract

In the nuclear detection system, the acquisition card will generate a large amount of event data, which needs to be uploaded to the PC for processing and analysis. Therefore, it is necessary to realize high-speed data communication between the acquisition card and the PC. As a widely used data interface protocol, USB3.0 has the advantages of fast transmission speed, high reliability and good versatility. Our system realizes the two-way communication between the host computer and FPGA through the USB3.0 interface. After actual testing, the system can achieve a maximum transmission speed of 374MB/s, which meets the needs of high-speed capture cards.

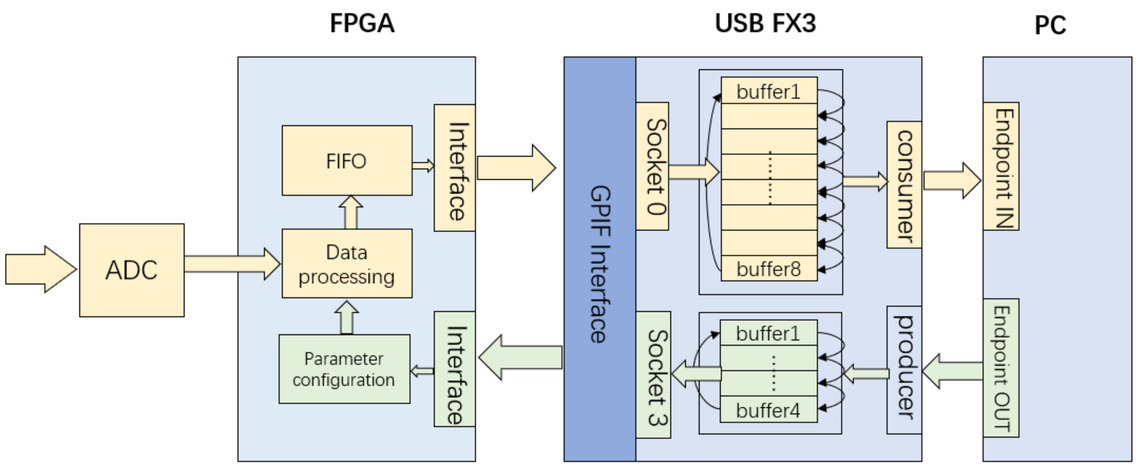
Introduction

In the nuclear detection system, the acquisition card will generate a large amount of event data, which needs to be uploaded to the PC for processing and analysis. Therefore, it is necessary to realize high-speed data communication between the acquisition card and the PC.

The overall structure of the system is shown in Fig. 1. The system includes ADC, FPGA, USB and PC. The ADC samples the detector signal, which is preprocessed by the FPGA and stored in the FIFO for buffering. Two modules are designed in the FPGA. One module is used to realize the data upload function, and another one is used to read the data from the PC to realize the control of the FPGA. Two transmission threads are implemented inside FX3 for bidirectional transmission between FPGA and PC.

This system uses a mature USB control chip,Cyusb3014.It is equipped with a FX3 processor, which is a powerful peripheral controller integrated with ARM9. It integrates a variety of general interfaces, including a high degree of freedom programmable interface GPIF II, which can meet the needs of various application scenarios. FX3 includes a SRAM, part of which can be configured as buffers for data buffering.

Figure 1. USB 3.0 Data transmission System



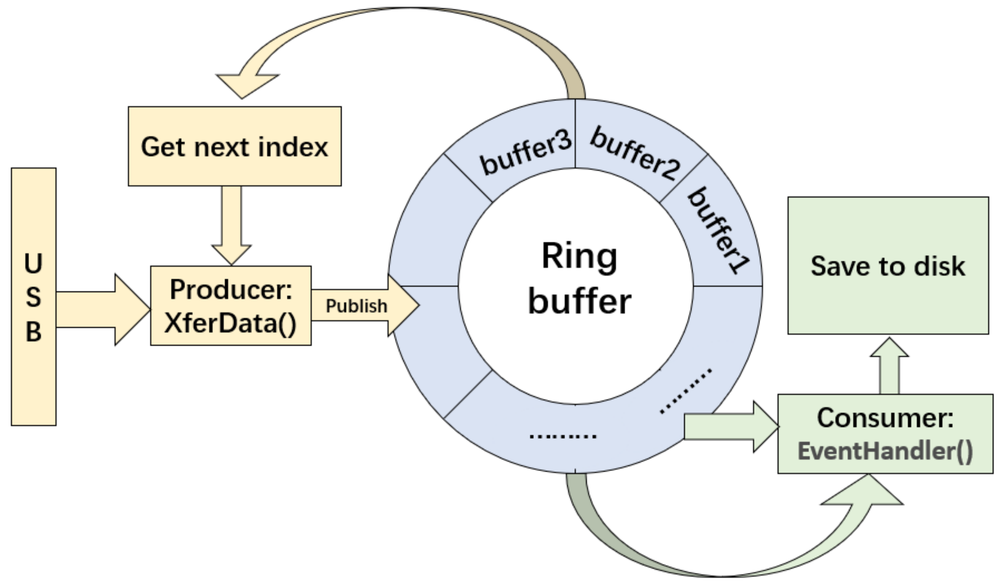
Critical Algorithm

There are the following key technologies to achieve high-speed upload of multi-channel data:

1. High-speed data transmission places strict requirements on the response delay of the host computer. Therefore, the design of the host computer is based on a high-performance disruptor architecture, which can realize a low-latency producer-consumer multi-threaded processing mode to avoid data backlog and lost.

2. The priority judgment of multiple channels uses the round-robin arbitration algorithm, which is a scheduling algorithm with variable priority. By this method, we can balance the data volume of multiple channels as much as possible.

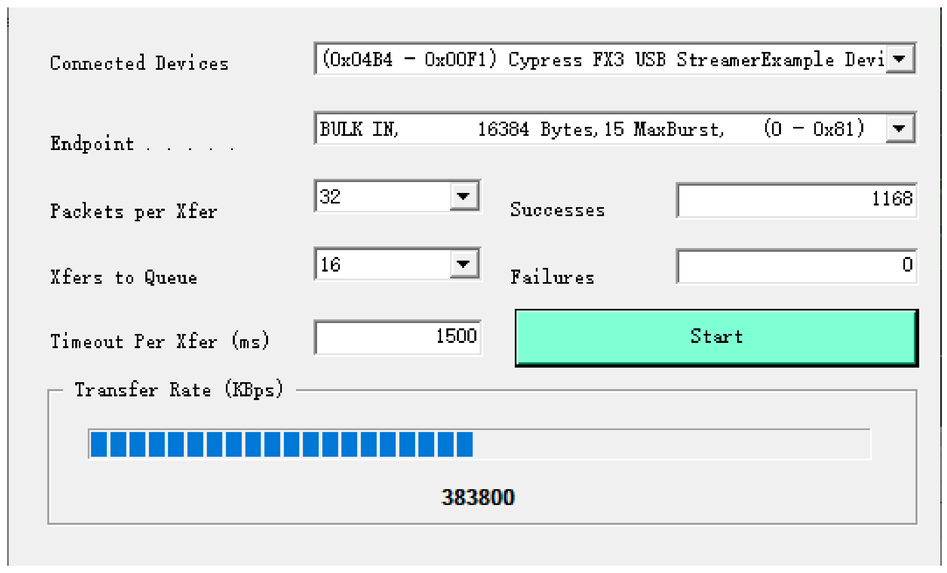
Figure 2. Diagram of disruptor architecture



Results

Pulse waveform data at equal intervals is generated in the FPGA to simulate the acquisition operation of the ADC. The host computer sends out the acquisition control command, then the data is transmitted to the host computer through USB and saved to the disk in real time. Use the speed test tool in the development kit to measure the speed, and the maximum transfer speed can reach 374MB/s. To verify transmission reliability, the collected data is analyzed through the software to check whether there are errors such as bit errors and packet loss. Through repeated measurements, it is verified that the USB transmission of the system has no bit errors. The system design meets the requirements.

Figure 3. Upload data speed test results



Discussions and Conclusions

This system realizes high-speed USB transmission channel by programming and self-defining FX3 in CYUSB3014. FPGA program is designed to contact with the USB interface and ensure smooth data transmission. The supporting software is designed to realize functions such as FPGA control and data reception. After actual measurement, the USB transmission speed is close to the theoretical maximum value in this mode. This system has a wide range of application in scenarios such as nuclide measurement.

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