The Fast Readout Unit for general control and data acquisition in heavy-ion experiments

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Abstract: To reduce the development time, production cost, and maintenance difficulties of the readout electronics, a Fast Readout Unit (FRU) has been designed for generic control and data acquisition in heavy-ion nuclear experiments at the Heavy Ion Research Facility in Lanzhou (HIRFL). FRU is an FPGA-based data acquisition advanced mezzanine card (AMC) module, suitable for micro telecommunications computing architecture (MicroTCA) and MicroTCA systems. The FRU can connect four front-end readout boards (FEBs) through optical links for data collection, packaging, and transmission. The system backplane bus uses the high-speed serial PCI Express (PCIe) bus, which is several times faster than the traditional parallel bus. This paper checks the performance test, and application test on the data transmission system. As a result, it is proved that the system can receive data via an optical link, transmit data via PCIe link, and accomplish data restoration. In addition, the AMC standard requires that the module management controller (MMC) be implemented onboard to monitor available and system of hardware needed management parameters. Thus, the system can meet the needs of heavy-ion nuclear experiments.

Introduction

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, interdisciplinary science, and relative applications.To reduce the development time, production cost, and maintenance difficulties of the readout electronics, a Fast Readout Unit (FRU), as shown in Figure 1, has been designed for generic control and data acquisition in heavy-ion nuclear experiments at HIRLF. To meet the transmission speed requirements of nuclear physics experiments, one of the candidate platforms is the MicroTCA, an industry standard that describes a small crate and backpanel.

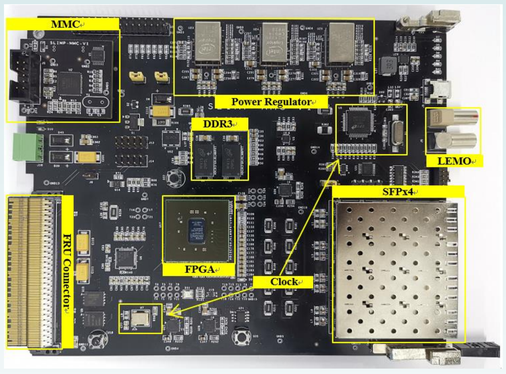

Figure 1. Picture of the FRU.

FRU Hardware distribution

The concept for FRU is a field-programmable gate array (FPGA)-based development platform designed to serve the general purpose of control and data acquisition (DAQ) system residing inside the MicroTCA crate, with high-speed bi-directional optical links allowing for a bandwidth of up to 6.6 Gbits/s. The FRU uses PCIe as the backplane bus and uses serial transmission to connect the boards in the MicroTCA crate. Intelligent Platform Management Interface (IPMI) control of FRU is foreseen. One MicroTCA crate shelf containing 12 FRU is sufficient to process the data from the 48 front-end electronics. The FRU printed circuit board (PCB) has been designed as residing in the MicroTCA crate, and the FRU is the half-height, double-width AMC, which occupies a mechanical volume of 150 mm × 187.3 mm × 13.88 mm. The FRU is designed in MicroTCA standard but still could work in stand-alone mode with an external power supply. Figure 2 shows the overview of the FRU design. The FRU is divided into six parts: FPGA control system, memory, data transmission, clock distribution, control and monitoring, power regulation.

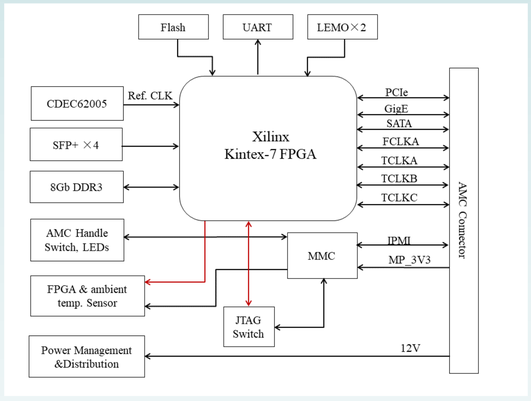

Figure 2. The FRU AMC module functional diagram.

FRU Firmware function

Using FPGA and peripheral circuits to complete the data transmission system, this transmission system comprises four core units, namely the SERDES unit, CDC unit, XDMA unit, and clock unit. This transmission system can realize the optical fiber receiving data after the CDC unit processes the data sent out through the PCIe. At the same time, to ensure the transmission system's continuous and stable operation, an intelligent management system is completed on the MMC. This system can complete the monitoring and management of the FRU board. Figure 3 shows the functional block diagram of the FRU system.

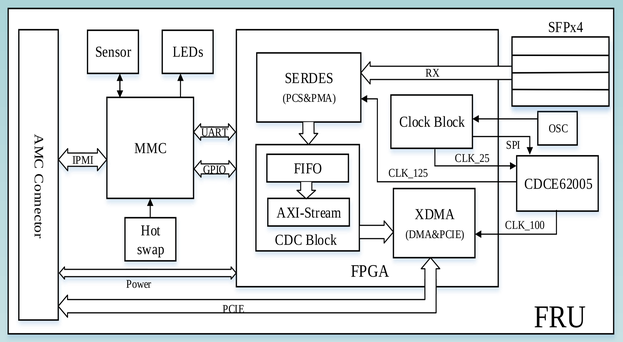

Figure 3. Functional block diagram of the FRU.

System construction and test

In the optical link interfaces test, data loop paths are created by connecting two adjunct optical link interfaces via the SFP+ modules. No error was observed in the 40 hours test, which indicated a bit error rate lower than 8.0×10^{-15}. In the data transmission rate test, the average transmission speed from the root complex device to the endpoint device is 393.1 MB/s. The extreme value of the write speed is about 430 MB/s, which is close to the theoretical value of the PCIe link. An example is using FRU for the readout of a CSI detector at HIRFL-CSR. We designed a small detector using a CSI crystal coupled APD. According to the test requirement, front-end readout electronics have been developed for CSI detectors. We conducted the test using a ^{60}Co source. The energy spectra obtained are shown in Figure 4.

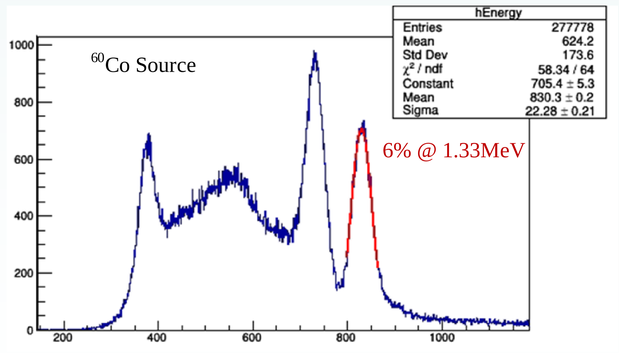

Figure 4. The energy spectra obtained by the constructed CSI detector and FRU with a ^{60}Co source.