HiGBt, a 5Gbps SerDes for heavy-ion physics experiments

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Introduction

The Heavy Ion Research Facility at Lanzhou (HIRFL) and the High-Intensity heavy-ion Accelerator Facility (HIAF) are the leading heavy-ion physics centers. Heavy-ion physics experiments at HIRFL and HIAF with significantly increased scale have put forward urgent requirements on high-speed and high-density data transmission links. In addition, the strong radiation environment is a significant challenge for commercial ASIC. Hence, the HiGBt, a general-purpose 5Gbps SerDes ASIC is specifically designed in 130 nm CMOS process for the on-detector and off-detector data transmission in these heavy-ion physics. Figure 1 shows the architecture of this proposed HiGBt.

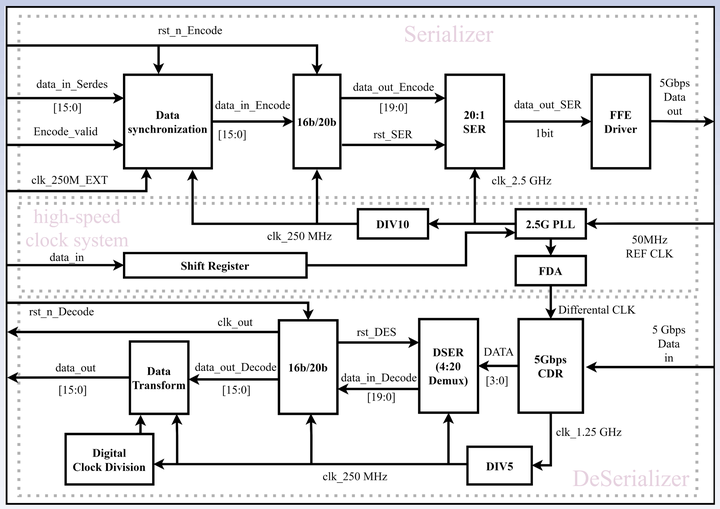

Figure 1 Architecture of the HiGBt

Main building blocks

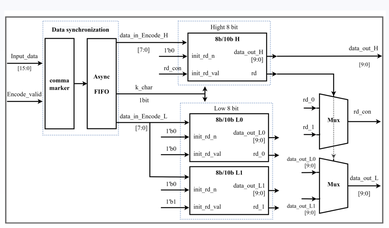

Figure 2 Schematic of the 16b/20b Encoder

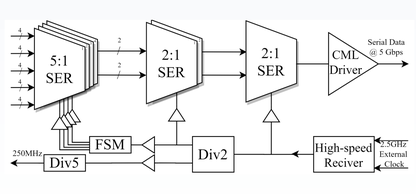

Figure 3 Schematic of the Serializer

The Serializer path consists of 16-bit input and 16-bit output asynchronous FIFO, a 16b / 20b Encoder, a 20:1 parallel-serial converter and an FFE driver. Figures 2 and Figures 3 shows the Encoder structure and the Serializer structure, respectively.

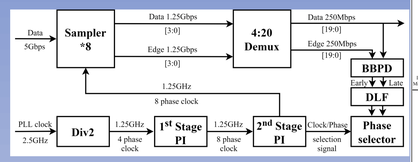

Figure 5 Schematic of the DeSerializer

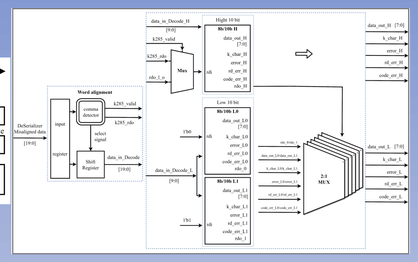

Figure 6 Schematic of the 16b/20b Decoder

The DeSerializer path consists of a clock data recovery device , a DeSerializer (Figures 2) and a 16b/20b Decoder (Figures 3).

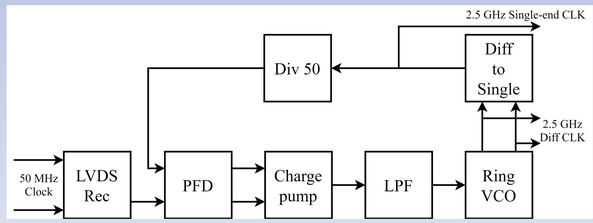

Figure 7 Schematic of the PLL

Figures 7 shows the PLL structure. The maximum output clock frequency of the PLL is 2.5 GHz.

The post simulation performance

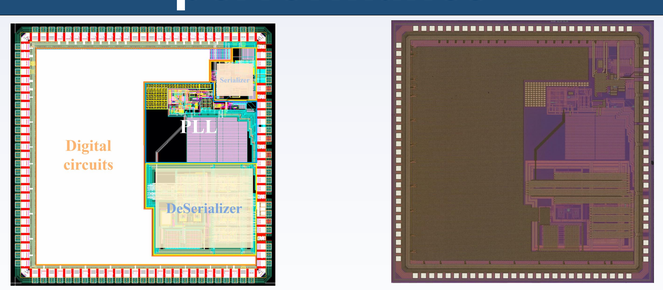

Figure 8 Layout of the HiGBt (left) and Physical map of tape-out HiGBt (right)

The layout of the HiGBt is shown on the left side of Figure 8, with an area of 310×310 μm^2. At present, this ASIC has been taped out, and its physical map is shown on the right side of Figure 8.

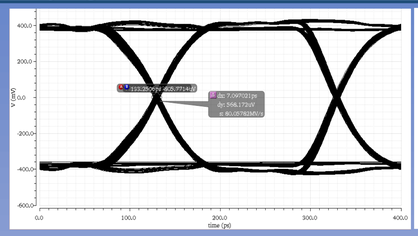

Figure 9 Eye diagram of the transmitter without pre-emphasis at typical case

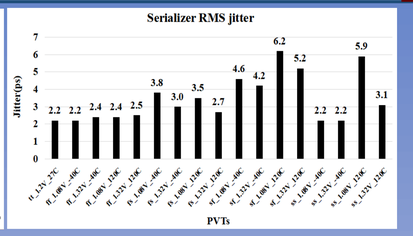

Figure 10 RMS jitter in different PVT variations

Figure 9 shows an eye diagram of the serial link transmitter without pre-emphasis enabled in the FFE driver. We calculated the RMS jitter of the eye diagram in different PVT variations and the results is shown in Figure 10. And the jitter with typical PVT variations is 2.2 ps, corresponding to a bit error rate of 1×10^{-14}.

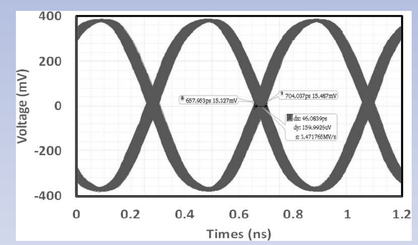

Figure 11 The eye diagram of the recovered clock

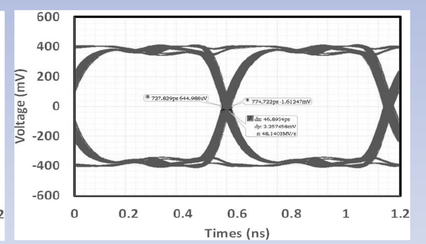

Figure 12 The eye diagram of the recovered data

For the DeSerializer path, the eye diagram of the recovered clock and data at 1.25 Gbps is shown in Figure 11 and Figure 12. The peak-peak jitters of the clock and data are 46.1 ps and 46.9 ps, respectively.

Conclusion

The HiGBT, which is 5Gbps SerDes, is designed in a 130 nm CMOS process for heavy-ion physics experiments at HIRFL and HIAF. The Serializer includes three stages to realize high-speed serialization. The DeSerializer is implemented in a high-linearity phase interpolator-based structure to avoid coupling two VCOs in adjacent channels. The 16b/20b Encoder (Decoder) employs an upper 8b/10b encoder (decoder) and two lower 8b/10b encoders (decoders) to improve the speed. Finally, the PLL adopts a ring VCO-based structure to reduce the power consumption. The power consumption is 123.4mW under 3.3V analog and 1.2V digital voltage.

References

1. A.X. Widmer and P.A. Franaszek, A DC-balanced, partitioned-block, 8B/10B transmission code, IBM J. Res. Dev. 27 (1983) 440.
2. M. Han, Researches on the key technologies of the high-speed SERDES interface chip design, Ph.D. Dissertation, University of Electronic Science and Technology of China (2012).
3. M. Verbeke, et al.: “A 1.8-pJ/b, 12.5-25-Gb/s wide range alldigital clock and data recovery circuit,” IEEE J. Solid-State Circuits 53 (2018) 470.
4. J. -H.Yoon, K.Kwon and H. -M. Bae: “3.125-to-28.125 Gb/s 4.72 mW/Gb/s Multi- Standard Parallel Transceiver Supporting Channel-Independent Operation in 40-nm CMOS,” IEEE Transactions on Circuits and Systems I: Regular Papers 67 (2020) 2647.