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Trigger and Timing Interface for the Read-Out Upgrade of the Belle II DAQ

To improve data throughput of the Belle II data acquisition we are upgrading the CPU-based COPPER system with a PCIe40 board carrying Arria 10 FPGA. Since one of the main functionality of the new system is event building in FPGA, the read-out system must be synchronized with the front-end electronics. This task is performed by the bidirectional trigger timing distribution system. During system commissioning we prepared several versions of the interface to this system. In the initial version of the interface we ported the code from Xilinx FPGAs to Arria 10. This revision also introduces monitoring of the status for multiple channels and a ring buffer to distribute trigger information to all channels in parallel. To improve stability under external noise, we implemented a clock-data recovery using an independent on-board oscillator as a reference clock in the next revision of the interface. We are also developing a version utilizing high-speed serial transceiver to replace CAT-7 RJ45 cables with optical fibers. The system commissioning has started in 2021 with few detectors and will be complete after the long shutdown 1 of SuperKEKB in 2023. In this paper, we will present the architectures of the interface to the trigger timing system implemented in the PCIe40 board and the system performance in the experiment.

Minioral

Yes

IEEE Member

No

Are you a student?

No

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