

Data Flow in the Mu3e DAQ

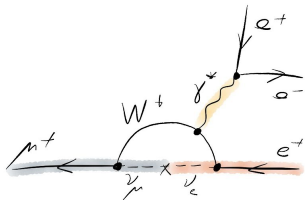
Marius Köppel on behalf of the Mu3e collaboration



Institute for Nuclear Physics, JGU Mainz

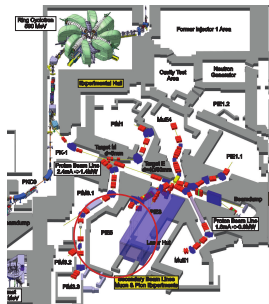
04.08.2022

Mu3e Motivation



SM with ν oscillation Br: $< 10^{-54}$

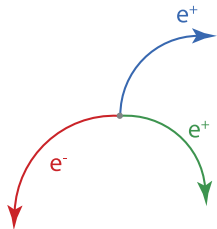
- Search for Lepton Flavor Violation
 $\mu^+ \rightarrow e^+ e^- e^+$
- Current limit (Br $< 10^{-12}$) set by
SINDRUM (1988)



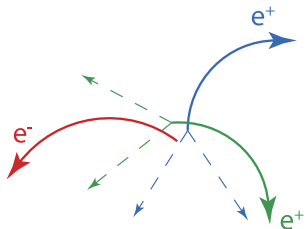
PSI Beam Line

- Muon beam of $10^8 \mu/s$
- One year of data taking
- Sensitivity up to one in 10^{15}

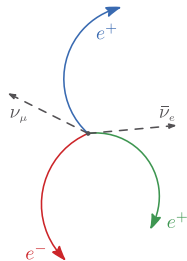
Mu3e Experiment



signal



random combinations of μ decays

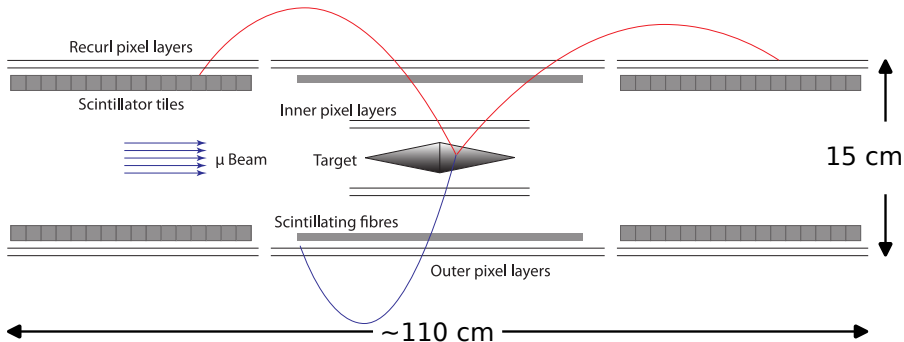


internal conversion

- $\sum p_e = 0$ and $\sum E_e = m_\mu$
- μ^+ decay at rest
- Good vertex and time resolution

3 tracks \rightarrow need of online reconstruction

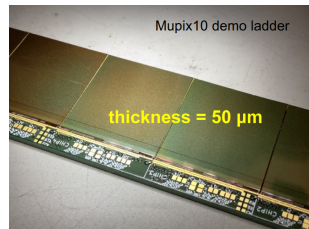
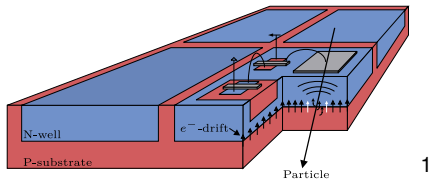
Mu3e Detector Concept



- Magnetic field of 1 T

- μ^+ stops at the target \rightarrow decay at rest

High Voltage Monolithic Active Pixel Sensors



sensor: 20 x 20 mm² pixel 80 x 80 μm²

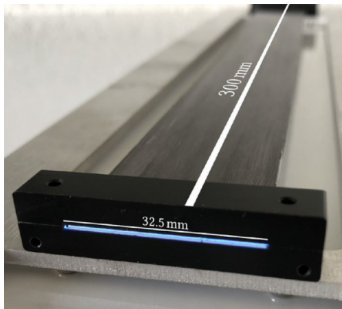
- Thinned down to 50 μm
- Fast charge collection

- Time resolution of a few ns
- Digitalization and zero suppression on the chip

→ up to 3 links of continuous 1.25 Gbit/s unsorted hit data

¹Ivan Perić et al., NIM A582 (2007) 876-885

Timing Detectors



- Fibre < 500 ps time resolution



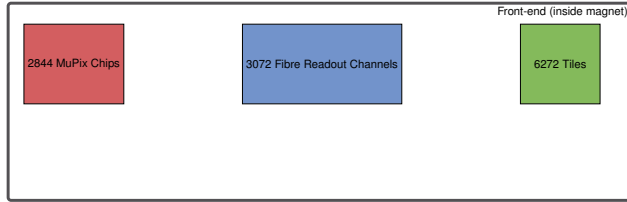
- Tiles < 70 ps time resolution

→ Readout via SiPM digitized via MuTRiG² chip, 1.25 Gbit/s unsorted hit data

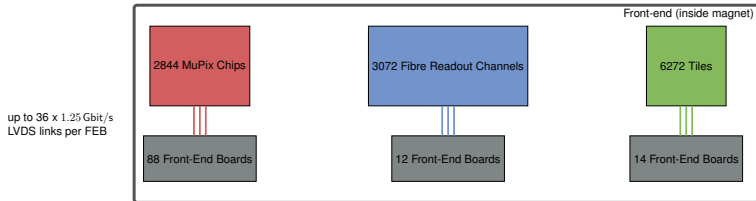
²Huangshan Chen et al., JINST 12 (2017) C01043

- 1 The Mu3e Experiment
- 2 Data Acquisition of Mu3e**
- 3 Mu3e Integration Run
- 4 Conclusion & Outlook

Mu3e DAQ

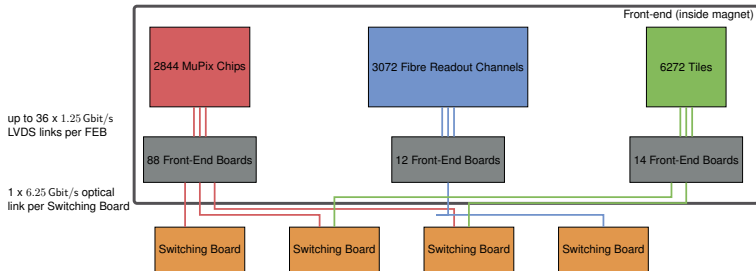


Mu3e DAQ

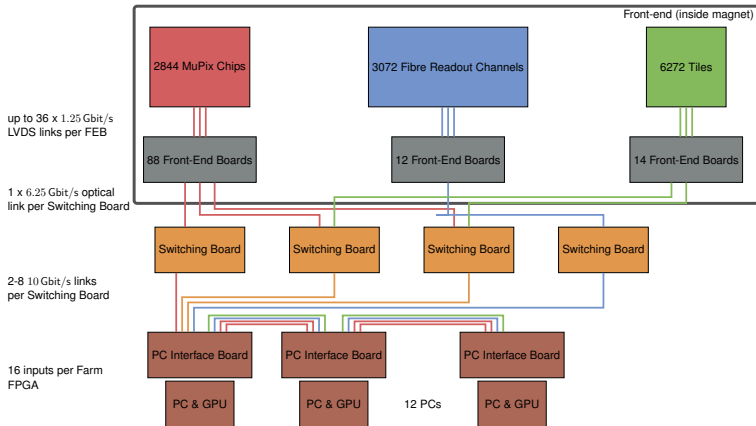


³K. Olchanski et al., MIDAS, <https://midas.triumf.ca>

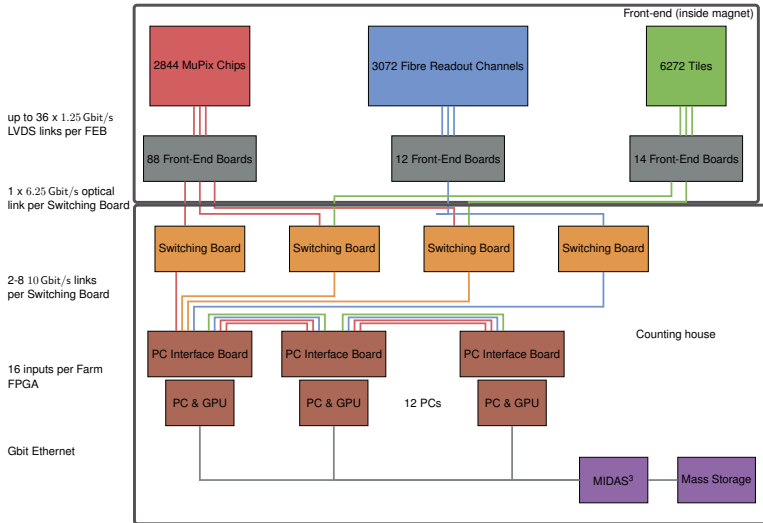
Mu3e DAQ



Mu3e DAQ

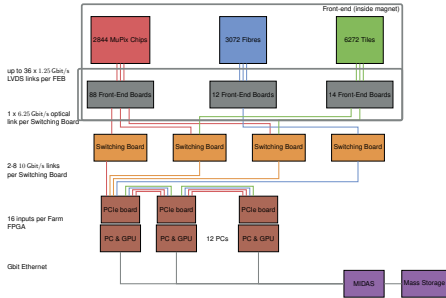


Mu3e DAQ

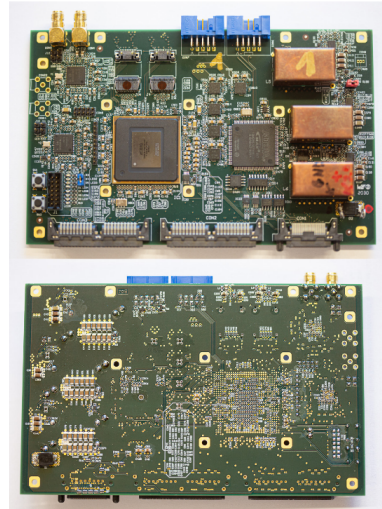


³K. Olchanski et al., MIDAS, <https://midas.triumf.ca>

Front-end FPGA Board



- Located inside the magnet
- Receives data from the detectors
- Sorts the data in time
- From electrical to optical
- **Timestamp correction of MuTRiG ASIC**

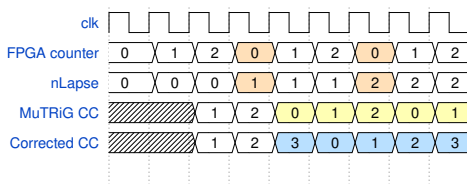


Timecounter correction MuTRiG

- MuPix is synchronised to 125 MHz and counts until 2^{11}
- MuTRiG coarse timecounter runs at 625 MHz
- 15-stage Linear-Feedback shift register with $2^{15} - 1$ deterministic states

→ Correction of early lapsing & deviation of 5

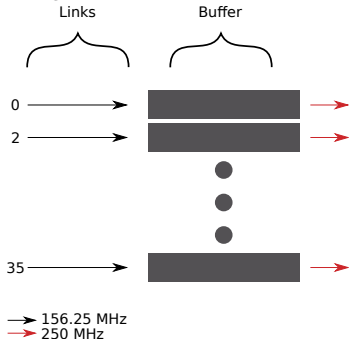
Timecounter correction MuTRiG



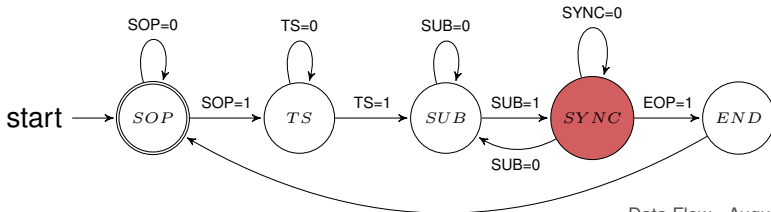
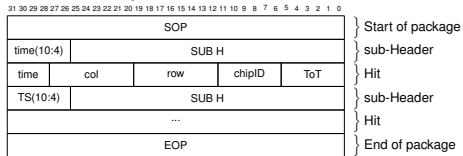
- Count on FPGA like MuTRiG counter (0 to 2)
- Count nLapse as overflows of FPGA counter
- Check receiving MuTRiG CC
- Subtracted nLapses to correct MuTRiG CC

```
process(clk)
begin
if rising_edge(clk) then
FPGA counter <= FPGA counter + 1;
if (FPGA counter = 2) then
nLapses <= nLapses + 1;
end if;
if (MuTRiG CC < FPGA counter) then
Corrected CC <= MuTRiG CC - nLapses;
else
Corrected <= MuTRiG CC -
(nLapses - 1);
end if;
end if;
end process;
```

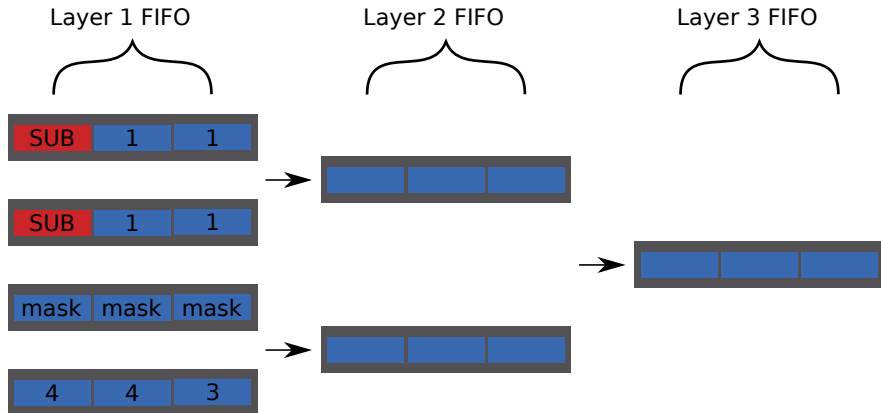

Synchronisation



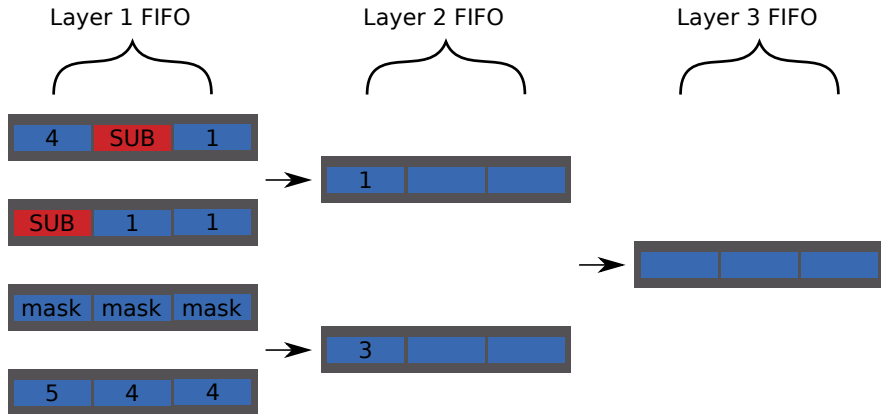
- 8 input links 32 bit x 156.25 MHz
- 1 output link 32 bit x 250 MHz



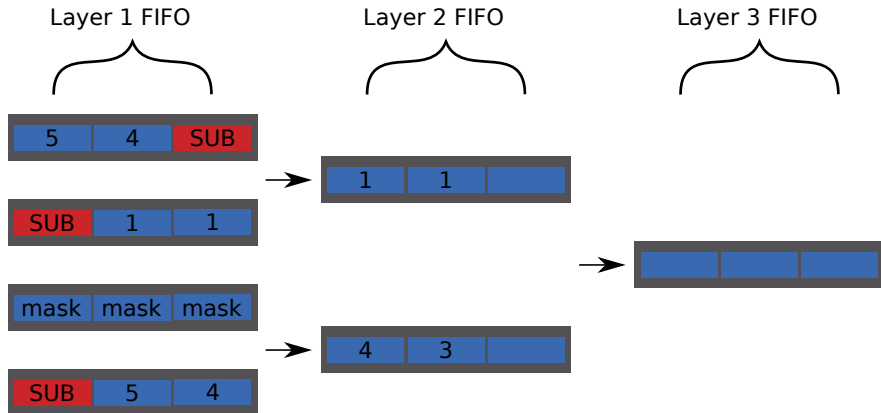
Sketch 4 to 1 Synchronisation Tree



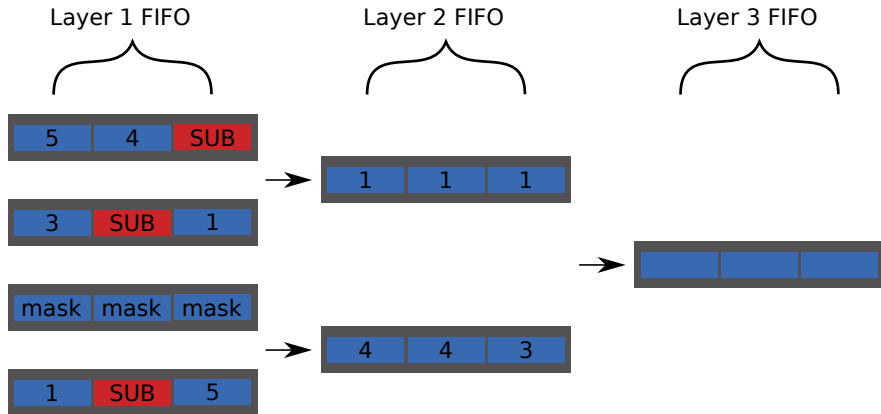
Sketch 4 to 1 Synchronisation Tree



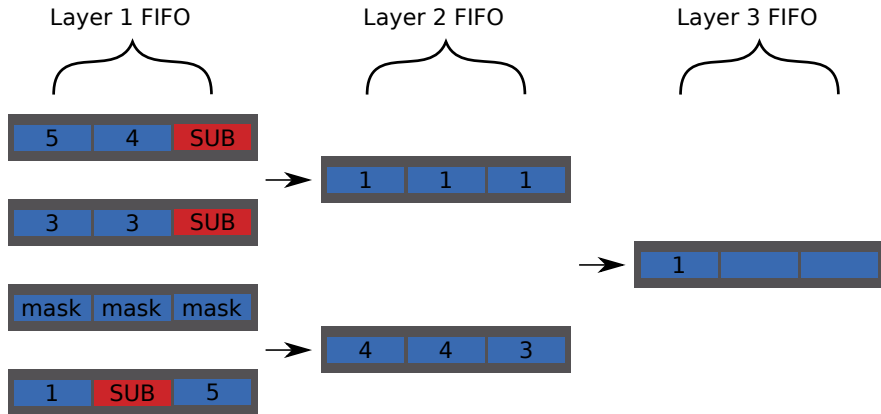
Sketch 4 to 1 Synchronisation Tree



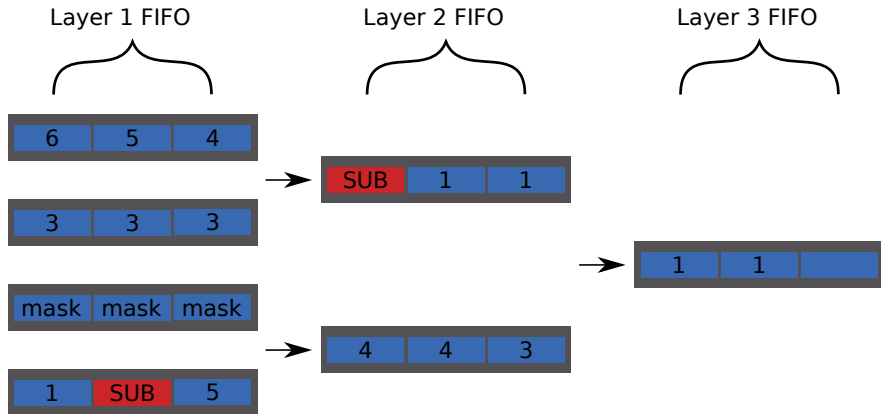
Sketch 4 to 1 Synchronisation Tree



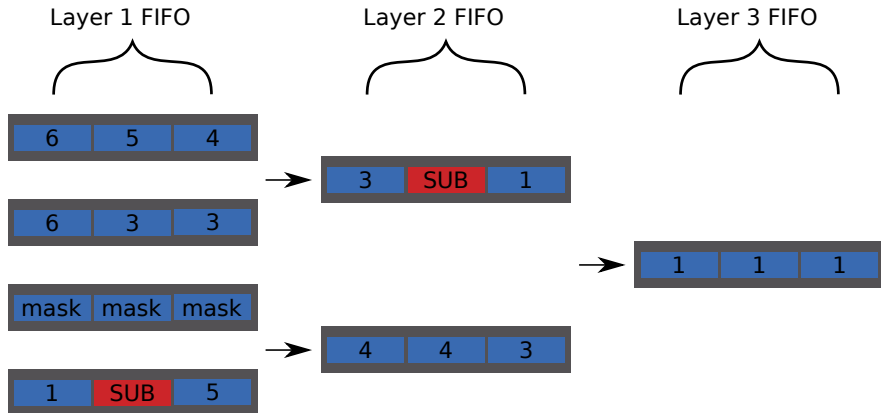
Sketch 4 to 1 Synchronisation Tree



Sketch 4 to 1 Synchronisation Tree

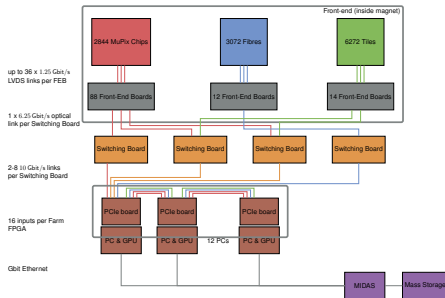


Sketch 4 to 1 Synchronisation Tree

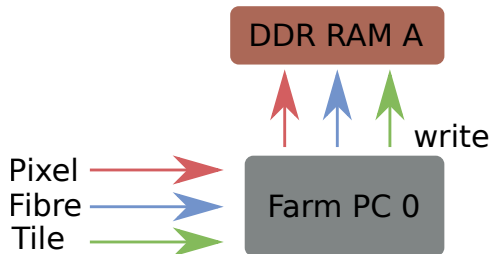


PC Interface FPGA Board

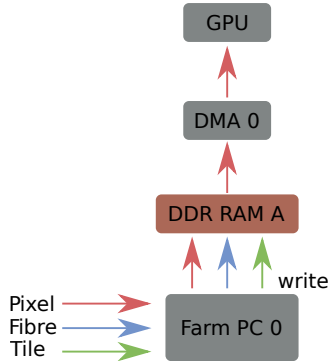
- Located outside the magnet, connected via 8-lane PCIe 3.0 to PC & GPU
- Synchronisation of different detectors
- Terasic DE5e-Net board
- **DDR 3/4 memory for buffering data for online tracking on the GPU**



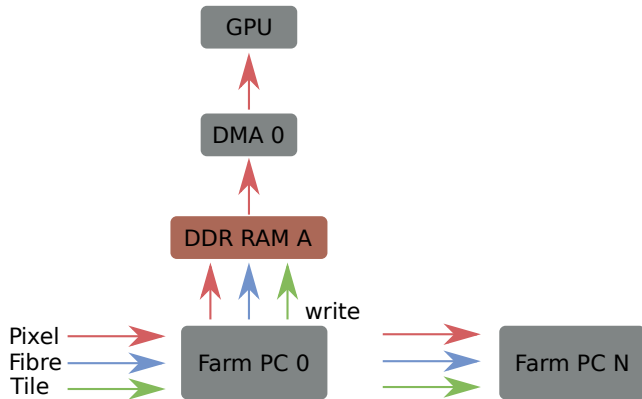
PC Interface FPGA Board Firmware



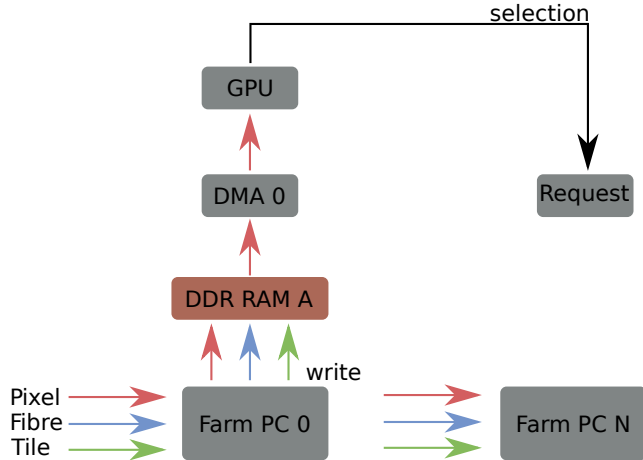
PC Interface FPGA Board Firmware



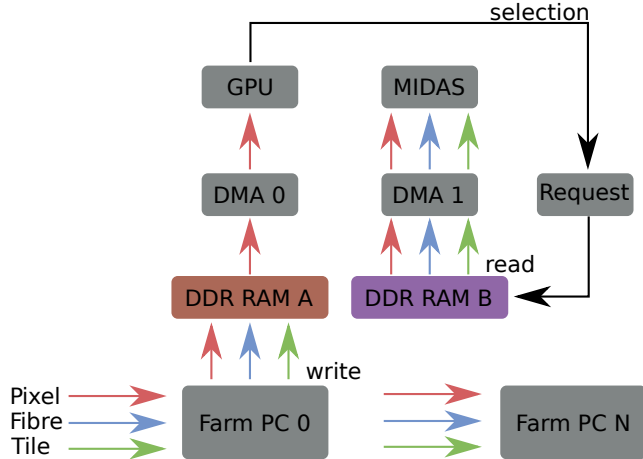
PC Interface FPGA Board Firmware



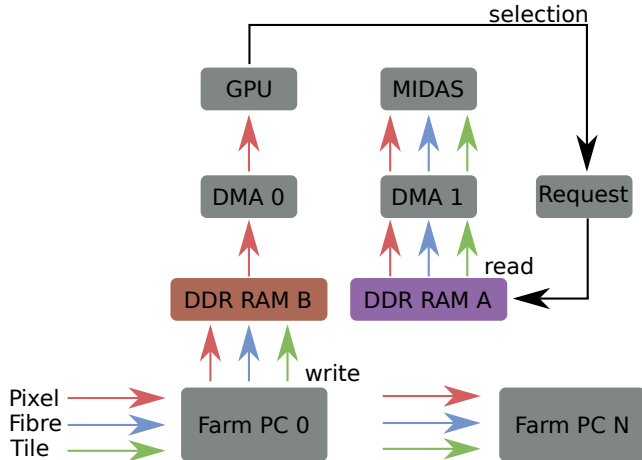
PC Interface FPGA Board Firmware



PC Interface FPGA Board Firmware

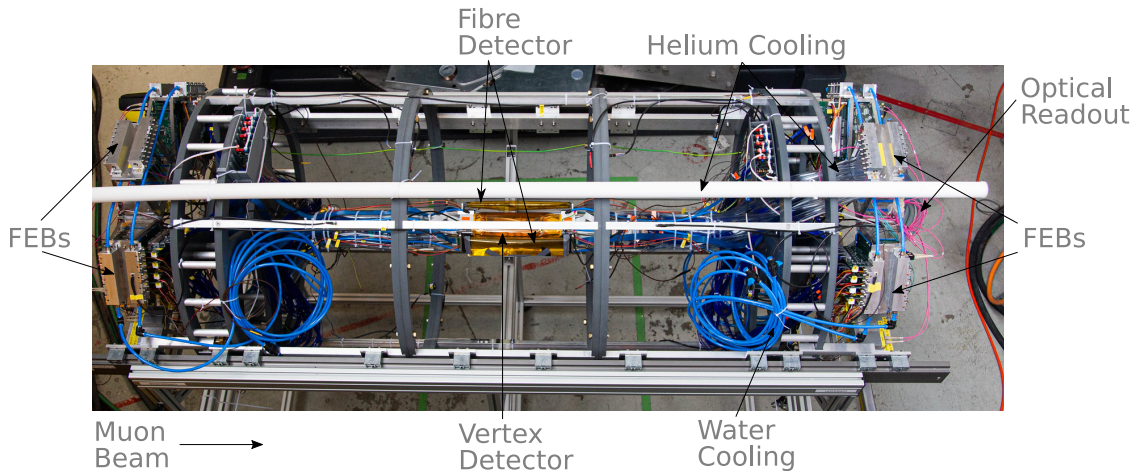


PC Interface FPGA Board Firmware

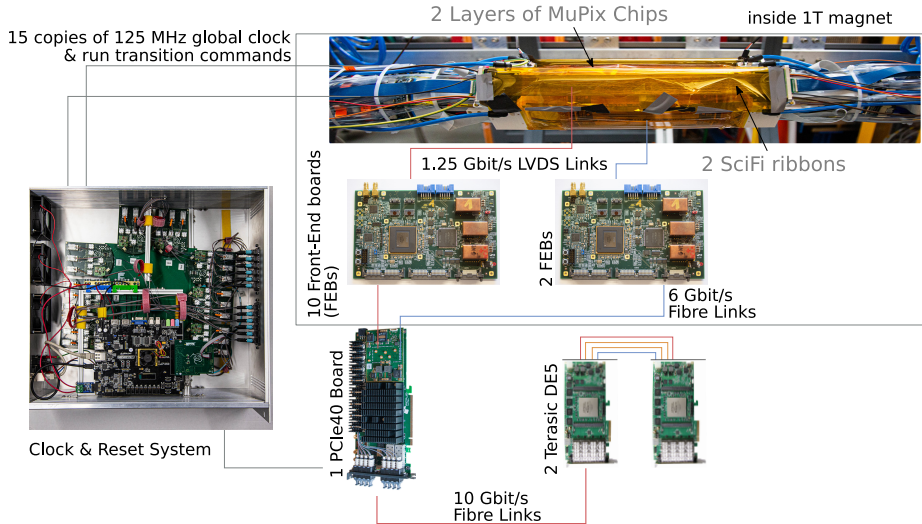


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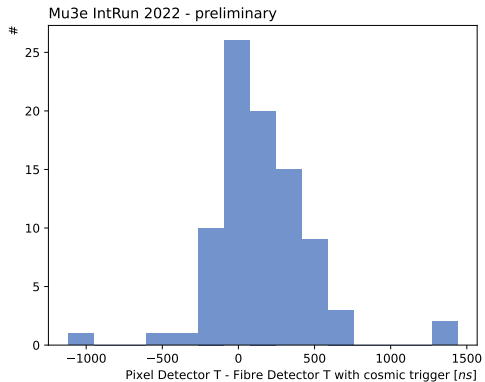
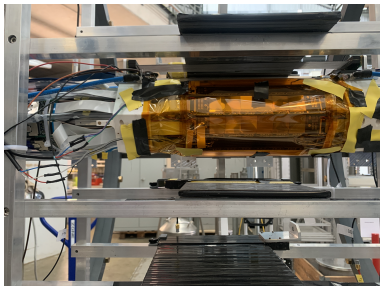
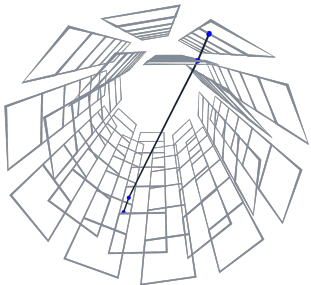
Mu3e Integration Run



Mu3e Integration Run DAQ



Mu3e Integration Results 2022



Mu3e Integration Results 2022

☰ Mu3e

- Status
- Transition
- OOB
- Messages
- Chat
- Elog
- Alarms
- Programs
- Buffers
- History
- OK/History
- MSCB
- Sequencer
- Event Dump
- Config
- Help
- mdump
- OnlineAna
- Mu3eDisplay
- Services
- DAQ
- Test
- Pixel
- SciF
- Tile
- FibreCounters

Run Status

Run 1263 Stopped	Start: Tue Jul 12 16:34:50 2022	Stop: Tue Jul 12 17:28:54	Data dir: /data1/run2022/d
Alarms: OFF	Restart: OFF		

1659526943 13:42:23.900 2022/08/03 [Logger.INFO] Client 'ana' on database 'ODB' pid 988041 does not exist and db_cleanup called by cm_p

Equipment

Equipment	Status	Events	Events/s
FEBCrates	Frontend stopped	930	0.0
Clock Reset	Frontend stopped	118672	0.0
SwitchingCentral	Frontend stopped	6346	1.0
LinksCentral	Frontend stopped	6345	1.0
SciFCentral	Frontend stopped	0	0.0
TimeCentral	Disabled	0	0.0
PixelCentral	Frontend stopped	6345	1.0
HAMEG1	Disabled	0	0.0
HeFlant	Frontend stopped	17316	0.0
HAMEG2	Frontend stopped	11672	1.0
HAMEG3	Frontend stopped	11672	1.0
HAMEG4	Frontend stopped	11672	1.0
HAMEG7	Disabled	0	0.0
Environment	Frontend stopped	17176	0.0
Water	Frontend stopped	17174	0.0
MuPix HV	Disabled	77	0.0
SciF HV	Disabled	0	0.0
HAMEG6	Frontend stopped	11672	1.0
ROSWCentral	Frontend stopped	902.4324	0.0
HAMEG5	Frontend stopped	11672	1.0
HAMEG8	Frontend stopped	11672	1.0
HAMEG9	Frontend stopped	11672	1.0

Logging Channels

Channel	Events	MB written	Compr.
#0: run01263.mid	902476761	57907.357	100.0%

Lazy Label	Progress	File Name	# Files
Clients			
mserver /mu3ebel		mbit00 /mu3ebel	Logger /m

Run Status

Alarms: OFF 3 Aug 2022, 18:

Transition: OOB Messages: Chat Stop: Alarms: Programs: Buffers: History: OK/History: MSCB: Sequencer: Event Dump: Config: mdump: OnlineAna: Mu3eDisplay: Services: DAQ: Test: Pixel: SciF: Tile: FibreCounters

Round Robin RO Debug

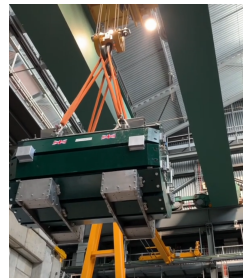
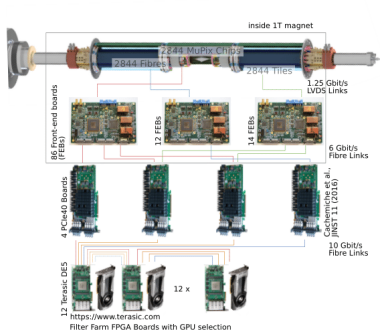
Tree Pixel US

Tree Pixel DS

Data Flow - August 3, 2022 - Slide 25

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Conclusion & Outlook



- Testing of PC Interface FPGA Board firmware with detector data
- Integration of the GPU selection
- Final commissioning of hit synchronisation

