Design of a 12-bit column-parallel ADC in the MAPS for real-time particle tracking

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INTRODUCTION

The Monolithic Active Pixel Sensor (MAPS) has been widely used in nuclear and particle physics. For example, the real-time particle tracking applications at the Heavy Ion Research Facility in Lanzhou (HIRFL) and the High-Intensity heavy-ion Accelerator Facility (HIAF) require MAPS to measure the particle hits' position, energy deposition, and arrival time. Thus, a MAPS with such capability is being designed in a 130nm process. As the critical part of this MAPS, a 12-bit column-parallel ADC has been designed to serve the pixels in every two adjacent columns. This ADC has been designed in a novel structure to satisfy the restricted constraints on area, power, speed, and accuracy. This paper will discuss the design and performance of this novel column-parallel ADC.

OVERALL ARCHITECTURE

As shown in Figure 1, the column-parallel ADC is designed as a fully differential cyclic architecture, mainly consisting of a multiplying digital-to-analog converter (MDAC), a sub-ADC, and a digital correction circuit.
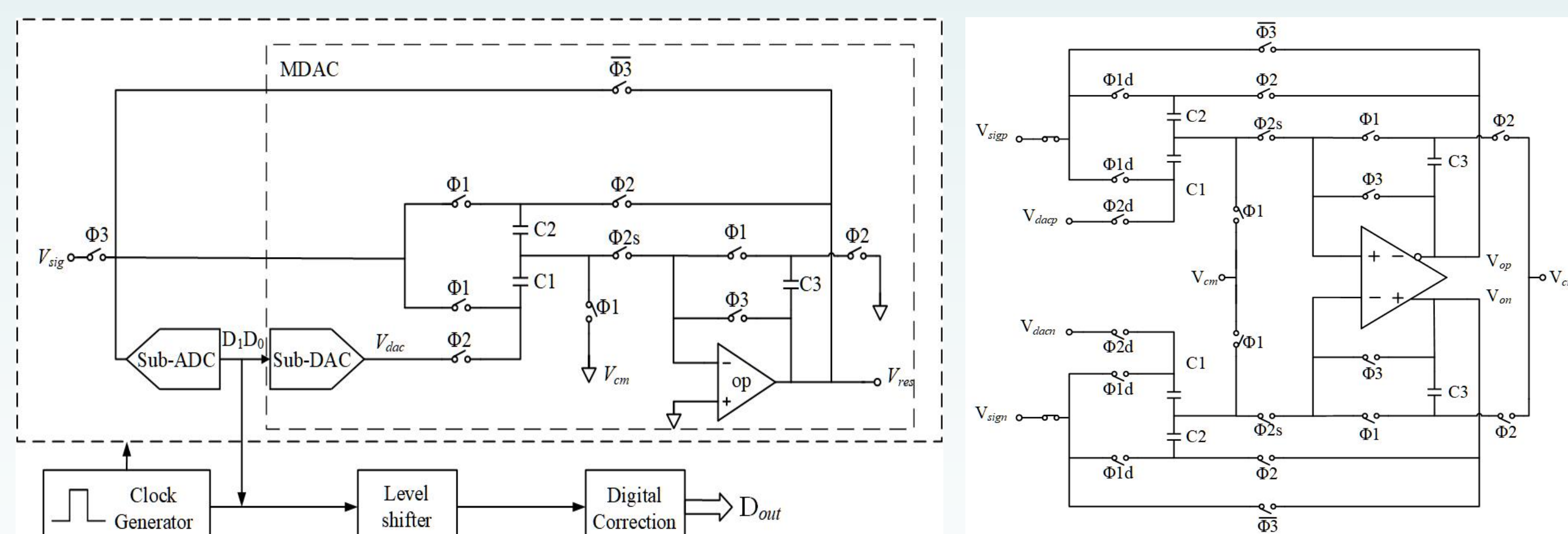

Figure 1 architecture of proposed Cyclic ADC

Figure 2 Schematic of the MDAC

OPTIMIZED MDAC DESIGN

The proposed MDAC stage employs a switched capacitor circuit to generate the residue signal and hold the signal for the next step. The MDAC circuits are shown in Figure 2. The schematic and timing diagram is shown in Figure 3, which explains the working

process of the circuit in detail. However, the problem caused by the charge accumulation on the capacitor C3 from the previous conversion cycle will influence the new cycle's first calculation. Therefore, to avoid this problem, two switches controlled by clock Φ3 are used to reset the charge on capacitance C3 in every input sample phase.

The sub-DAC generates the signal V_{dac} as presented in equation (1). The charge stored on the capacitance C1 transfers into C2 to generate the residue voltage V_{res}. In this MDAC, all the capacitance are equal, so the output can be expressed as equation (2).

$$V_{dac} = V_{dacp} - V_{dacn} = DV_{ref} = \begin{cases} V_{ref} & D_1D_0 = 00 \\ 0 & D_1D_0 = 01 \\ -V_{ref} & D_1D_0 = 11 \end{cases} \quad (1)$$

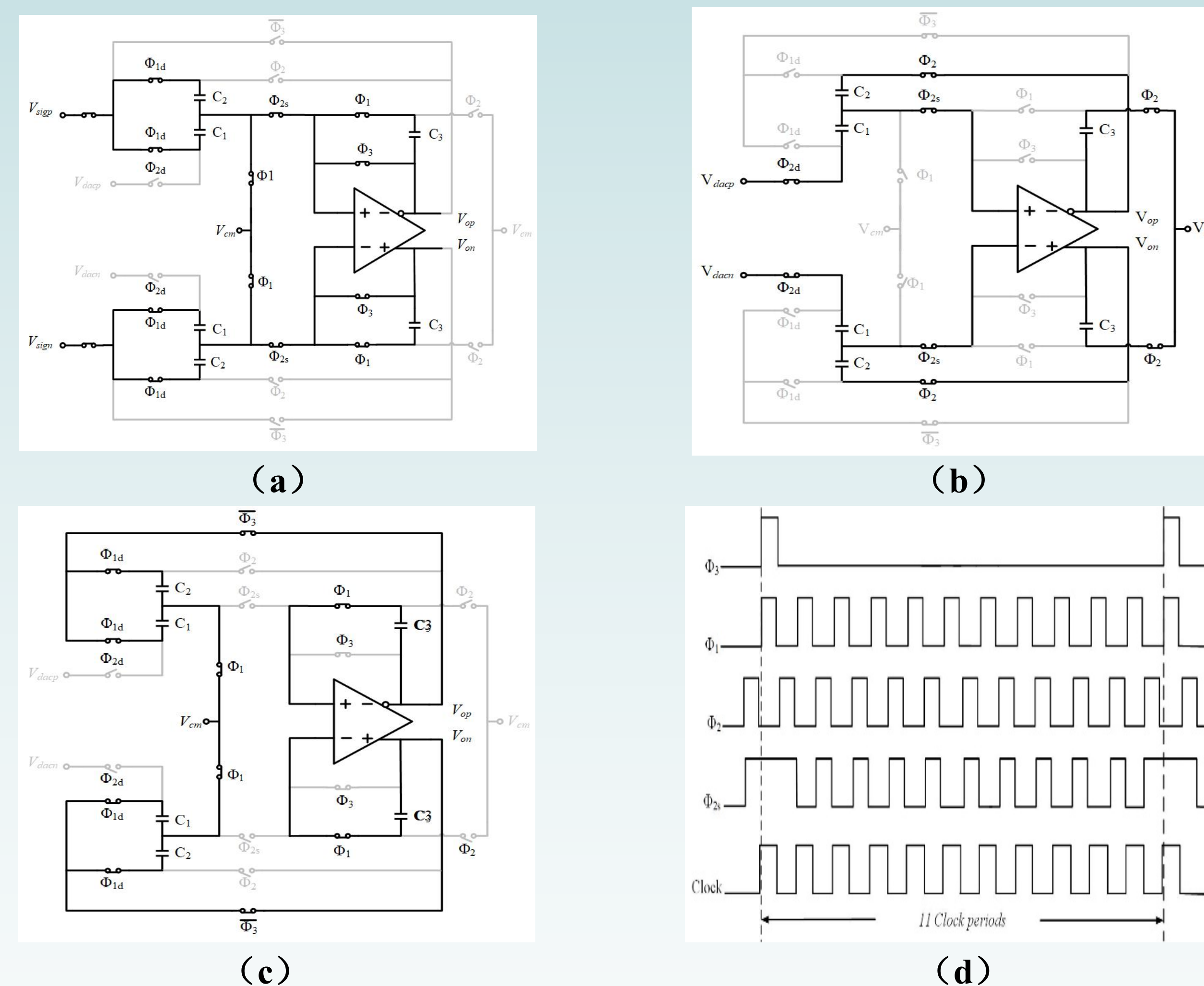$$V_{res} = 2V_{in} + DV_{ref} \quad (2)$$

Figure 3 MDAC schematic and timing diagram. (a) external sample phase. (b) amplification phase. (c) internal sample phase. (d) timing diagram.

THE DIGITAL CORRECTION

The digital correction circuit is mainly composed of the correction units consisting of a DFF and a half adder, which is shown in Figure 4. The clock Φr is to reset the carry signal of all the correction units when the first 1.5bit code is generated, as shown in Figure 5. After 11 Φ1 clock cycles, the corrected 12bit data D_{out} is stored in the DFFs output.
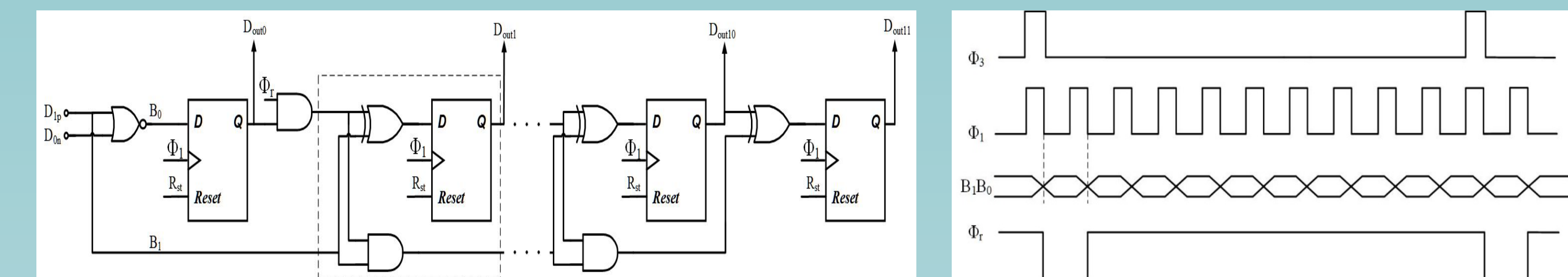

Figure 4 Structure of the digital correction circuit.
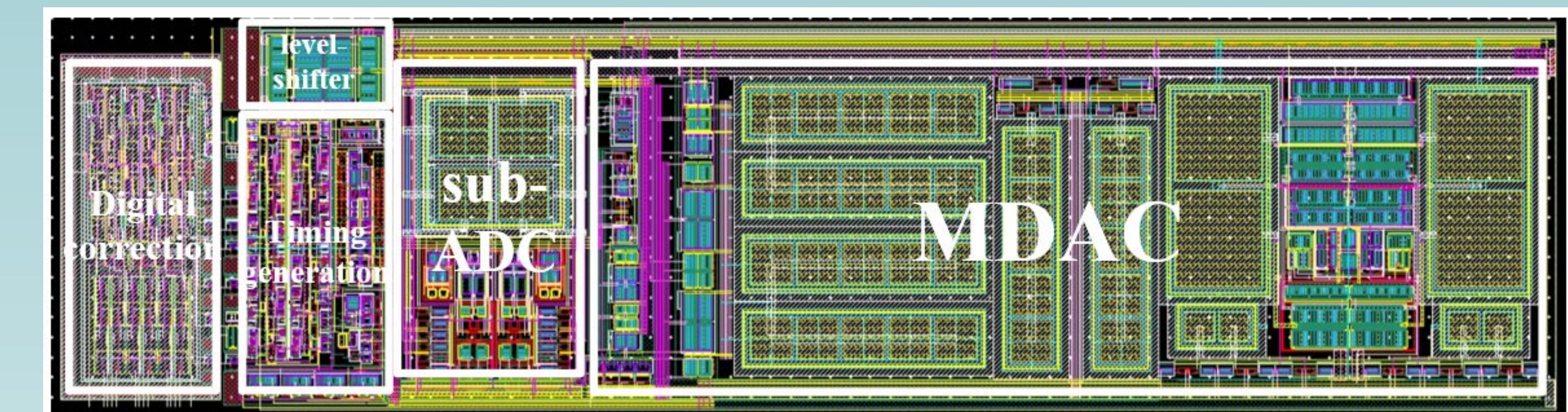

Figure 5 Timing diagram of the DCC.

Figure 6 Layout of this column-parallel ADC

CONCLUSION

The layout of the column ADC is shown in Figure 6. The performance of the ADC is shown in Figure 7. As the critical part of the MAPS with position, energy, and arrival time measurement capability for real-time particle tracking, a 12-bit column-parallel ADC has been designed to serve the pixels in every two adjacent columns. Each ADC covers a small area of 380×100 μm² and consumes power only of 7.6mW at a 3.3V power supply. At 40MHz internal clock frequency, the ENOB of ADC reaches 11.61bit at the sampling rate of 3.63MHz, with the SNDR of 71.65dB.
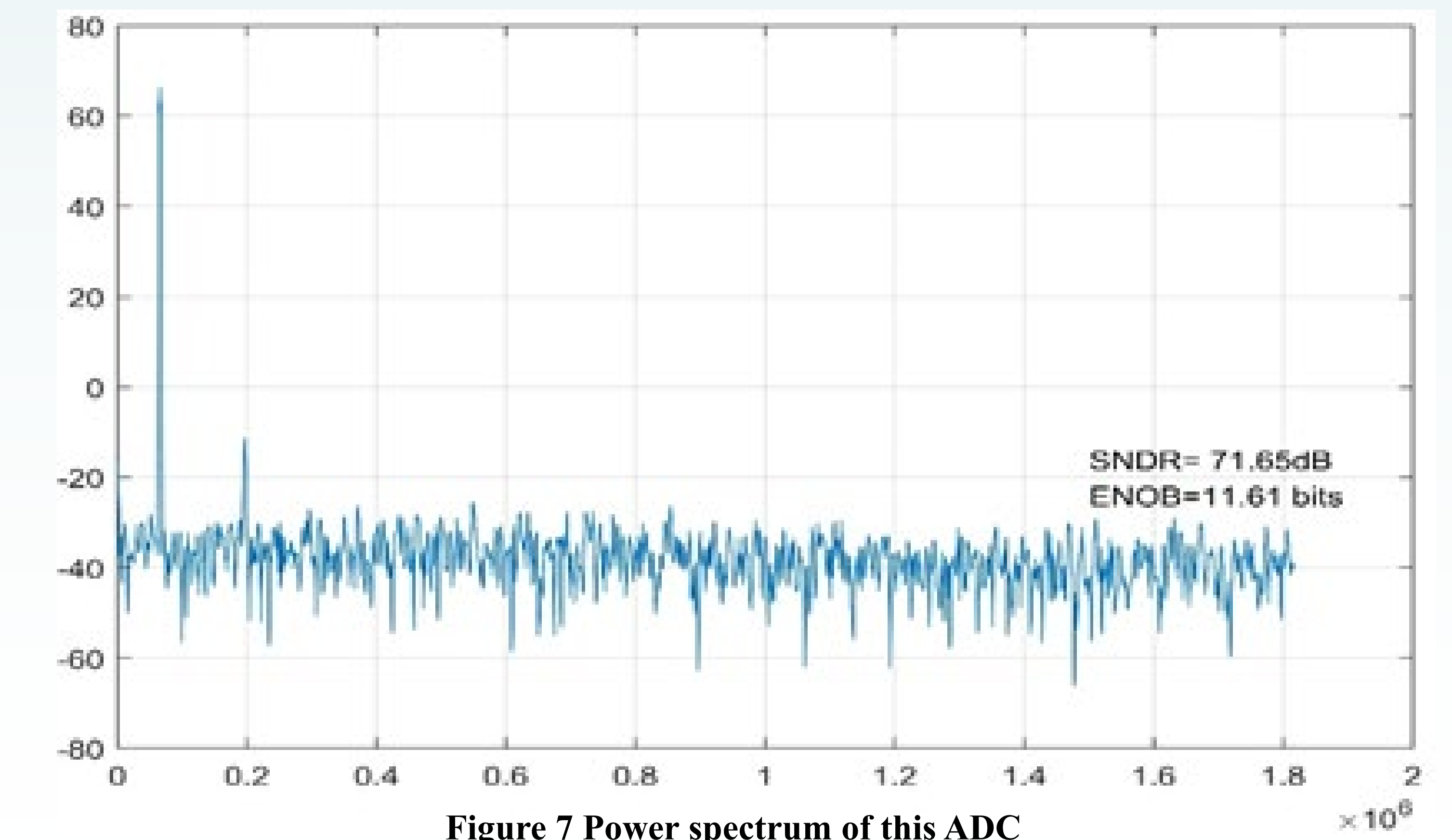

SNDR= 71.65dB
ENOB=11.61 bits

Figure 7 Power spectrum of this ADC