Design of a Pipeline Regional ADC for Monolithic Active Pixel Sensor

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ABSTRACT

A Monolithic Active Pixel Sensor (MAPS) has been designed in a 130nm process for HIRLF(Heavy Ion Research Facility in Lanzhou) and HIAF(heavy-ion Accelerator Facility). This MAPS can measure the energy deposition, the hit position, and the arrival time of the particle hit. As the critical component of this MAPS, a regional ADC converts the analog energy and time signal from the pixels into digital data. This regional ADC is designed as an optimized pseudo-differential pipeline architecture. In addition, digital correction is employed for the output codes of each stage to improve the accuracy.

Table. 1 Key parameter of the Pipeline Regional ADC

Parameters	Description
Process	130 nm CMOS
Chip Size	1250×450μm²
Power Consumption	83.02mW
Sampling Frequency	40MS/s
SNDR	71.81dB
ENOB	11.64bit

ARCHITECTURE

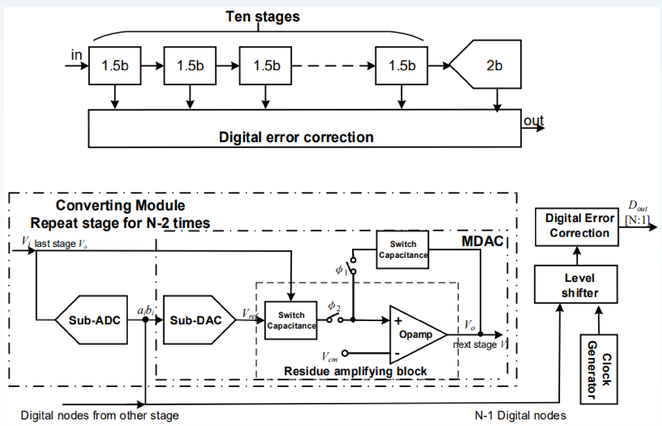

Fig. 1 Structure of the pipeline ADC

Fig. 1 shows the architecture of this regional pipeline ADC. The ADC consists of ten 1.5-bit stages and a final 2-bit flash stage. This pipeline ADC is designed as an optimized pseudo-differential pipeline architecture with no sample and hold module settled before. the first stage to reduce the power consumption. With the digital correction for the output codes of each stage, this ADC can reach a precision of 12-bit. This ADC includes a clock generator and a digital error correction module, apart from the pipeline converting module First, the 1.5-bit sub-ADC quantifies the sampled analog signal coarsely. Then, transforming it into the corresponding analog quantity. After the subtraction operation between the analog signal, the residue can be amplified precisely by a gain of two through an amplifier with a negative feedback structure. Finally, the sub-ADC can capture the amplified result in the next stage for further quantification.

SUB-MODULE DESIGN

A. The Sub-ADC

The specific structure of Sub-ADC is shown in Fig.2. it consists of two fully differential comparators. First, the analog signal is sampled and calculated by the switched capacitance circuit, controlled by two-phase non-overlapping clocks. Then the signal transfers to a dynamic comparator to compare with the reference voltage.

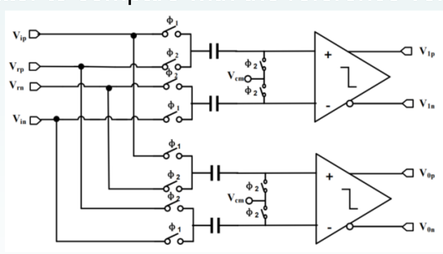

Fig. 2 Schematic of the comparator

B. The MDAC

Fig. 3 shows the schematic of the MDAC, in which a charge reversal structure has been adopted. the amplifier's operating point can stabilize to the common-mode voltage when Φ1 is high. and When Φ2 comes high, A precise multiplying circuit can be realized.

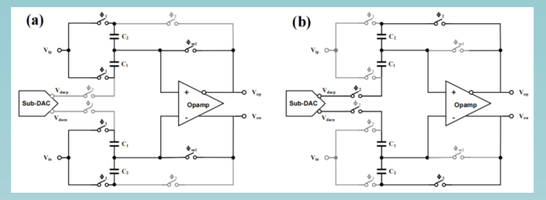

Fig. 3 Schematic of the MDAC. (a)sampling phase. (b)amplification phase.

C. The Digital Correction Module

The digital correction module, shown in Fig. 4, synchronizes the digital code generated from each stage. The delay part adopts a dynamic structure consisting of inverters controlled by Φ1 or Φ2.

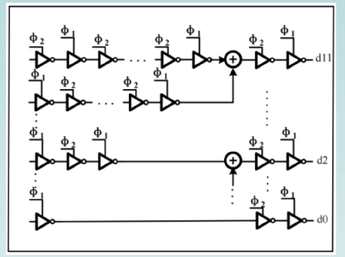

Fig. 4 Structure of the digital correction module

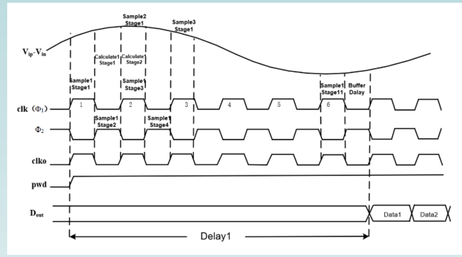

Fig. 5 Operation timing diagram of the ADC

D. Operation timing logic

As shown in Fig. 5, a timing interlaced structure is used to improve the utilization rate of the switch-capacitor circuit and curtail the power consumption.

RESULTS

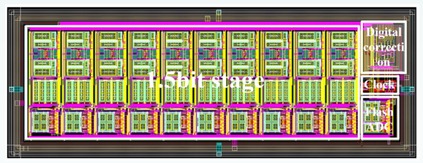

Fig. 6 Layout of the pipeline ADC

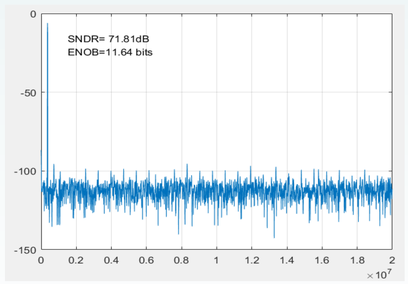

Fig. 7 The power spectrum of this ADC

The layout of the pipeline ADC is shown in Fig. 6, which occupies an area of 1250×450μm². Figure 7 demonstrates the performance of the regional ADC, where the signal-to-noise ratio (SNDR) is 71.81dB with an effective number of bits (ENOB) of 11.64bit.