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EJFAT

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To increase the science rate for high data rates (100Gbs - 1Tbs) with guaranteed Quality of Service (QoS), JLab is partnering with ESnet for proof-of-concept engineering of an 1.5 network layer AI/ML directed dynamic Compute Work Load Balancer (CWLB) of UDP streamed data using an FPGA for fixed latency and high throughput in order to demonstrate seamless integration of edge / core computing to support direct experimental data processing for immediate use by JLab science programs and others such as the EIC as well as data centers of the future. The ESnet/JLaB FPGA Accelerated Transport (EJFAT) project is targeting near future projects requiring high throughput and low latency for hot data, and data-center horizontal scaling applications for both hot and cooled data.

The CLWB distributes commonly tagged UDP packets to individual and dynamically configurable destination endpoints. Additional tagging provides for individuated stream reassembly at the endpoint with horizontal scaling. The CLWB is an FPGA programmed at the data-plane level with both P4 and RTL to effect a packet parsing state machine that performs table look-ups through several levels of indirection to dynamically map LB meta-data to destination hosts and rewrite the UDP packet header as required. Control plane programming uses conventional host computer resources to monitor network and compute farm telemetry in order to make dynamic AI/ML guided decisions for destination compute host redirection / load balancing.

Minioral

Yes

IEEE Member

No

Are you a student?

No

Author: GOODRICH, michael

Presenter: GOODRICH, michael

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