An Accurate Small Direct Currents Measurement System Based on Low-noise and Stable Amplifier

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1 Introduction

The accurate measurement of small direct currents has wide applications in fundamental metrology and physical sciences. In radionuclide metrology, the accuracy and linearity of the ionization current measurement limit the uncertainty levels in activity determinations. In several physical experiments (e.g., particle beam and single-electron tunneling), the accurate measuring of the small direct current is needed.

The system designed in this paper is to improve the measurement uncertainty of the ionization current in radionuclide metrology. Further, to serve as a universal picoammeter and calibrator. The design goals are as follows:

- Real-time measuring, processing, and display.
- Low noise level, fast settling, and low burden voltage.
- Overall measurement uncertainty: $u < 100$ ppm

3 The System Structure

The overall block diagram of the measurement system is in Fig. 1. Input current is amplified, sampled, filtered, calculated, and then displayed to user in real time.

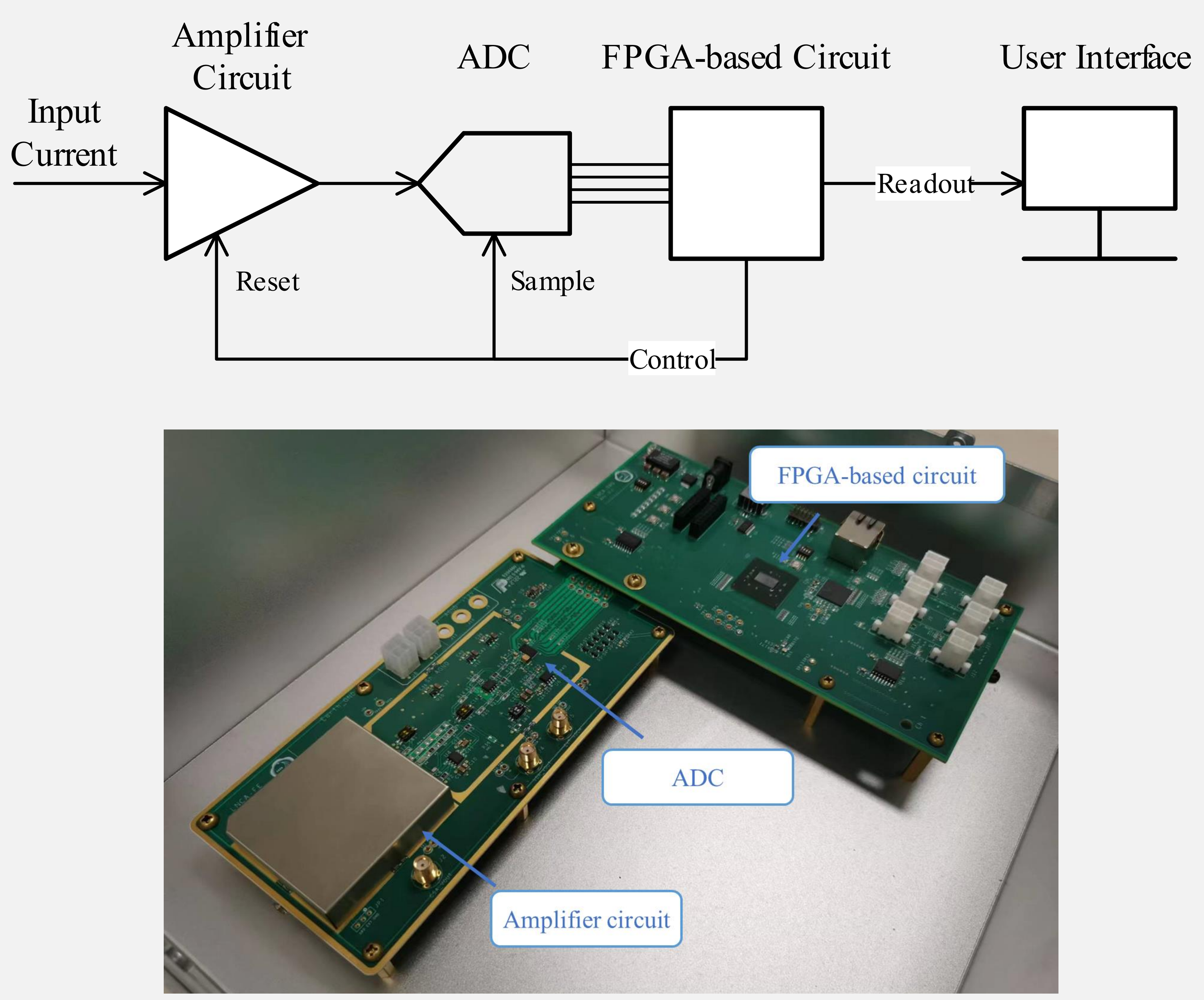

Fig. 1. The overall block diagram and photo of the small direct current measurement system.

4 Detailed Design

a) The Low-noise and Stable Amplifier

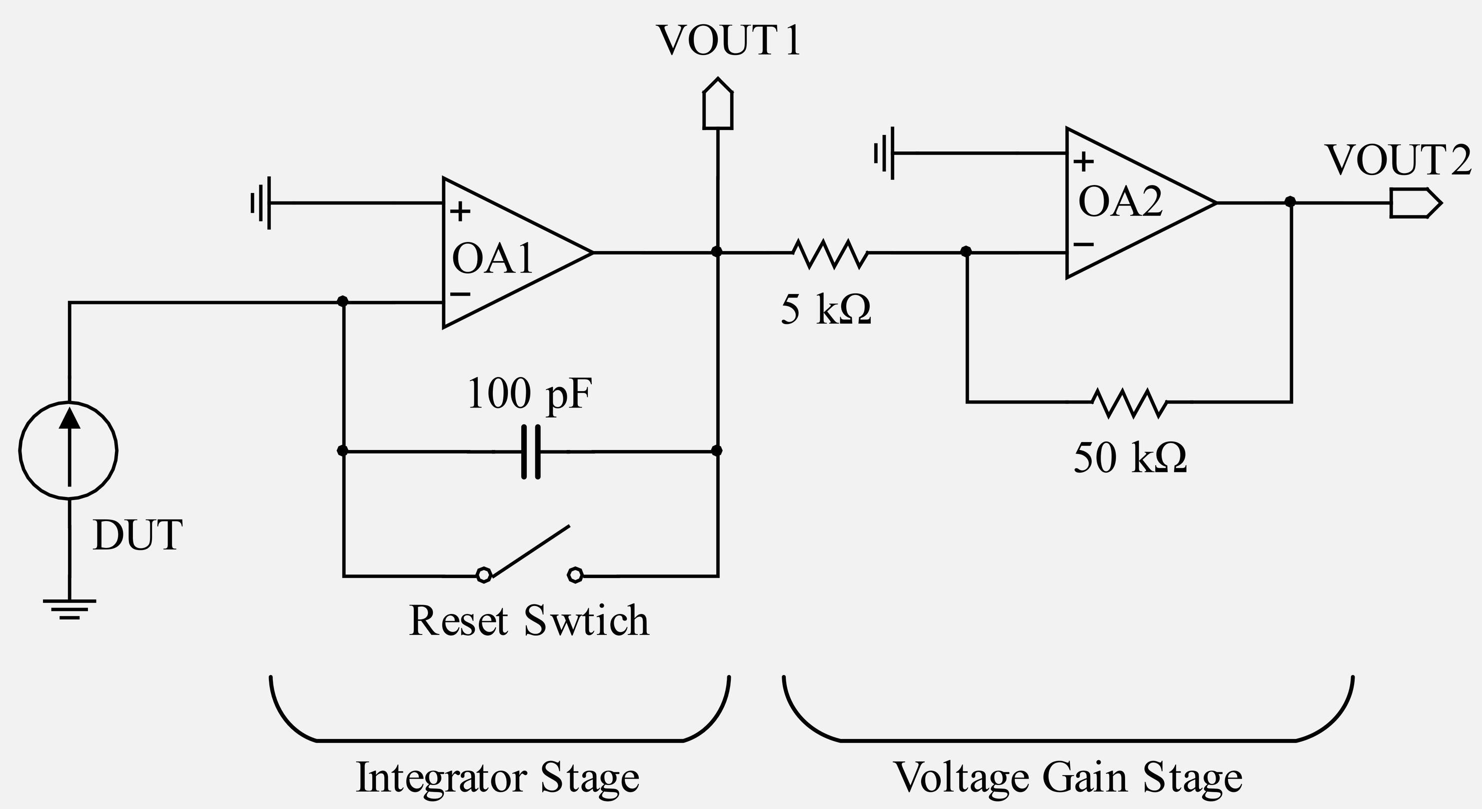

Fig. 2.The simplified schematic of the amplifier circuit that has two gain stages.

Design ideas for this circuit:

- Low noise input integration stage:
  - Providing 10^8 transimpedance gain: $G_1 = I \times \frac{T}{C}$
  - Current to voltage conversion.
  - No feedback resistor generating thermal noise.
- Inverting voltage gain stage:
  - Providing remaining 10-fold voltage gain.
  - 50 kΩ/5 kΩ resistor pair: implemented by multiple metal film resistors to ensure precision.

Besides, A fully-differential output amplifier implemented as a 2nd order Bessel filter (not shown in fig. 2) is used for single-to-differential conversion, buffering the ADC input, and filtering.

b) The control and readout circuit

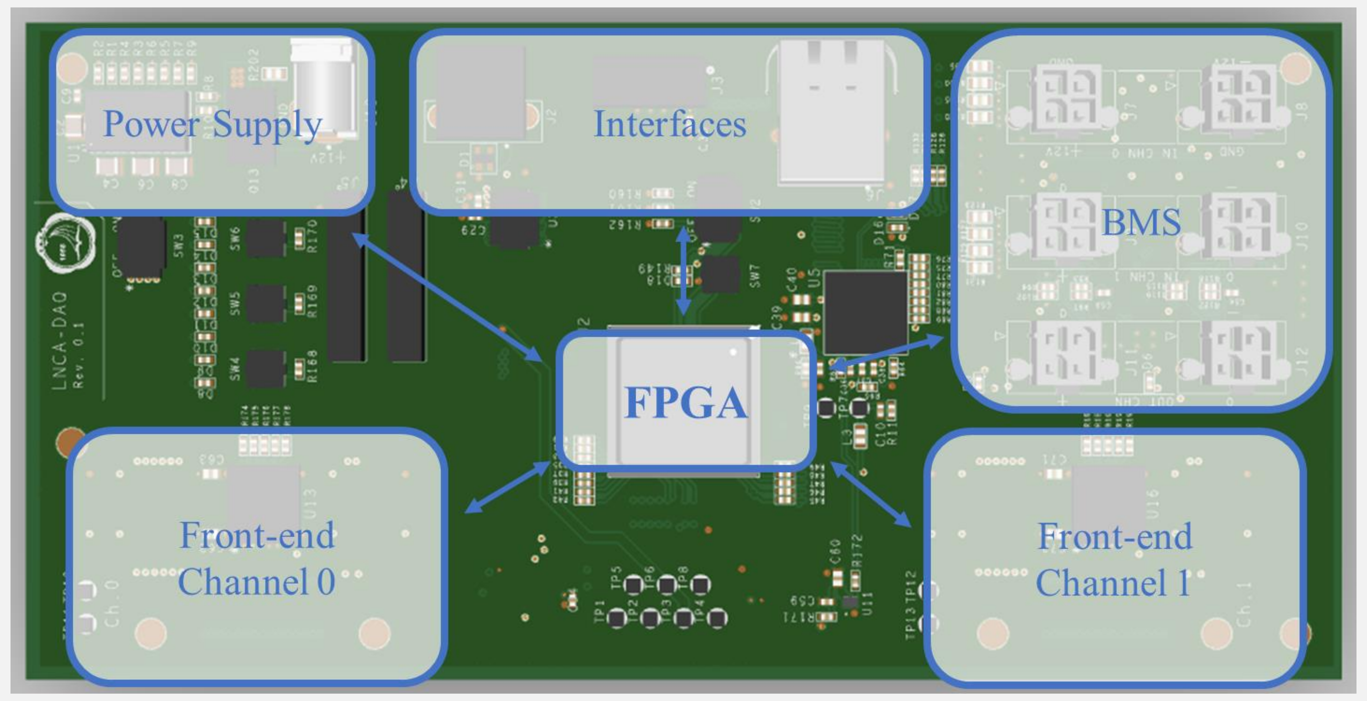

Fig. 3. Modules of the control and readout circuit.

This circuit mainly includes:

- Two individual galvanic-isolated front-end circuit interfaces.
- The dual rails battery management system (BMS) provides an uninterruptible power supply for the front-end circuit.
- Ethernet and USB interfaces.
- An FPGA whose functions are shown in fig. 4.

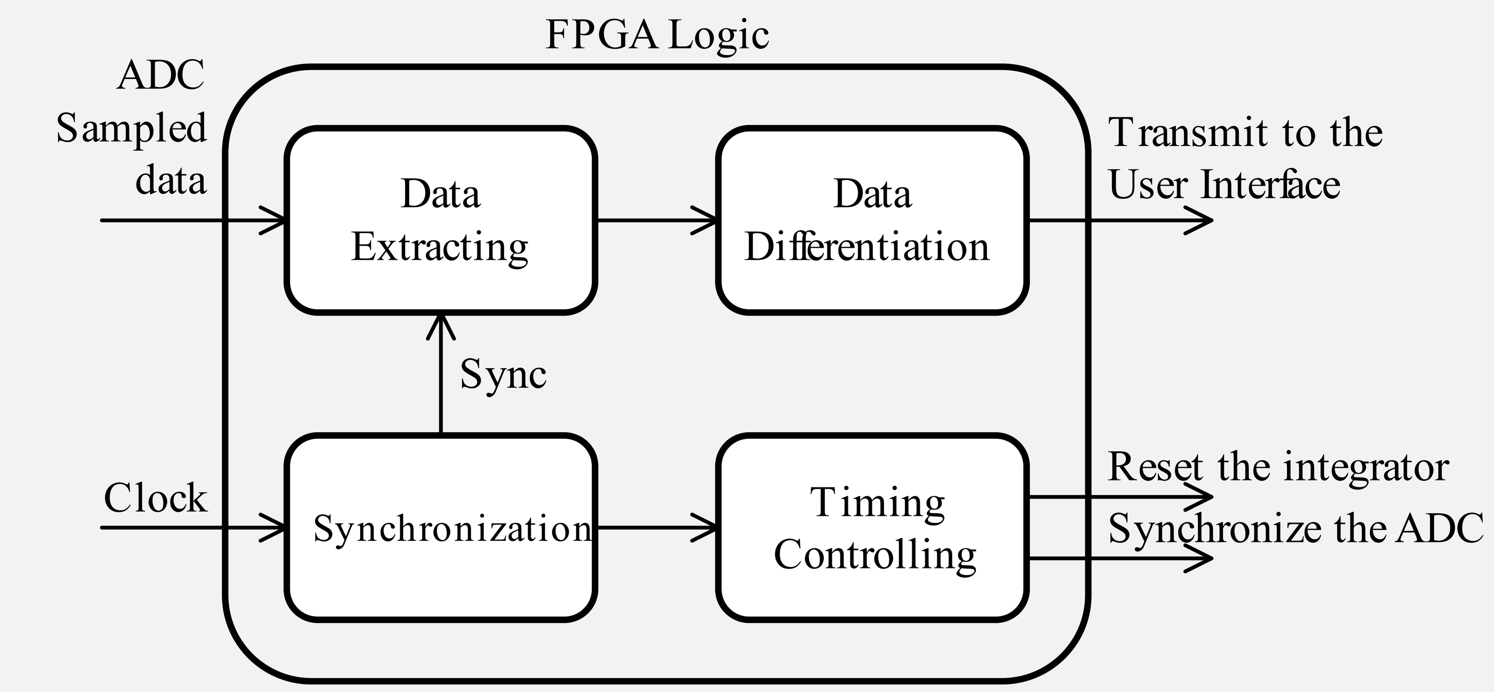

Fig. 4. FPGA Logic functions

5 Simulation and Analysis

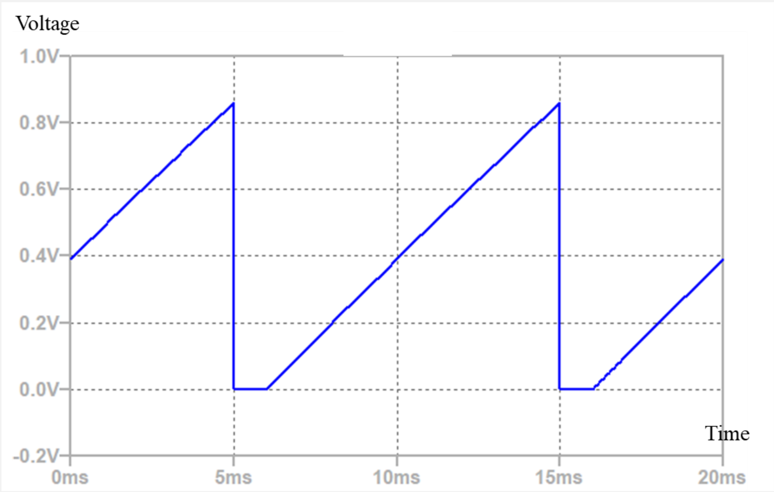

Fig. 5. Analog circuit transient simulation

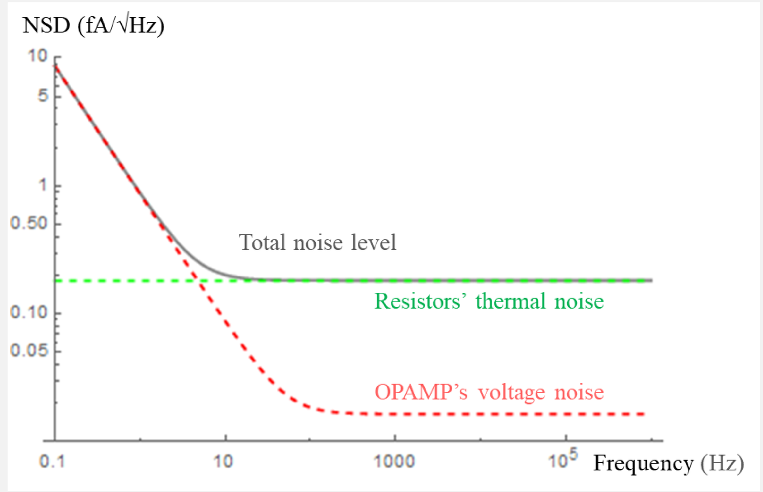

Fig. 6. Analog circuit noise estimation

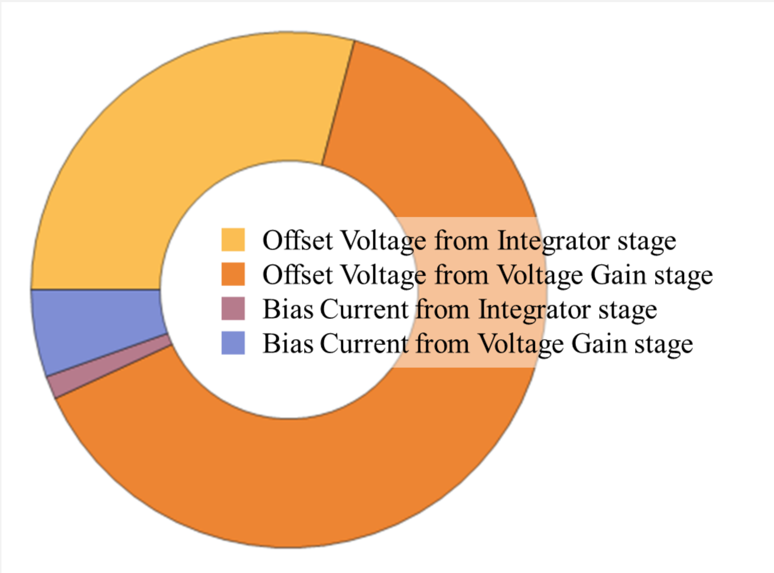

Fig. 7. DC offset contributions

According to simulations, the noise spectral density (NSD) of the front-end circuit is at fA/√Hz level (see fig. 6). The overall DC offset is about several mV, which is mainly contributed by the V_{OS} of the voltage gain stage (see fig. 7). The transient and frequency response of each gain stage are also simulated and analyzed.

The PCBs have been produced and are currently debugging. Further tests will be implemented soon to verify the simulation results and the design requirements.