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NTIMP1—A Fast Pulse Readout Chip with 1.2V Power Supply for Time-of-Flight Measurement in HFRS OF HIAF

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Abstract

A very fast pulse readout ASIC, NTIMP1, with 1.2V power supply is presented in this work. It is going to be used as front-end electronics (FEE) for reading out the timing resistive plate chambers (RPCs) in the time of flight (TOF) wall of RIBLL2 experiment of the the High Intensity Heavy Ion Accelerator Facility (HIAF), China. NTIMP1 is fabricated using 0.13μm standard CMOS Technology, and the eight-channel front-end readout architecture is featured with a high-bandwidth preamplifier dealing with differential current input, a discriminator with adjustable thresholds, and a LVDS module ensuring long-distance signal transmission. The input of NTIMP1 can range from 4 fC to 2048 fC and the input impedance of the preamplifier can be adjusted externally with an off-chip resistor, so as to match with the strip electrode impedance of RPCs. The bandwidth of the preamplifier is 640MHz, which allows a very short signal peaking time of no more than 800ps. The jitter of the leading edge is lower than 10ps suggesting that NTIMP1 is suitable for high-resolution TOT measurement as well as time-slewing correction.

Introduction

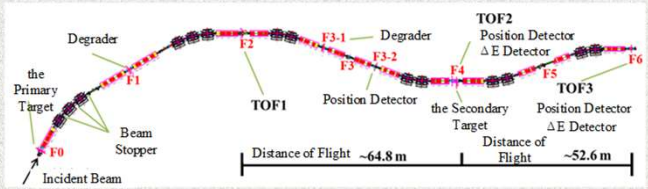

Fig.1 TOF measurements of HFRS in RIBLL2 at HIAF

The High Intensity Heavy Ion Accelerator Facility (HIAF) is the world's first advanced heavy ion research facility with the combination of superconducting linear accelerator, synchrotron and storage ring[1]. It perfectly combines the characteristics of high pulse current intensity of linear accelerator and high energy of synchrotron. High energy FRagment Separator (HFRS) is one of the most significant facility to investigate the radioactive physics in HIAF, such as particles identification through Bρ-TOF-ΔE methods. In HFRS, diamond detectors are used as TOF detectors which deliver fast signals when an ionizing particle is passing through. Typical values of the anode signals at 50 Ω impedance are as follows: rise time, 1ns; FWHM, 3~4ns; Fall time, 600ps; amplitude, <100mV; equivalent charge, 20~2000fC.

ASIC description

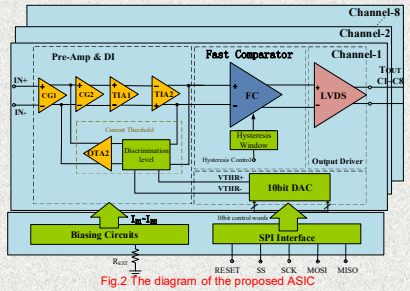

Fig.2 The diagram of the proposed ASIC

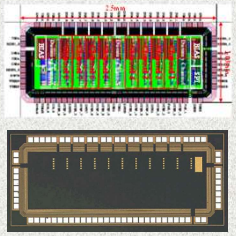

Fig.3 Layout and photomicrograph of the prototype chip

NTIMP1 has a die-area of 2.5mm×1.03mm and contains eight identical channels with common biasing circuits and SPI interface. A NTIMP1 channel consists of a preamplifier-discriminator stage, fast comparator, LVDS transmitter and a 10-bit DAC that generates differential threshold voltages for signal discrimination. Using an external resistor, the biasing circuits offer appropriate voltage/current references for the whole ASIC, especially, a constant-transconductance for CG input transistor for impedence matching with detector's transmission line.

PA and DI Design Considerations

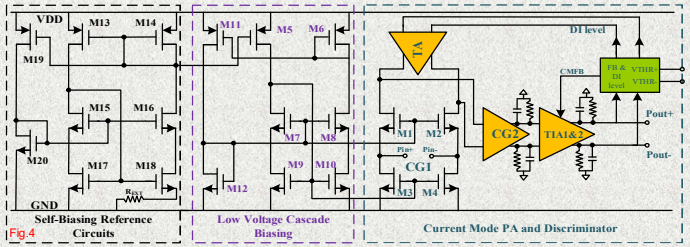

Fig.4

- Extern resistor R_{EXT} decide the working current of self-biasing circuits, as well as the gm of M1 and M2.

$$g_{m(M1)} = \frac{2\sqrt{M18/M17} - R_{EXT}}{R_{EXT}} \cdot \sqrt{\frac{M1 \cdot M5 \cdot M3}{M18 \cdot M14 \cdot M9}}$$

(Mn stands for the W/L of transistor Mn.)

- Cascade biasing circuits offer low biasing-voltage for input transistors M1 and M2 of the Common-Gate stage-1 (CG1), ensuring better dynamic range at the outputs of CG2.
- Input impedence of CG1 can be adjusted through tuning R_{EXT}, and calculated as $1/g_m(M1)$. R_{EXT}≈150Ω, is suggested to make the Input impedence of CG1 around 50 Ω.
- When the differential input signal is smaller than input threshold, a positive feedback keeps output baseline at ½(VTHR+ - VTHR-). On the opposite, a negative feedback helps setting up the output signals to propriate values.

Simulation and Experimental results

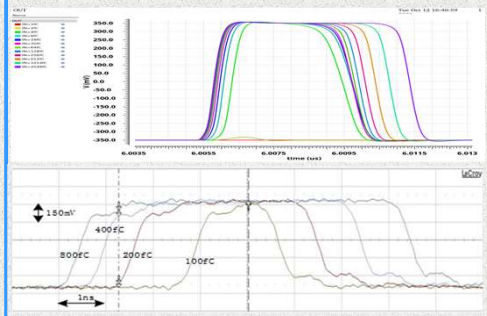

Fig.5 The simulation results and preliminary test of LVDS output

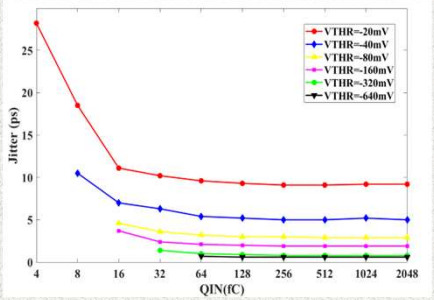

Fig.6 The simulation results of single channel time jitter

Parameters	NINO	PADI-2	PADI-8	NTIMP1
Process	CMOS 0.25μm	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.13μm
Channels	8	4	8	8
Power Supply(V)	3.3	1.8	1.8	1.2
PA Bandwidth (MHz)	\	293	411	640
PA Conversion Gain (mV/fC)	\	7.8	30	11.4
ENC (e-, rms)	< 5000	1753	1145	1334
Input Impedance (Ω)	40-75	37-370	30-160	35-120
Front Edge Time Jitter (ps, rms)	< 25	< 50	< 25	< 10 (VTHR<-40mV)
Power Diss. (mW/Channel)	27	17.4	17	6.1

Tab.1 Simulation Results and Comparison with Other Similar Chips

Summary

- A fast pulse readout ASIC, NTIMP1, is developed in order to readout the signals of diamond detector for TOF measurement in HFRS facility. The time resolution of the whole TOF system is restricted as 150 ps and the output jitter of NTIMP1 is turned out to be 20 ps.
- The signal path is optimized by lowering the impedence of key points, making the signals setting-up as fast as possible, so, at the discrimination-level, the projective timing jitter of temporal noise can be greatly rejected.
- Eight front-end channels are fabricated in the ASIC, suggesting its potential for reading out signals from pixel-array detectors.
- NTIMP1 is designed for TW correction through TOT measurement, benefitting from which, high-resolution TOF can be achieved.